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Comparison And Overview Of SCR Based ESD Protection Devices For CMOS ICs

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Abstract

An overview of SCR based ESD protection devices is made that recounts the working function, strong parameters and drawbacks of these devices. A brief history and evolution of some ESD protection device is also presented. This helps in understanding how a problem or a drawback in one device can be tackled or removed in a later device. In the end, a comparison of these devices is made based on some important values and characteristics, which can be speedily referred before designing an on-chip ESD protection circuit for CMOS ICs.

1. Introduction.

The phenomenon of Electrostatic discharge (ESD) takes place between two or more objects at different electrostatic potentials. This causes high momentary current to flow in the body through which the discharge occurs. ESD is differentiated into different model by ESDA. These have varying effects on the IC [1]-[4]. Devices are usually damaged by ESD due to thermal breakdown in silicon or melting of metal used in connection, caused by high-current or high-voltage overstress. If a low power CMOS IC is zapped with ESD, the complete IC or a part of it may get damaged due to discharge over-current [5]. With the new technology, the operating voltages are getting reduces, because of which ESD has become a very serious concern. It is also verified that SCR based ESD protection devices are suitable for CMOS submicron and deep submicron technologies [6]. These devices have advantageous features such as very good ESD robustness, very small area and low power dissipation due to very low on-resistance [19]. Moreover, the power dissipation i.e. I_{ESD} X V_H of SCR based device is far less than that of other ESD protection devices such as diodes, BJTs, etc. The response of an ESD protection device is recorded and observed using a Transmission Line Pulse setup and the turn-on time is defined as the time interval measured from 90% to 10% of the falling edge of voltage [7].

Low-Voltage Triggered SCR (LVTSCR) is one of the SCR based devices that can provide effective on-chip ESD protection [8]. LVTSCR, Lateral SCR (LSCR) and Modified Lateral SCR (MLSCR) [9], Boundary MOS Triggered SCR devices (BPTSCR and BNTSCR) [17] [18] are innovative structures whereas there are some triggering technique based devices that can replace these devices. Some these devices are gate-coupled technique [10], the GGNMOS-triggered technique [11], [12], the substrate-triggered technique [13], [14], double-triggered technique [15]. All these devices can be used to provide good on-chip ESD protection and are briefed in the later sections. These devices are later compared. The resulted are tabulated in table 1.

2. Working of SCR.

A SCR device can be represented using its two transistor model as shown in fig. 1. Fig. 2 shows the V-I characteristics of this device. It consists of a NPN and a PNP transistor connected to each other to form a 2 terminal/ 4 layer device PNPN structure. The fig also suggests use of various layers in standard CMOS processes to achieve this design. Anode is connected to positive supply while cathode is connected to negative

side. The hole current flows through PNP transistor and electron current flows through NPN transistor as long as the voltage drop in Rnwell and Rp is greater than 0.7 V. This is known as triggering (Vt) of SCR. The positive feedback keeps the device in conducting condition. After successful triggering, this mechanism allows regeneration of carriers, making the holding value of voltage Vh to drop. If this device is reverse biased, the parasitic diode between well and substrate gets forward biased thus giving rise to the curve on the left half [16] of fig. 2.

A modification in this structure is use of Gate connection (G), connected to the P-subs. Such a device is used in power electronic applications. However this structure has some inherent problems such as high Vt, slow turn on speed, etc. making it less effective for ESD protection application in CMOS ICs. However, its ability to allow large current to flow through it even with small device area promotes its usefulness. A number of devices have been developed based on this basic structure to provide good on-chip ESD protection.

3. Some SCR Based Devices.

A. Low-Voltage Triggered SCR (LVTSCR)

The structure of this device is shown in fig. 3. The switching voltage is equal to the drain breakdown or punch-through voltage of the nMOS device, about 7V for 0.25µm CMOS process [8]. Hence, the LVTSCR can provide good ESD protection even without a circuit, thus saving the layout area significantly. However, this is effective in protecting input stage only. To effectively protect the output stage, use of small resistor is suggested. Good ESD protection between I/O pads to VDD or VSS can be provided using complementary LVTSCR structures [8].

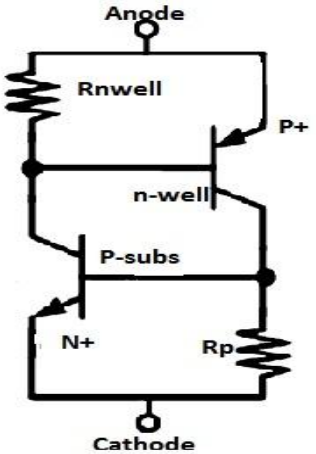

Fig. 1. Schematic of SCR showing its two transistor model

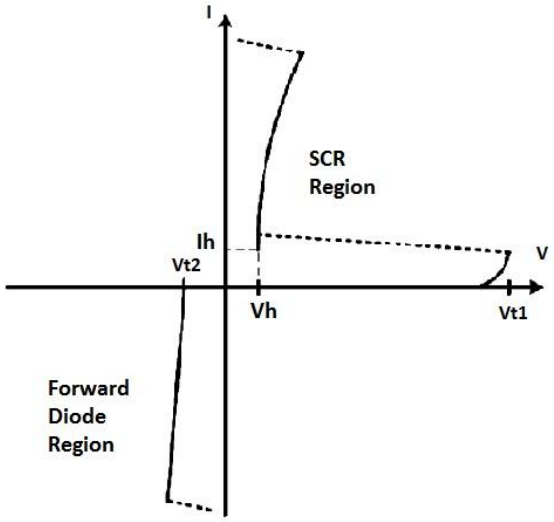

Fig. 2. V-I Characteristics of SCR device.

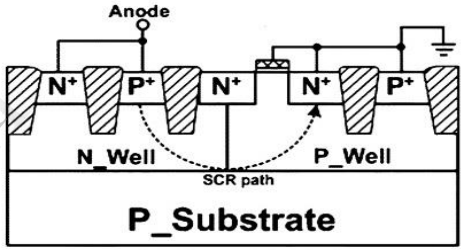

Fig. 3. Structure of LVTSCR

B. Gate-Coupled LVTSCR [10]

This device is useful in deep submicron processes wherein lower switching voltage is desirable for better ESD protection. Various modes of ESD stresses like PD, ND, NS and PS are considered [4]. PD stress is grounded using NMOS-triggered LSCR (NTLSCR) whereas the NS stress is grounded using a PMOS-triggered LSCR (PTLSCR). These two devices together form the complementary gate-coupled LVTSCR device. Fig. 4 shows the combined structure of these two devices.

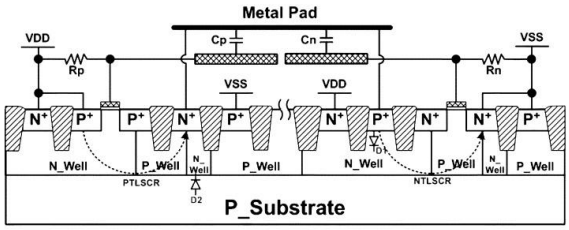

Fig. 4. Structure of Gate-coupled LVTSCR Device.

C. Substrate Triggered SCR (STSCR) [13] [14]

When a current is applied to the base or substrate of an SCR device, it can be quickly triggered on into its latching state. P-type substrate triggered SCR (P-STSCR) N-type substrate triggered SCR (N-STSCR) are the devices that employ substrate triggered technique for turning on the SCR. The structure of P-STSCR and N-STSCR are as shown in fig. 5 and 6 respectively. In P-STSCR an extra P+ diffusion is inserted into the P-well, which connects out as its p-trigger node. The case of n-trigger node in N-STSCR is similar. With the increase of substrate/ well- triggered current, the switching voltage of PSTSCR/NSTSCR device can be reduced to its holding voltage. The turn-on time of STSCR can also be reduced to about 10 ns under 5-V voltage pulse with 10-ns rise time with 0.25 µm CMOS process. The turn-on time can be further reduced by increasing the substrate/ well-triggered current [13] or reducing the rise time of voltage pulse [15]. With the lower switching voltage, the STSCR device can clamp the overstress ESD voltage to a lower voltage level more quickly to fully protect the ultrathin gate oxide of input stages. The STSCR device with dummy-gate structure had also been invented which further reduce the switching voltage and to improve the turn-on speed of STSCR.

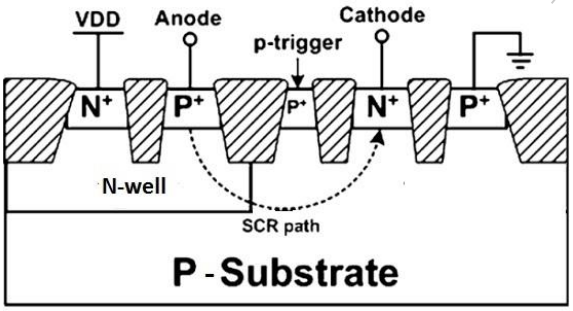

Fig. 5. Structure of P-STSCR.

D. Double Triggered SCR (DTSCR) [15]

Double triggering is another method to reduce the switching voltage and increase the turn-on speed of the SCR device. This is shown in fig. 7. The resulting device is named Double Triggered SCR (DTSCR). The extra P+ and N+ diffusions are inserted into the P-well and N-well of DTSCR device structure and connected out as the p-trigger and n-trigger nodes of the DTSCR device. The switching voltage of the DTSCR can be reduced to a lower voltage level more efficiently if the substrate and N-well triggered currents are synchronously applied to the p-trigger and n-trigger nodes, respectively. In a 0.25 µm CMOS process, when a 0-to-5 V voltage pulse with rise time of 10 ns is applied to the anode of the DTSCR, the turn-on time of the DTSCR is about 37 ns under the positive voltage pulse of 1.5 V at p-trigger node of DTSCR. The turn-on time can be further reduced with increasing the voltage biases at the p-trigger and n-trigger nodes or reducing the rise time of voltage pulse [15].

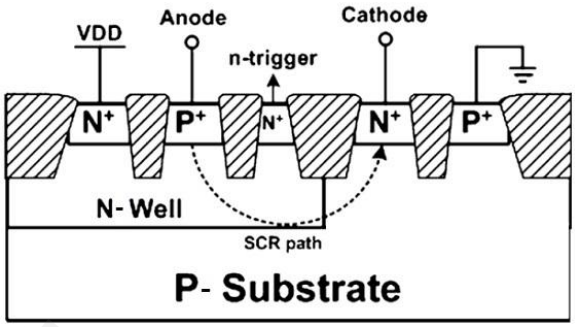

Fig. 6. Structure of N-STSCR

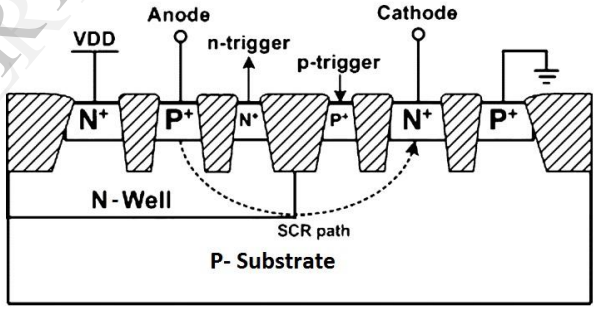

Fig. 7. Structure of DTSCR

E. Boundary MOS Triggered SCR [17] [18]

Boundary MOS Triggered SCR is a recently developed structure. It is an innovative design that does not contain any STI layer in the path through which current is conducted. The structure of Boundary P-MOS Triggered SCR (BPTSCR) and Boundary N-MOS Triggered SCR (BNTSCR) are as shown in fig 8 and 9 respectively. The MOS structure is located across the junction of N-well and P-well as a trigger element to provide trigger current from N-well to P-well. When trigger is applied at the gate of BPTSCR, the voltage on base of the NPN transistor will increase due to the substrate resistor. As long as the base voltage of the NPN transistor is greater than 0.7V, the NPN bipolar transistor in the SCR structure is active, which will further trigger the parasitic PNP bipolar

transistor owing to positive feedback regeneration mechanism. Subsequently, the BPTSCR will be successfully triggered into latching state to discharge the ESD current. The operation of BNTSCR is also similar. By changing gate length and other dimensions of the device, the trigger voltage, speed, holding voltage of the device can be changed. The turn on time of about 4nsecs has been reported [17] [18]. Also, the on-resistance of the device is very low, thus allowing high power dissipation.

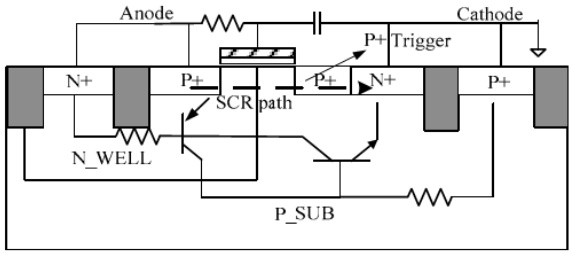

Fig. 8. Structure of BPTSCR.

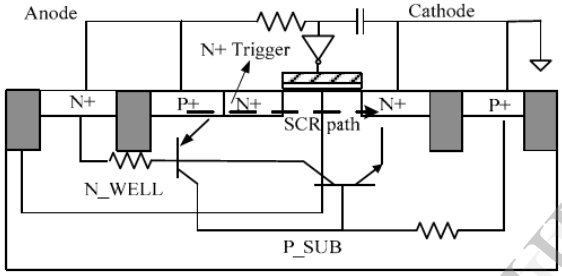

Fig. 9. Structure of BNTSCR.

4. Comparison.

With advancement in technology, feature size is reducing and the constant field scaling allows the supply voltage to be reduced. With newer technologies, this value has come very close to 1V which makes the on-chip SCR based ESD protection device free from latch-up concerns. Added to this, these devices have other advantageous features such as very good ESD robustness, very small area and low power dissipation due to very low on-resistance.

The following table (table 1) summarizes various important characteristics of some select SCR based ESD protection devices.

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Table 1. Comparison of some important SCR Based ESD protection devices

Name of Device	Switching Voltage	Turn-on Speed	Latch-up Problem	Usefulness (depending on switching voltage, turn-on speed and latch-up problem)
Lateral SCR (LSCR)	High	Slow	Present	Poor
Modified Lateral SCR (MLSCR)	Medium	Slow	Present	good
Low Voltage Triggered SCR (LVTSCR)	Low	Medium	Present	good
Gate Coupled LVTSCR	low and tuneable	fast	Present	Very good
GGNMOS Triggered SCR (GGSCR)	Low	fast	Present	Very good
Substrate Triggered SCR (STSCR)	low and tuneable	fast	Present	Very good
Double Triggered SCR (DTSCR)	low and tuneable	fast	Present	Very good
Boundary MOS Triggered SCR (BMTSCR)	low and tuneable	very fast	No	Excellent

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