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Comparison of FPGA based FIR filter using direct form and convolution based algorithm

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Abstract

To achieve greater flexibility, higher performance (in terms of attenuation and selectivity), better time and environment stability in signal processing operations, we adopted the digital signal processing (DSP) techniques. In this paper we focus on a digital signal processing system (digital filter) that resort a distorted signal and separates a combined signal. This work concentrates at first on the development of a low pass finite impulse response (FIR) digital filter using MatLab FDA tool then we designed two different methodologies for the implementation of a low pass finite impulse response digital filter: FIR using direct form method and FIR using convolution algorithm. These two methodologies are implemented using hardware description language (VHDL) as a design entity, and their synthesis by xilinx synthesis tool on Spartan 3 family XC3S4000l-4fg900 FPGA kit has been done. The experimental result shows that proposed delay free model using convolution algorithm requires less execution time than the traditional structure of the filter.

Keywords : VHDL, DSP, FIR, IIR, FPGA

1. Introduction

In signal processing a system that performs mathematical operations to reduce or enhance certain aspects of a signal is considered as the Digital filter [1]. These are the important class of LTI systems that performs mathematical operations on a sampled, discrete-time signal to reduce or enhance certain aspects of that signal. Basic Fourier Transform theory states that the linear convolution of two sequences in the time domain is the same as multiplication of two corresponding spectral sequences in the frequency domain. Filtering is in essence the multiplication of the signal spectrum by the frequency domain impulse response of the filter [2, 3].

The general form of the digital filter difference equation is given in equation (1).

$$y(n) = -\sum_{k=1}^{N} a_k\, y(n-k) + \sum_{k=0}^{M-1} b_k\, x(n-k) \quad (1)$$

where y(n) is the current filter output, the y(n-k)‘s are previous filter outputs, the x(n-k)‘s are current or previous filter inputs, the ak‘s are the filter‘s feed forward coefficients corresponding to the zeros of the filter, the bk‘s are the filter‘s feedback coefficients corresponding to the poles of the filter, and N is the filter‘s order[4,5].

Depending upon the filter coefficient there are two type of digital filter if the coefficient are fixed then it is frequency selective filter and if the coefficients updated at each iteration in order to minimize the difference between the filter output and the desired signal then it is a adaptive digital filter. The frequency selective filters are of two type infinite impulse response (IIR) and finite impulse response (FIR)[6]. **IIR** filters have one or more non- zero feedback coefficients. That is, as a result of the feedback term, if the filter has one or more poles, once the filter has been excited with an impulse there is always an output. **FIR** filters have no non-zero feedback coefficient. That is, the filter has only zeros, and once it has been excited with an impulse, the output is present for only a finite (N) number of computational cycles[7].

In this paper the architecture of FIR filter is simulated using MATLAB and then it is implemented in FPGA

This FIR filter is verified by implementing a proposed structure of convolution technique using FPGA. The organization of the paper is as follows. In section II, an overview of the FIR filter, designed in MATLAB is presented. The direct form structure of FIR filter, implemented using FPGA is presented in section III. The proposed structure for the verification of FIR filter using convolution technique, implemented in FPGA is presented in section IV. Section V gives the conclusion.

2. Design of the FIR filter

A discrete-time filter produces a discrete-time output sequence for the discrete-time input sequence. In the Finite Impulsive Response (FIR) system, the impulse response sequence is of finite duration, i.e. it has a finite number of non-zero terms and hence the filter coefficients are also constant. The response of the FIR filter depends only on the present and past input samples (a causal system), thus making the system always stable [8, 9, 10]. FIR filter output samples can be computed using the following expression as given in equation (2).

$$y(n) = \sum_{k=0}^{N} h(k)\, x(n-k) \qquad (2)$$

Where X [k] is FIR filter input samples, h[k] are the coefficients of FIR filter frequency response and y[n] are FIR filter output samples. In this paper we have proposed a sixth order low pass FIR filter whose coefficients are shown in the table 1.

Table 1.

Transfer function coefficient	Coefficients
h(0)	0.01
h(1)	0.064
h(2)	0.443
h(3)	0.443
h(4)	0.064
h(5)	0.01

We have designed this low pass FIR filter using MatLab FDA tool with the specification as shown in the table 2. The magnitude and phase plot of the filter is shown in figure 1.

Table 2.

Filter parameters	Specification
Response type	Low pass
Order	6^{th}.
Stable	yes
Design method	Rectangular window
Cut off frequency (w_c)	0.25 (normalized)
Attenuation at cut off frequency	6 db

To design this filter we have used rectangular window method which is defined in equation (3) [11, 12].

$$\omega_R(n) \triangleq \begin{cases} 1, & -\frac{M-1}{2} \le n \le \frac{M-1}{2} \\ 0, & otherwise \end{cases} \qquad (3)$$

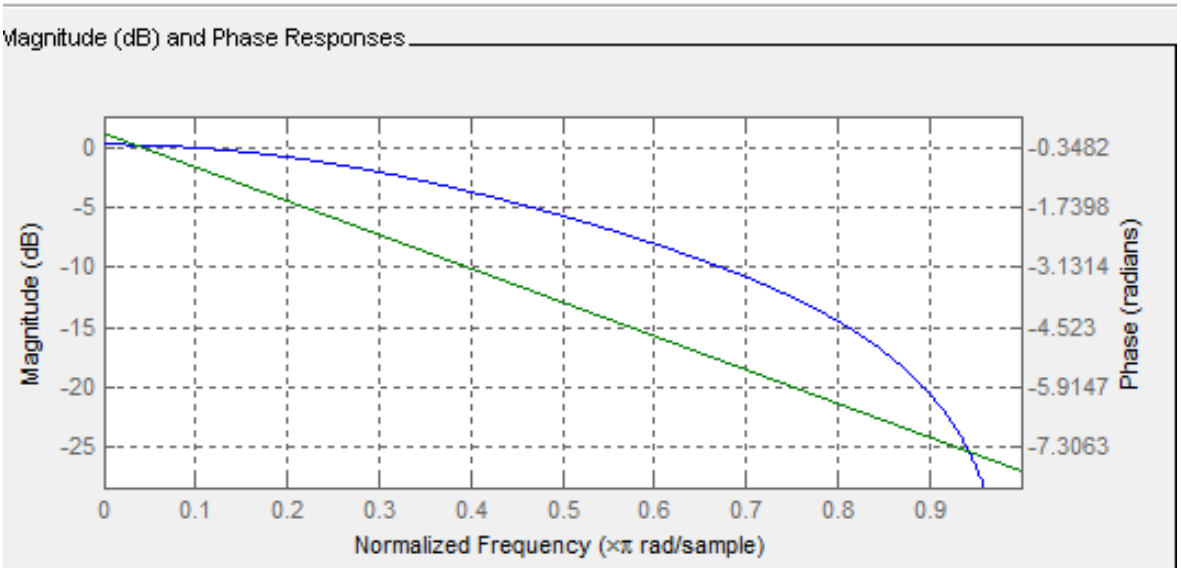


Figure 1. Magnitude and phase plot of the FIR filter.

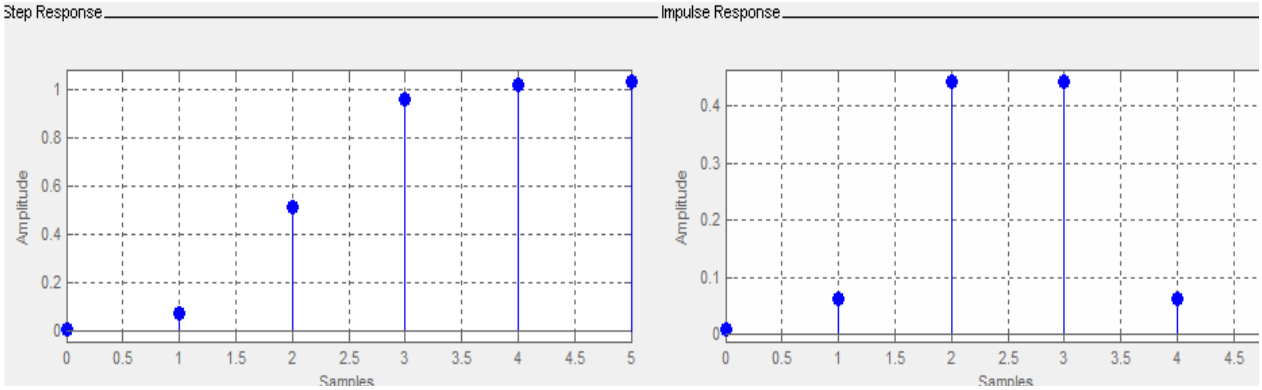


Figure 2. Step and Impulse response of the filter

Where 'M' is the window length in the samples. Here in our FIR filter the window length is six. The impulse response and the step response of the filter are shown in the figure 2.

3. Implementation of the FIR filter using direct form structure

Form the basic difference equation as given in equation (2), we can write the equation of the FIR filter as

$Y(n) = h(0)\,x(n) + h(1)\,x(n-1) + h(2)\,x(n-2) + h(3)\,x(n-3) + h(4)\,x(n-4) + h(5)\,x(n-5)$ (4) [13,14,15].

To implement this equation 4 we have used the direct form structure as shown in the figure 3. Here b (k) is the coefficient and z^{-1} is the delay flip flop[16,17]. To implement this filter in FPGA level we have to approximate the co efficient as shown in the table 3.

Table 3.

Transfer function co-efficient	Actual value	Approximate value	Binary equivalent value
h(0)	0.01	0.015625	0000000.00000100
h(1)	0.064	0.0625	0000000.00010000
h(2)	0.443	0.4453125	0000000.01110010
h(3)	0.443	0.4453125	0000000.01110010
h(4)	0.064	0.0625	0000000.00010000
h(5)	0.01	0.015625	0000000.00000100

Using these approximate values of the transfer function coefficient, we have implemented the filter in Spartan 3 family FPGA xc3s4000l-4fg900.To implement the direct form structure in FPGA we have used the logical elements like D flip flop as delay element adder for the addition operation and shift register[19,20,21]. The timing analysis using impulse response as the input and resource utilization for this structure of the FIR is shown in the figure 4 and figure 5.

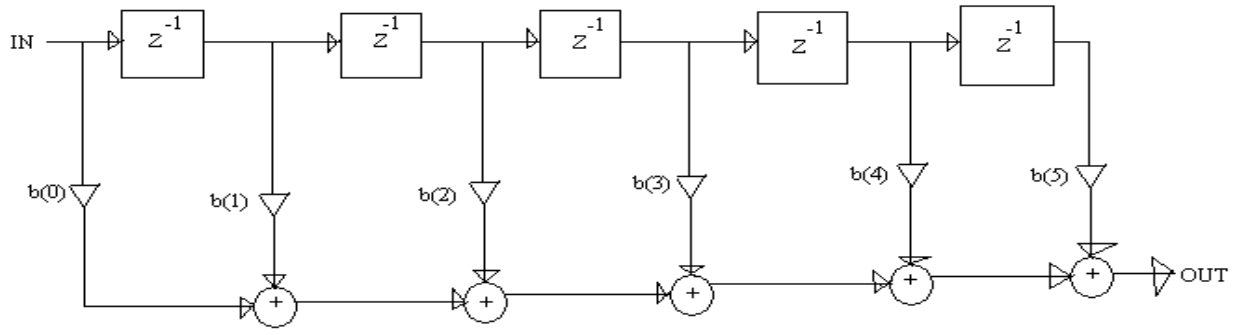


Figure 3. Direct form structure of the filter

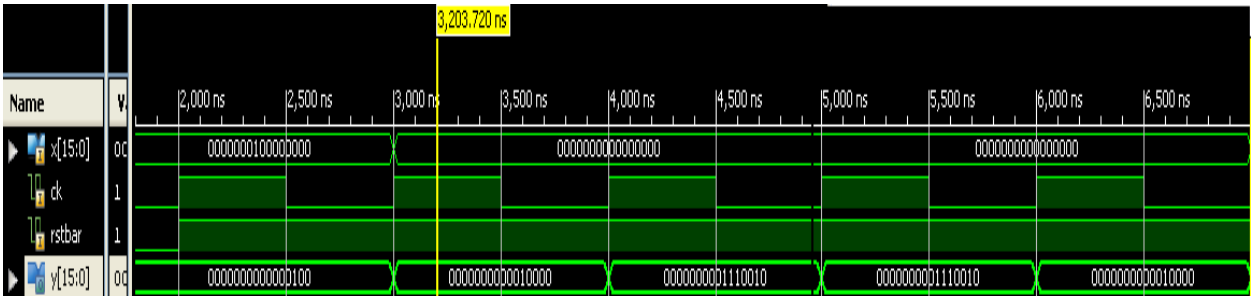


Figure 4. Simulation result of the direct form structure of the FIR filter

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	64	55,296	1%
Number of 4 input LUTs	277	55,296	1%
Number of occupied Slices	199	27,648	1%
Number of Slices containing only related logic	199	199	100%
Number of Slices containing unrelated logic	0	199	0%
Total Number of 4 input LUTs	277	55,296	1%
Number of bonded IOBs	32	633	5%
Number of BUFGMUXs	1	8	12%
Average Fanout of Non-Clock Nets	2.96		

Figure 5. Device utilization summary of the direct form FIR filter

4. Implementation of the FIR filter using proposed structure

Here in this section we have proposed the structure of FIR filter using the convolution technique[22,23,24,25]. We know that the output of any LTI system is given by equation 4.

$$y[n] = x[n] * h[n] \quad (4)$$

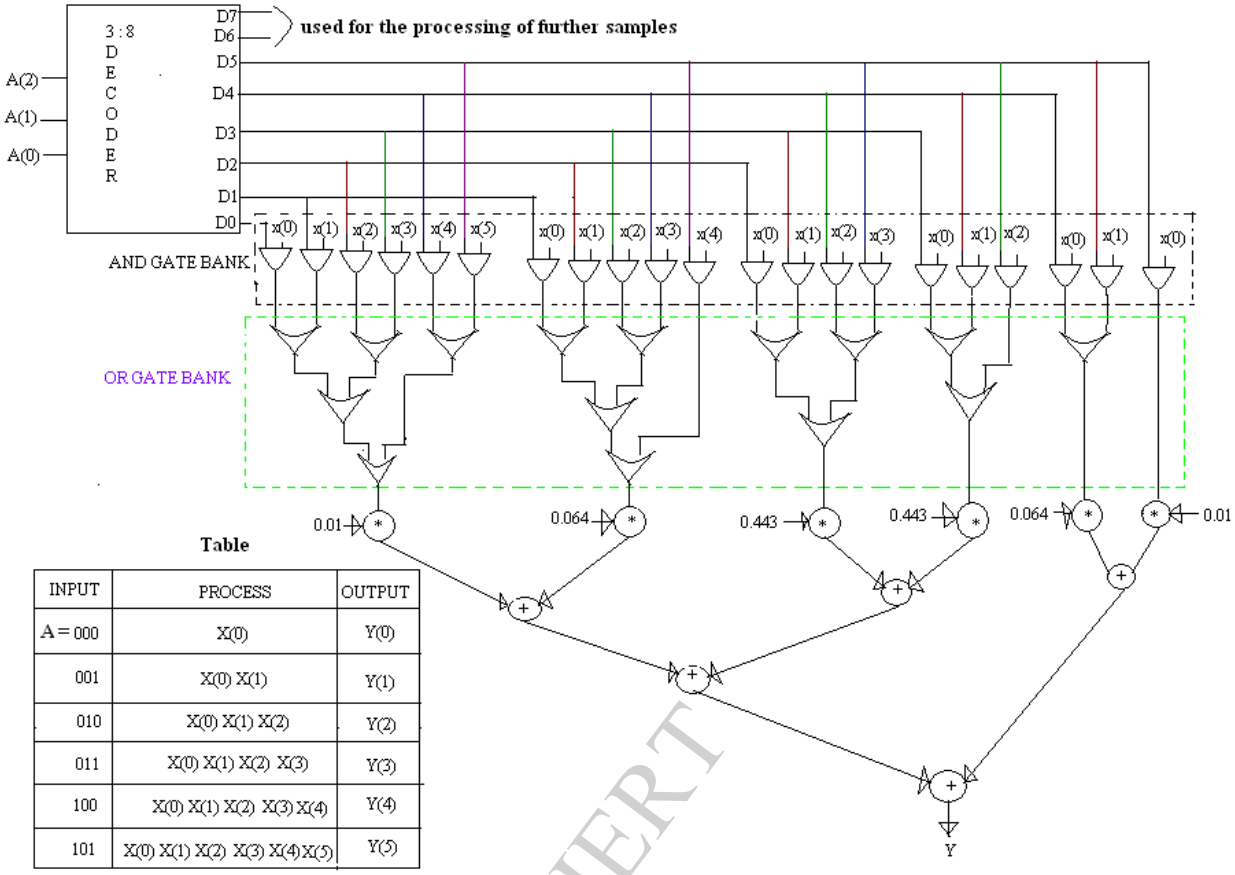
The system function of the FIR filter h[n] can be represented by the equation 5[26, 27].

$$h[n] = \sum_{k=0}^{M} b_k \, \delta[n-k] \quad (5)$$

Thus the output of the FIR filter y(n) can be defined using the equation 6[28,29,30].

$$y[n] = \sum_{k=0}^{M} b_k \, x[n-k] \quad (6)$$

Using these equation we can proposed the circuit of the FIR filter , using logical elements like banks of AND gate , OR gate , decoder , shift register and adder as shown in the figure(6).To operate this filter we have to use the table as given below. At first when the input of the decoder is set at "000" then D_0 output of the decoder will be enabled. This output will takes the input x(0) as shown in the figure (6) through the banks of AND and OR gates then the input x(0) will be multiplied with the first coefficient b_0.This process of multiplication will be performed by the shift register as shown in the figure(6), at last through the banks of adder we get our output y(0). Similarly if we set the input of the decoder "001" then D_1 output of the decoder will be enabled .This output D_1 will take input x(1) and x(0) through banks of AND and OR gates. In this way the process continues for all the samples. The timing analysis using impulse response as the input and resource utilization for the proposed structure of the FIR filter is shown in the figure 7and figure 8. The impulse response of this proposed structure is same as the direct form structure.



Table

INPUT	PROCESS	OUTPUT
A = 000	X(0)	Y(0)
001	X(0) X(1)	Y(1)
010	X(0) X(1) X(2)	Y(2)
011	X(0) X(1) X(2) X(3)	Y(3)
100	X(0) X(1) X(2) X(3) X(4)	Y(4)
101	X(0) X(1) X(2) X(3) X(4) X(5)	Y(5)

Figure 6. Circuit diagram of the proposed FIR filter

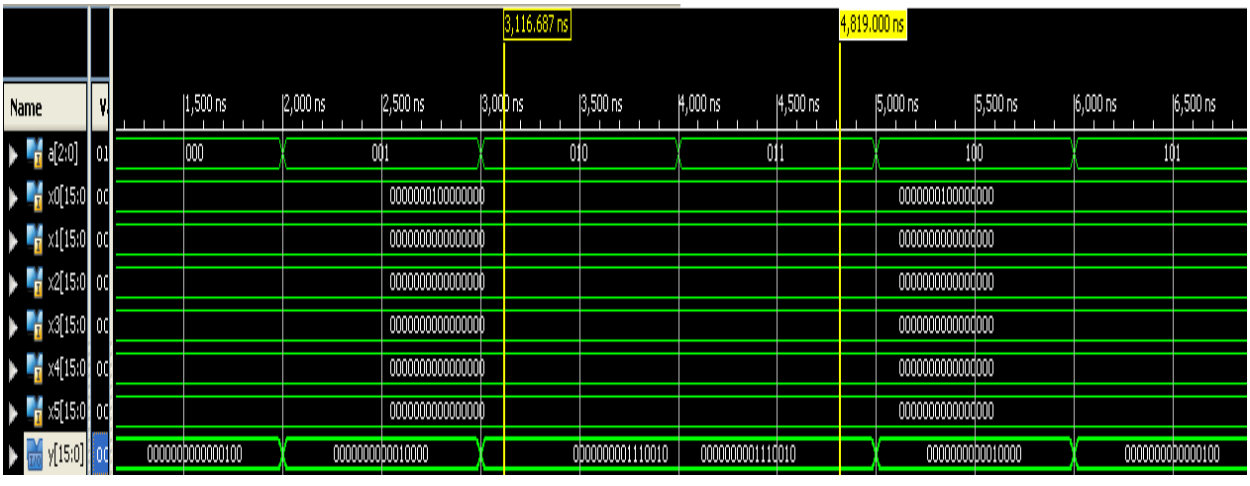


Figure 7. The timing analysis using impulse response

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Latches	6	55,296	1%	
Number of 4 input LUTs	443	55,296	1%	
Number of occupied Slices	247	27,648	1%	
Number of Slices containing only related logic	247	247	100%	
Number of Slices containing unrelated logic	0	247	0%	
Total Number of 4 input LUTs	443	55,296	1%	
Number of bonded IOBs	97	633	15%	
Average Fanout of Non-Clock Nets	2.97			

Figure 8. Device utilization summary of the proposed FIR filter

5. Conclusion

In this paper, we have presented a model that can implement a FIR filter using only combinational logic blocks. In this model the critical path delay is reduced and the power consumption for both structures is equal 0.268 watt. Thus using the delay free model we can reduce the computation time of the digital filter.

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