Comparison of Low Power Phase Frequency Detectors for Delay Locked Loop

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Abstract: In this paper, the performance of two low power and area efficient phase frequency detectors is compared. A Falling Edge PFD uses only 12 transistors. A FE-PFD consumes less power and therefore it is suitable for low power applications. This PFD operates up to 1GHz at 1.8V supply voltage. It is free from dead zone. High speed PFD uses 18 transistors. It is not free from dead zone. Both the circuits are designed and simulated using Tanner13.0v in 0.18um CMOS process with 1.8V supply voltage. These can be used in DLL for high speed, high frequency and low power applications.

Keywords: Phase Frequency Detector, Delay- Locked Loop, Maximum Operating Frequency, Dead Zone, Tanner

I. Introduction

In recent years, the design of low power Delay Locked Loop (DLL) for the different application has become one of the greatest challenges in high-performance very large scale integration (VLSI) design. As a consequence, many techniques have been introduced to minimize the power consumption of new VLSI circuits. Integrated DLL's play the versatile roles in the applications of time synchronization and multiphase clock generation clock [1]. A typical DLL architecture [2] is depicted in Fig.1. It consists of a phase frequency detector (PFD), a charge pump, a loop filter and a voltage-controlled delay line (VCDL).

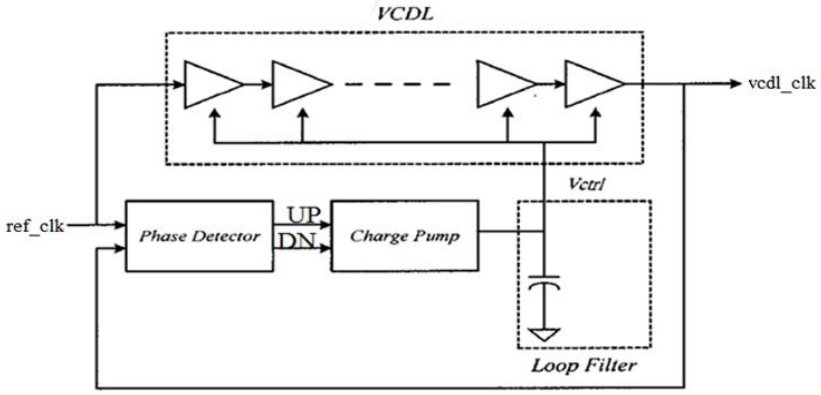

Fig.1 DLL Block Diagram

The PFD compares the rising edges of the reference clock and the VCDL clock, and generates a lead signal when the reference phase is leading or a lag signal when the reference phase is lagging. The phase difference detected in the PFD passes through the loop filer to control the VCDL. As the phase difference critically affects the overall characteristics of the DLL such as lock-in time and jitter performance, the PFD should be designed to work accurately for any phase difference.

II. Circuit Architecture with its Simulation

A. FALLING EDGE PFD

FE- PFD reduces the power consumption of the delay circuit by using simple architecture composed of only 12 transistors [3]. When REF and VCDL are low, UPb and DNb start pre-charging and then, UP and DN go low. UP and DN are high when both REF and VCDL are high. UP goes low at the falling edge of VCDL and DN goes low at the falling edge of REF. The difference in pulse width of UP and DN signals is equal to the phase difference between the input frequencies. The operation is identical for negative phase difference.Fig.2. shows the block diagram of FE-PFD.

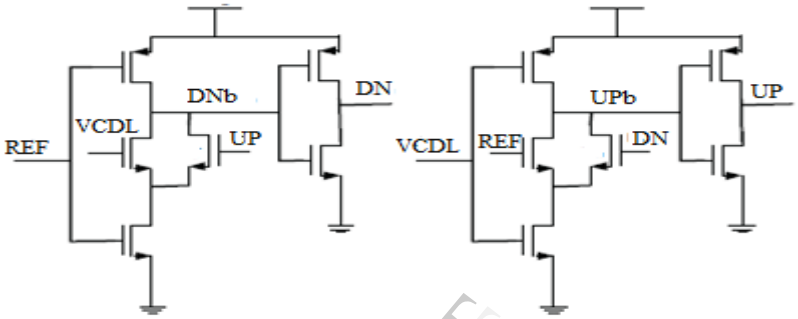

Fig.2 Falling Edge PFD

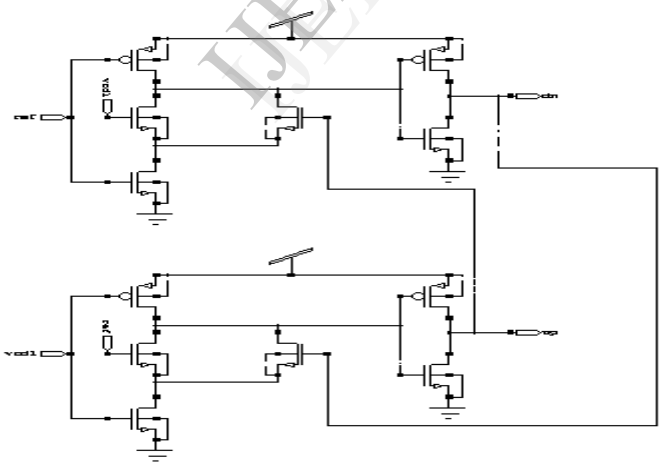

Fig. 3 Schematic of Falling Edge PFD

The phase frequency detector circuit can be analyzed in three different ways. One way in which ref signal leads vcdl signal, second in which ref signal lags vcdl signal and third ref signal is in phase with vcdl signal. In the first case, ref signal is leading vcdl signal. The difference in pulse width of UP and DN signals is equal to the phase difference between the input frequencies.

1. REF is leading

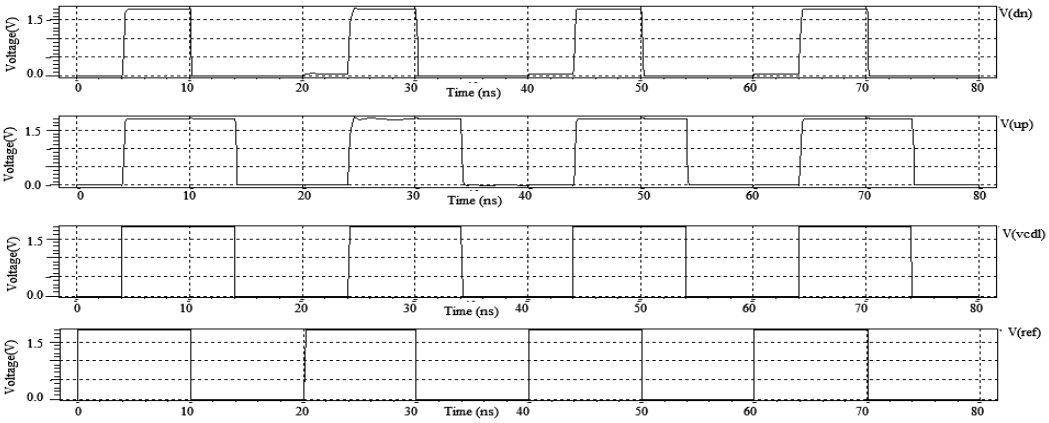

Fig.4 FE- PFD simulation I (ref signal leads vcdl signal)

2. VCDL is leading

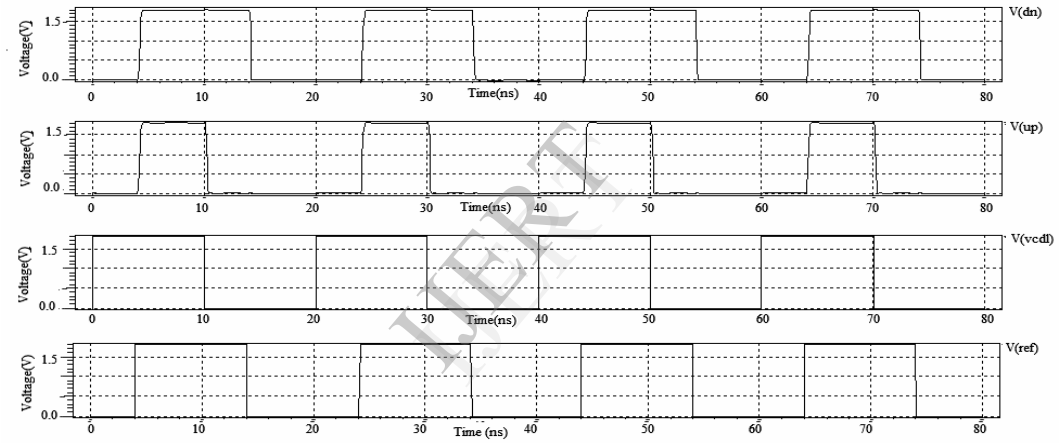

Fig. 5 FE-PFD simulation II (ref signal lags vcdl signal)

3. LOCK condition

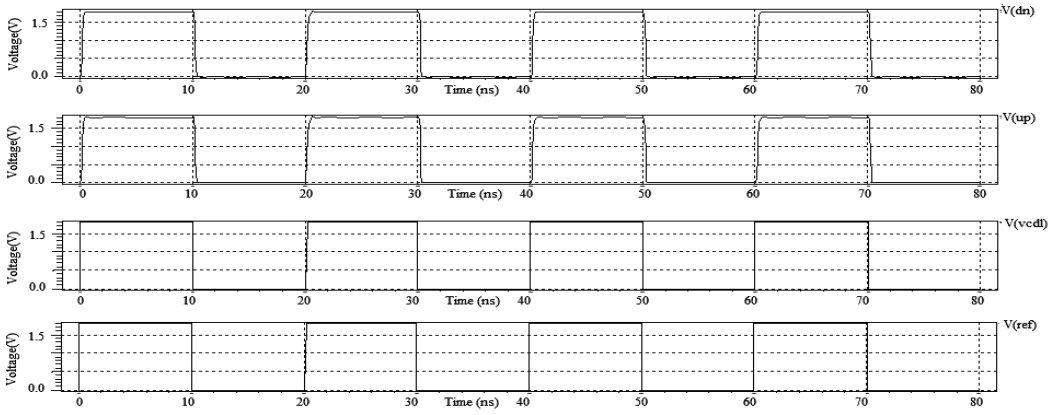

Fig.6 FE-PFD simulation III (ref signal is in phase with vcdl signal)

B. High Speed PFD

In the high speed PFD two invertors and NAND gates are added [4]. In this PFD the feedback path is totally eliminated compared to traditional PFD. So improvement is possible with high speed PFD which is another way to reduce the power consumption. In this PFD high speed is also achieved by detection of both the rising and falling edges of input signals. The pre-simulated output of this high speed PFD is shown in Fig 8, 9 and 10. These three conditions are ref clk leading, vcdl clk leading and lock condition. Fig 8 and 9 show the input leading signal condition. Fig. 10 shows the lock condition with UP and DN signals low. In this case the UP and DN signals are ground with very small spikes in place of pluses compare to conventional PFD. The resulted output shows the corresponding UP or DN signal high with the value of error generated between two input frequency signals. The schematic of High Speed PFD is shown in Fig.7

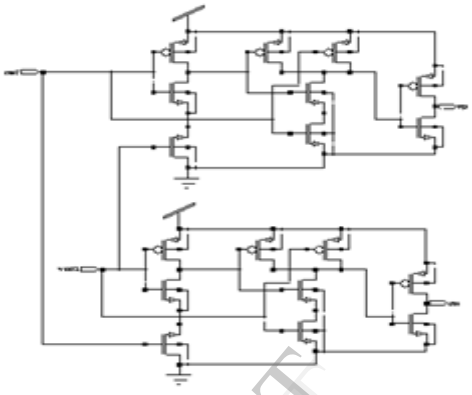

Fig.7 Schematic of High Speed PFD

In the first case, ref signal is leading vcdl signal. In this up pulse represents the difference between the phases of two clock signals.

1. REF is leading

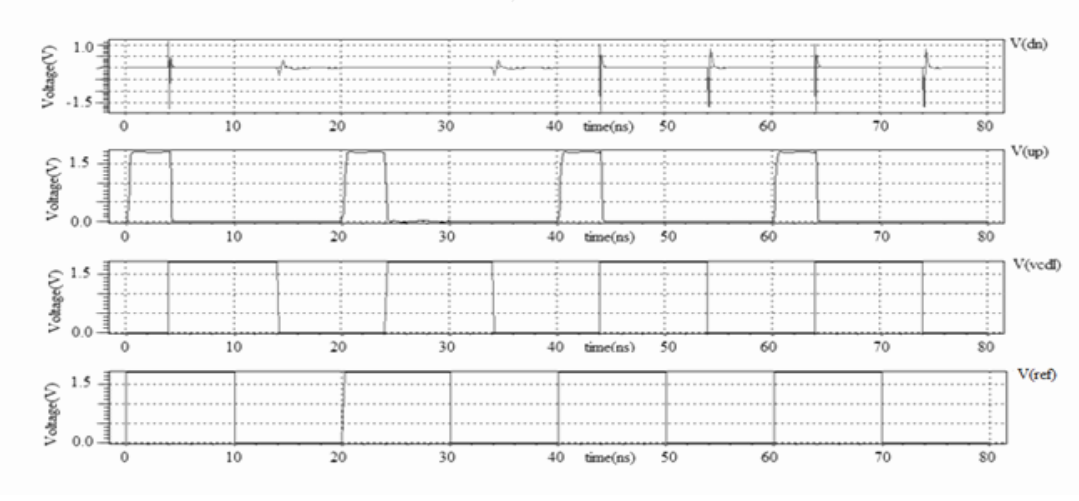

Fig.8 High Speed PFD simulation I (ref signal leads vcdl signal)

In the second case, ref signal is lagging vcdl signal. In this dn pulse represents the difference between the phases of two clock signals.

2. VCDL is leading

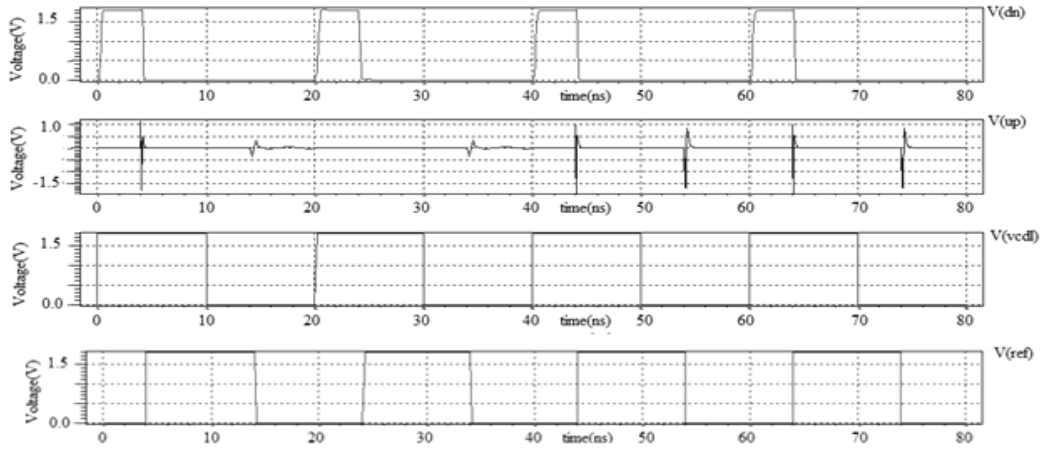

Fig. 9 High Speed PFD simulation II (ref signal lags vcdl signal)

In the third case, ref signal is in phase with vcdl signal. In this case, the loop is in locked state and small spikes are present on both the up and dn output.

3. LOCK condition

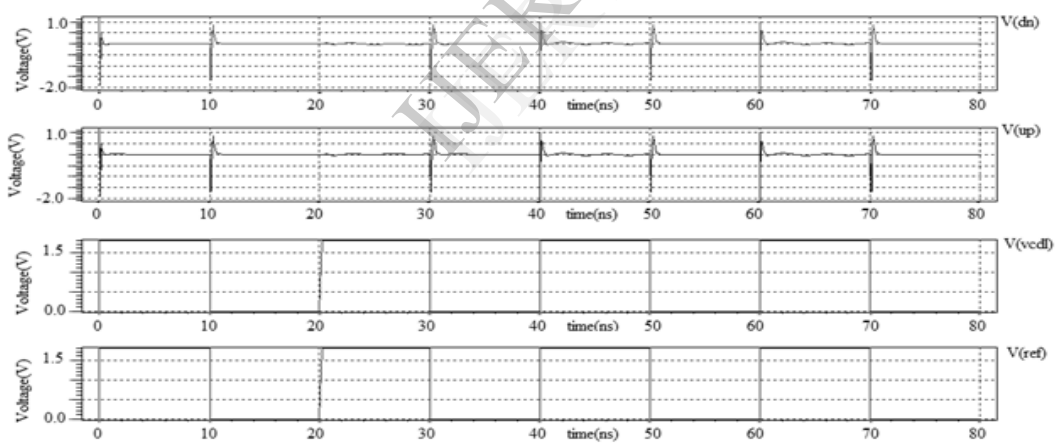

Fig.10 High Speed PFD simulation III (ref signal is in phase with vcdl signal)

III. Important terms of PFD

A. *Dead Zone*

Dead zone is due to small phase error, when both the input signals of PFD are very close to each other but output signals are not able to generate this error [5].Dead zone is due to the delay time of the logic components of digital circuit and the reset time that requires by the reset path to reset the flip flop of the PFD.

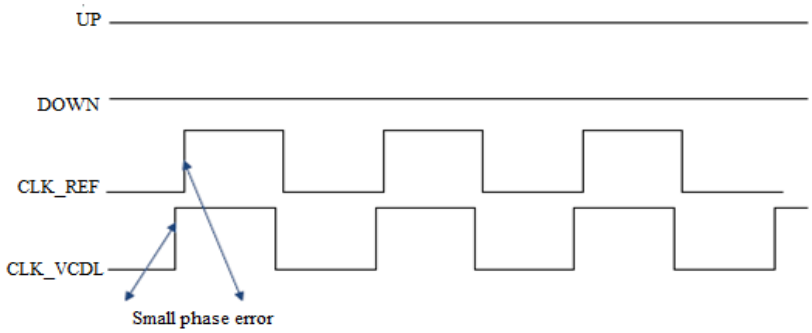

Fig. 11 Dead Zone

Fig.12 illustrates the output voltage vs. the phase error measured by the PFD. Fig.12(a) illustrates the relation in no dead zone PFDs, while Fig.12(b) illustrates the relation in the presence of a dead zone. We can see that in a dead zone PFDs the relation become nonlinear around zero. This is due to inability to detect the phase error in this region.

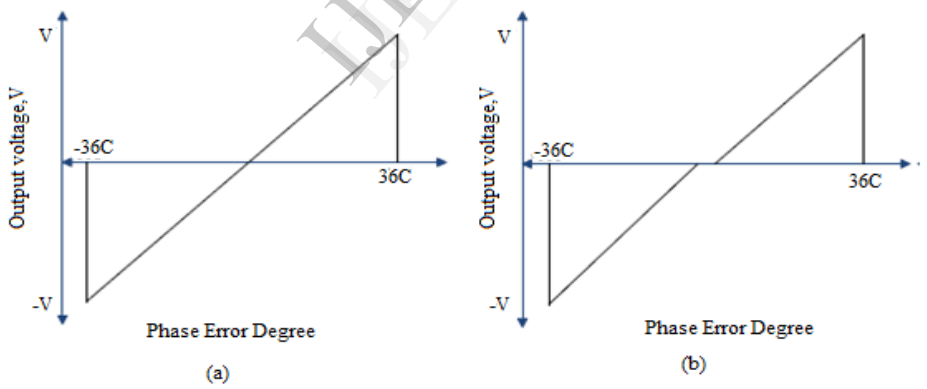

Fig 12 Phase Error vs. Output Voltage

(a) No Dead Zone (b) Dead Zone

B. *Maximum Operating Frequency*

The maximum operating frequency is defined as the shortest period with correct UP and DN signals together with the inputs have the same frequency and 90 degree phase difference [5].

IV. Performance Comparison

Table 1 depicts different parameters for the falling edge PFD and the high speed PFD for various parameters when both are designed on Tanner13.0v. It is seen that falling edge PFD has the lowest power and consumes less area compared to high speed PFD.

Table 1

Parameters	Falling Edge PFD	High speed PFD
Max operating frequency	1 GHz	1GHz
Power consumption(Watts)	6.951 e-006	8.513e-006
Transistor counts	12	18
Supply voltage	1.8v	1.8v
Dead Zone	Free	2 ps
Delay(sec)	1.4155e-008	4.2266e-009

V. Conclusion

This paper compares the performance of high speed PFD and FE-PFD. The power consumption of FE-PFD is found to be 6.951uW. Thus, it is suitable for low power applications and is free from dead zone problem. Whenever fast operation is required, high speed PFD is preferred as compared to FE-PFD. Dead zone of high speed PFD at 1GHz is only 2ps. So the dead zone is approximately zero and very small power consumption can be achieved by high speed phase frequency detector.

References

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