Comparison of Various Leakage Power Reduction Techniques for CMOS Circuit Design

Hina malviya
RKDF Institute of Sciecnce & Technology, Bhopal

Prof. Murli Manohar Hinnwar
RKDF Institute of Sciecnce & Technology, Bhopal

Abstract

Power consumption is now a major technical problem facing the CMOS circuits in deep submicron process. As process moves to finer technologies, leakage power significantly increases very rapidly due to the high transistor density, reduced voltage and oxide thickness. We first experimentally investigate existing low-power techniques and point out problems with them. We then propose a family of circuit types for low-power design centered around inserting controlling transistors between pull-up and pull down circuits as well as between pull-up circuits/pull down circuits and power/ground.We have compared different approach, named "sleepy keeper," which reduces leakage current while saving exact logic state. Sleepy keeper uses traditional sleep transistors plus two additional transistors – driven by a gate's already calculated output – to save state during sleep mode. In short, like the sleepy stack approach, sleepy keeper achieves leakage power reduction equivalent to the sleep and other approaches but with the advantage of maintaining exact logic state (instead of destroying the logic state when sleep mode is entered).. Unfortunately, sleepy keeper causes additional dynamic power consumption, approximately 15% more than the base case (no sleep transistors used at all). However, for applications spending the vast majority of time in sleep or standby mode while also requiring low area, high performance and maintenance of exact logic state, the sleepy keeper approach provides a new weapon in a VLSI designer's arsenal.

I. Introduction

In Deep Sub-Micron (DSM) technology, more number of gates is to be integrated on a single chip, so as to result in small geometries. But with this power densities and total power are rapidly increasing. Design of low power circuits has become important in a variety of application [1]. However reducing power consumption involves a trade off between timing and area at different stages of the design. The successful power sensitive design requires engineers to accurately and efficiently be able to perform these tradeoffs. To handle these issues efficiently, it is essential to understand the different types and source of power dissipation in the digital complementary metal oxide semiconductor (CMOS) circuits. The reason for choosing the CMOS technology is that it is the most dominant digital IC implementation technology. There are several VLSI techniques to reduce leakage power. Each technique provides an efficient way to reduce leakage power, but disadvantages of each technique limit the application of each technique [2]. We propose a new approach, thus providing a new choice to low-leakage power VLSI designers. Previous techniques are summarized and compared with our new approach presented in this paper.

The paper is organized as follows. Literature review about existing domino circuit discussed in section 2. Simulation result is presented and compared in section 3 with the brief conclusion of the paper in section 4.

II. Literature Review

A. SLEEP MODE APPROACH

One of the most commonly known traditional approaches for subthreshold leakage power reduction is the sleep approach [30-31]. In the sleep approach, additional transistors (sleep transistors) are inserted in between the power supply and ground. An additional "sleep" PMOS transistor is placed between VDD and the pull-up network of a circuit and an additional "sleep" NMOS transistor is placed between the pull-down network of the circuits and GND[2]. These sleep transistors turn off the circuit by cutting off the power rails. Figure 1 shows the structure of sleep approach. The sleep transistors are turned on when the circuit is active and provide very low resistance in the conduction path so that circuit‟s performance will not affects due to these additional transistors[3]. During the standby mode these transistors are turned off and introduce large resistance in the conduction path so that leakage power is reduced in the circuit. By cutting off the power source, this technique can reduce leakage power effectively. These types of techniques are also called gated-VDD and gated- GND [2,9].

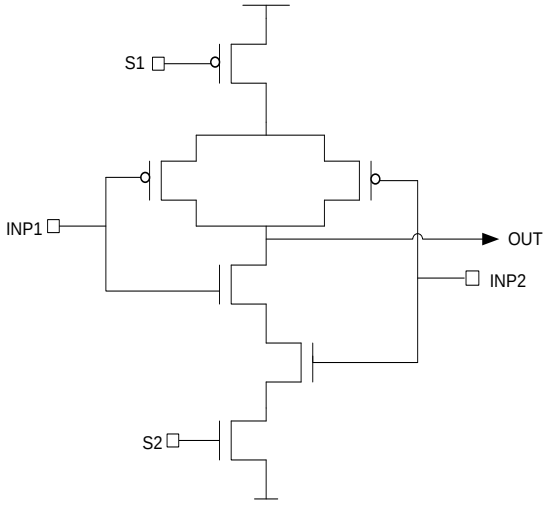

Fig. 1 Sleep Approach NAND gate

B.STACK APPROACH

Another leakage power reduction technique is the stack approach, which forces a stack affect by breaking down an existing transistor into two half size transistors. Subthreshold leakage is exponentially related to the threshold voltage of the device, and the threshold voltage changes due to body effect [4]. From these two facts, one can reduce the subthreshold leakage in the device by stacking two or more transistors serially [5]. The transistors above the lowest transistor will experience a higher threshold voltage due to the difference in the voltage between the source and body as shown in Figure 2. Also, the Vds of the higher transistor is decreased, since the intermediate node has a voltage above the ground. These results in reduction of DIBL effect hence better leakage savings. However, forced stack devices have a strong performance degradation that must be taken into account when applying the technique [3-5].

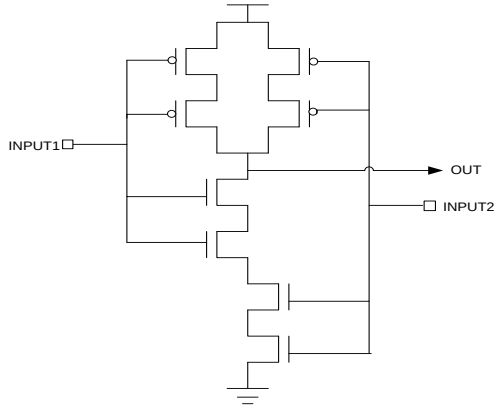

Fig. 2 Stack Approach based 2 input NAND gate

C. SLEEPY STACK APPROACH

The main idea behind the sleepy stack technique is to combine the sleep transistor approach during active mode with the stack approach during sleep mode. The structure of the sleepy stack approach is shown in Fig. 3. The sleepy stack technique divides existing transistors into two transistors each typically with the same width half the size of the original single transistor"s width. Then sleep transistors are added in parallel to one of the transistors in each set of two stacked transistors; the divided transistors reduce leakage power using the stack effect while retaining state [5]. The sleepy stack technique divides existing transistors into two transistors each typically with the same width W1 half the size of the original single transistor"s width (i.e.W1 = W0/2), thus, maintaining equivalent input capacitance. The added sleep transistors operate similar to the sleep transistors used in the sleep technique in which sleep transistors are turned on during active mode and turned off during sleep mode [6]. During active mode, *S*=0 and *S'*=1 are asserted, and thus all sleep transistors are turned on. Due to the added sleep transistor, the resistance through the activated (i.e., "on") path decreases, and the propagation delay decreases (compared to not adding sleep transistors while leaving the rest of the circuitry the same, i.e., with stacked transistors). During the sleep mode, *S*=1 and *S'*=0 are asserted, and so both of the sleep transistors are turned off. The stacked transistors in the sleepy stack approach suppress leakage current. Although the sleep transistors are turned off, the sleepy stack structure maintains exact logic state. The leakage reduction of the sleepy stack structure occurs in two ways. First, leakage power is suppressed by high- transistors, which are applied to the sleep transistors and the transistors parallel to the sleep transistors. Second, stacked and turned off transistors induce the stack effect which also

suppresses leakage power consumption. By combining these two effects, the sleepy stack structure achieves ultra-low leakage power consumption during sleep mode while retaining exact logic state. The price for this, however, is increased area [4].

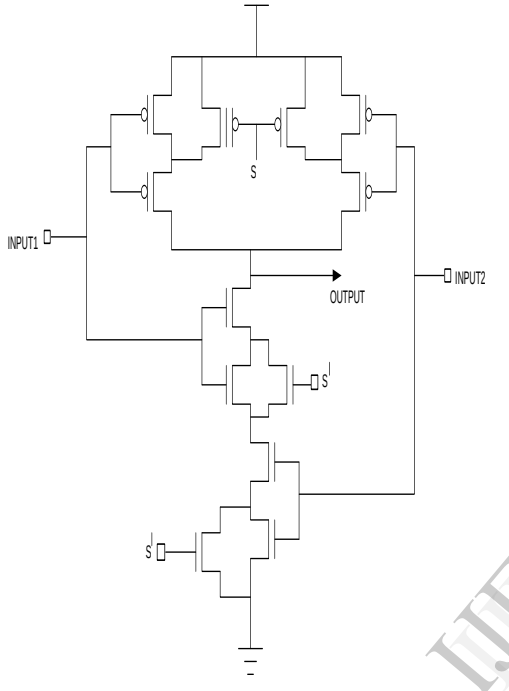

Fig. 3 Sleepy Stack Approach based 2 input NAND gate

D. SLEEPY KEEPER APPROACH

Another leakage power reduction technique is the "sleepy keeper" approach. The structure of the sleepy keeper approach as well as its operation is described here. The basic problem with traditional CMOS is that the transistors are used only in their most efficient, and naturally inverting, way: namely, PMOS transistors connect to VDD and NMOS transistors connect to GND [9]. It is well known that PMOS transistors are not efficient at passing GND; similarly, it is well known that NMOS transistors are not efficient at passing VDD. However, to maintain a value of „1" in sleep mode, given that the „1" value has already been calculated, the sleepy keeper approach uses this output value of „1" and an NMOS transistor connected to VDD to maintain output value equal to „1" when in sleep mode [7-8]. As shown in Figure 4,

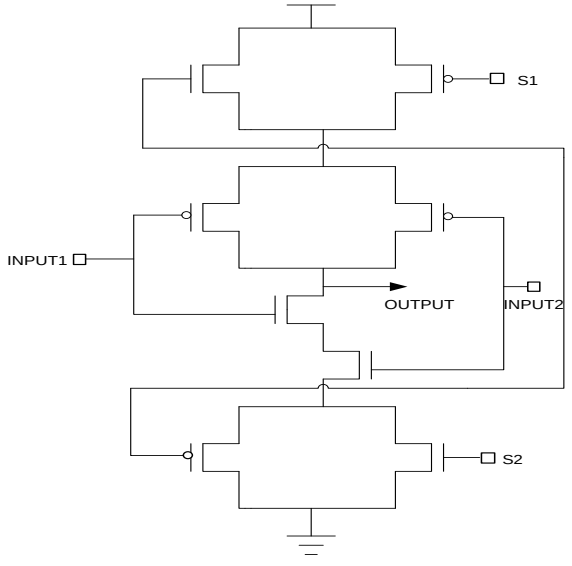

Fig.4. Sleepy keeper Approach based 2 input NAND gate

An additional single NMOS transistor placed in parallel to the pull-up sleep transistor connects VDD to the pull-up network. When in sleep mode, this NMOS transistor is the only source of VDD to the pull-up network since the sleep transistor is off. Similarly, to maintain a value of „0" in sleep mode, given that the „0" value has already been calculated, the sleepy keeper approach uses this output value of „0" and a PMOS transistor connected to GND to maintain output value equal to „0" when in sleep mode. As shown in Figure 4, an additional single PMOS transistor placed in parallel to the pull-down sleep transistor is the only source of GND to the case pull-down network which is the dual case of the output „1" explained above [3]. For this approach to work, all that is needed is for the NMOS connected to VDD and the PMOS connected to GND to be able to maintain proper logic state[11]. This seems likely to be possible as other researchers have described ways to use far lower VDD values to maintain logic state.

III. Simulation and Results

We have simulated 2 input NAND gate by applying sleepy approach, forced stack approach, sleepy stack approach and sleepy keeper approach. By analyzing the results of dynamic power consumption, average power consumption, static power consumption, delay and

power delay product (PDP). These circuit"s schematics are designed on cadence virtuoso schematic editor and simulated it by using spectre simulator on cadence virtuoso specter version 5.1.0. 65nm process technology has been used for designing these

circuits.The transistors are used in the smallest possible size i.e. channel length is taken as 60nm and channel width is taken as 90nm (W/L=1.5). The high threshold sleep transistors decrease the leakage in the circuit with the delay penalty. The main logic circuit is implemented with low threshold transistors to compensate the delay arises due to high threshold sleep transistors. In active mode, sleep transistors S1 and S2 are set as S1=0 and S2=1 sp that in active mode circuit can work properly. In sleep mode, sleep transistors are set as S1=1 and S2=0 so that there is no connection between VDD and GND in the sleep state and no leakage could flow through the circuit.

The transistors are used in the smallest possible size i.e. channel length is taken as 60nm and channel width is taken as 90nm (W/L=1.5). The high threshold sleep transistors decrease the leakage in the circuit with the delay penalty. The main logic circuit is implemented with low threshold transistors to compensate the delay arises due to high threshold sleep transistors. In active mode, sleep transistors S1 and S2 are set as S1=0 and S2=1 sp that in active mode circuit can work properly. In sleep mode, sleep transistors are set as S1=1 and S2=0 so that there is no connection between VDD and GND in the sleep state and no leakage could flow through the circuit.

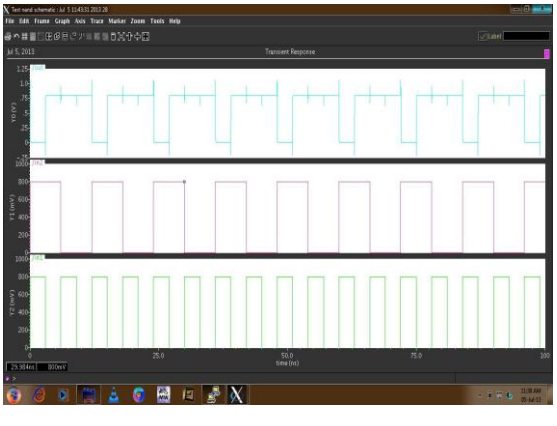

Fig. 5 Output waveform of 2 input NAND gate

TABLE I

Average power, Dynamic power, Static power, Delay and PDP for 2 input NAND gate

65nm	Average power (nW)	Dynamic power(nW)	Static power (pW)	Delay (pSec)	PDP (1E-21)
Base	47.35	47.15	197.4	18.212	3.595
Sleep	43	42.97	24.04	24.04	.602
Forced stack	61.64	61.62	15.45	40.105	.619
Sleepy keeper	42.83	42.79	35.97	23.42	.842
Sleepy stack	50.59	50.57	17.7	26.746	.473

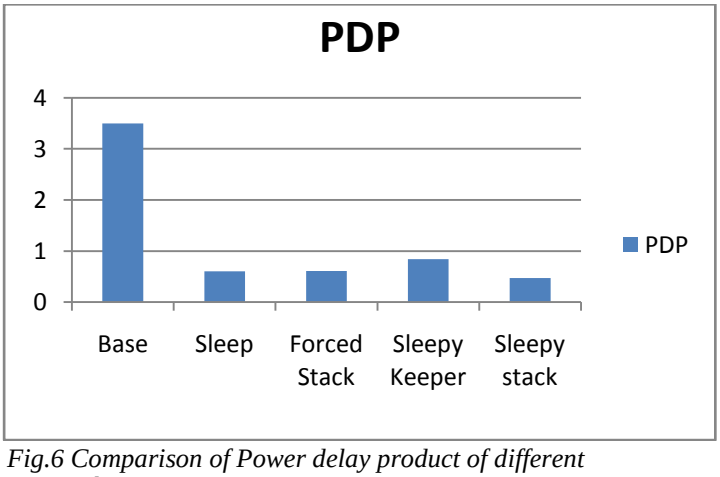

Fig.6 Comparison of Power delay product of different Approaches

IV.Conclusion

In nanometer scale CMOS technology, subthreshold leakage power is compatible to dynamic power consumption, and thus handling leakage power is a great challenge. In this paper, we compared a differnt circuit structure named "sleepy stack to tackle the leakage problem. The sleepy stack has a combined structure of four well-known low-leakage techniques, which are the forced stack, sleep transistor techniques. However, unlike the forced stack technique, the sleepy

stack technique can utilize high-Vth transistors without incurring large delay overhead. Also, unlike the sleep transistor technique, the sleepy stack technique can retain exact logic state while achieving similar leakage power savings. In short, our sleepy stack structure achieves ultra-low leakage power consumption while retaining state. In 2 input NAND gate we have achieved dynamic power reduction upto 20.03%, static power reduction upto 65.91%, delay increment upto 101.5% and PDP upto 40.20%.

References

[1] S. Mutoh et al., "1-V Power Supply High-speed Digital Circuit Technology with Multithreshold-Voltage CMOS," *IEEE Journal of Solis-State Circuits*, Vol. 30, No. 8, pp. 847-854, August 1995.

[2] M. Powell, S.-H. Yang, B. Falsafi, K. Roy and T. N. Vijaykumar, "Gated-Vdd: A Circuit Technique to Reduce Leakage in Deepsubmicron Cache Memories," *International Symposium on Low Power Electronics and Design*, pp. 90-95, July 2000.

[3] K.-S. Min, H. Kawaguchi and T. Sakurai, "Zigzag Super Cut-off CMOS (ZSCCMOS) Block Activation with Self-Adaptive VoltageLevel Controller: An Alternative to Clock-gating Scheme in Leakage Dominant Era," *IEEE International Solid-State Circuits Conference*,pp. 400-401, February 2003.

[4] Z. Chen, M. Johnson, L. Wei and K. Roy, "Estimation of Standby Leakage Power in CMOS Circuits Considering Accurate Modeling of Transistor Stacks," *International Symposium on Low Power Electronics and Design*, pp. 239-244, August 1998.

[5] J.C. Park, V. J. Mooney III and P. Pfeiffenberger, "Sleepy Stack Reduction of Leakage Power," *Proceeding of the International Workshop on Power and Timing Modeling, Optimization and Simulation*, pp. 148-158, September 2004.

[6] J. Park, "Sleepy Stack: a New Approach to Low Power VLSI and Memory," Ph.D. Dissertation, School of Electrical and Computer Engineering, Georgia Institute of Technology, 2005. [Online]. Available http://etd.gatech.edu/theses

[7] A. Kahng, S. Muddu, P. Sharma, "Defocus-aware leakage estimation and control**,"** *International Symposium on Low Power Electronics and Design*, pp. 263-268, Aug. 2005.

[8] G. Ribes, J. Mitard, M. Denais, S. Bruyere, F. Monsieur, C. Parthasarathy, E. Vincent, and G. Ghibaudo, "Review on high-k dielectrics reliability issues**,"** *IEEE Transactions on Device and Materials Reliability*, Vol. 5, Issue 1, pp. 5-19, March 2005.

[9] K. Flautner, N. S. Kim, S. Martin, D. Blaauw, and T. Mudge, "Drowsy Caches: Simple Techniques for Reducing Leakage Power," *Proceedings of the International Symposium on Computer Architecture*, pp. 148-157, May 2002

[10] H. Hanson, et al. Static energy reduction techniques for microprocessor caches. *Proc. of the Int. Conf. Computer Design*, 2001.

[11] http://www.microwind.org/

[12] J. Kao and A. Chandrakasan, "MTCMOS sequential circuits,"*Proceedings of European Solid-State Circuits Conference*, pp 332- 335, September 2001.

[13] Cadence Design Systems, http://www.cadence.com/.