Comparison of Various Switching Techniques for 7-Level Cascaded Multilevel Inverter: A Review

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Abstract— **Utilization of power semiconductor apparatus to enhance power quality may typically use active-power devices optimally operating with very high switching frequencies. This paper deals with comparison of various switching techniques like Stepped wave, In-phase Disposition carrier and Hybrid Level shifted carrier Pulse width modulation techniques for the control of a 7-level cascaded multi level inverter. Comparison is done in terms of design of the pulses and their operation.**

Keywords— Cascaded Multilevel inverter (CMLI), Hybrid modulation, sequential switching pulse, Multilevel Sinusoidal PWM, Hybrid In-phase Disposition (HIPD).

I. INTRODUCTION

The multilevel converters achieve high-voltage switching by the use of series of voltage steps, each of the individual power devices are within the ratings. Among the multilevel inverters, the cascaded H-bridge topology is attractive in high-voltage applications, because it requires the least number of components to obtain the same number of voltage level.

High-voltage capability with voltage limited devices; low harmonic distortion and increased efficiency are some of the special features of multilevel inverter. The cascaded multilevel inverter appears to be superior to other at high-power rating because of its modular nature of modulation, control and protection requirements of each full bridge inverter [2-6]. Many new modulations have been developed to meet the growing number of MLI topologies. They are aimed to generate a stepped switched waveform that approximates an arbitrary reference signal with adjustable amplitude, frequency and phase fundamental component.

Most of the modulation methods developed for multilevel inverters are based on multiple-carrier arrangements with PWM. The carriers can be arranged with vertical shifts or with horizontal displacements. In this paper, vertical displacements is considered i.e., level shifted carrier. With the use of hybrid modulation the performance of the MLI is improved. It also has the advantage of equal power dissipation among the power devices in a cell.

Comparison of the 7-level cascaded multilevel inverter with stepped pulses, In-phase Disposition and Hybrid IPD in terms of the voltage levels and the harmonics content is considered.

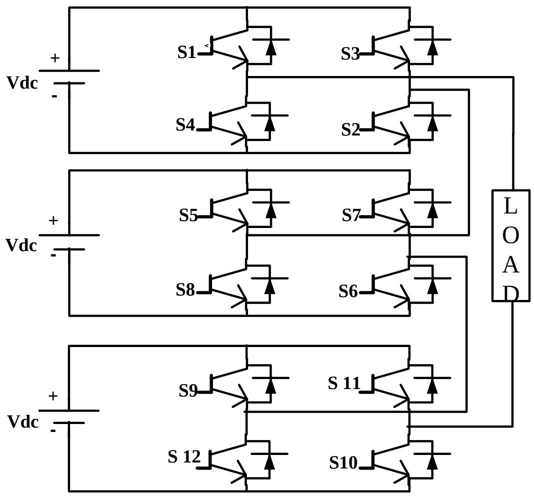

Fig.1. Schematic diagram of the inverter topology used to verify the proposed hybrid modulations.

II. PWM TECHNIQUE FOR CHB INVERTER

A. *Stepped Pulses*

The stepped pulses, this is the conventional topology for triggering of the cascaded multilevel inverter. Output voltage is a staircase wave, there will be rise of level with the pulse given to the corresponding H-bridge.

B. *In Phase Disposition PWM (IPDPWM)*

Fig.2 shows the in-phased disposition multi-carrier modulation scheme. A multilevel inverter with M no. of voltage levels it may requires (M-1) triangular carriers. In the

ISSN: 2278-0181
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level shifted multi-carrier modulation scheme, all the carriers have equalized magnitude & frequency[9]. The modulation index is

$$m_i = \frac{A_r}{A_c(M-1)} \quad (1)$$

Frequency modulation

$$m_f = \frac{F_c}{F_r} \quad (2)$$

Where Ar is the amplitude of reference sinusoidal waveform from peak to peak; Ac is the amplitude of carrier waveform; Fc is the frequency of the carrier waveform; Fr is the frequency of reference waveform.

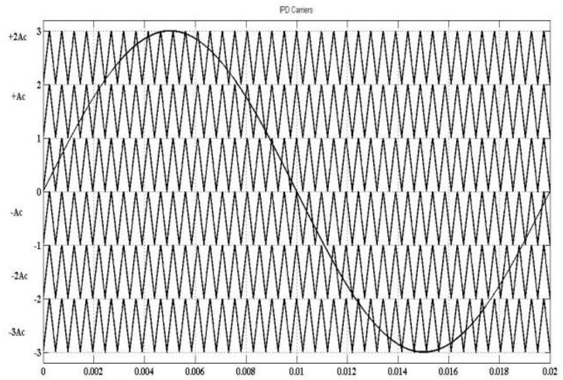


Fig.2. Level Shifted 5-Level IPD Carrier PWM

C. Hybrid In-phase Disposition

Fig.3 depicts the hybrid in-phase disposition 7 - level carrier waveforms for 7-level carrier PWM topology with three carrier waveforms for 7-levels correspondingly a sinusoidal reference. The m_i of this system is comparatively however the plentiful-ness to be viewed as Ar is the sufficiency of the reference sinusoidal waveform from least to most extreme amplitudes. The modulation index is

$$m_i = \frac{A_r}{A_c\left(\frac{M-1}{2}\right)} \quad (3)$$

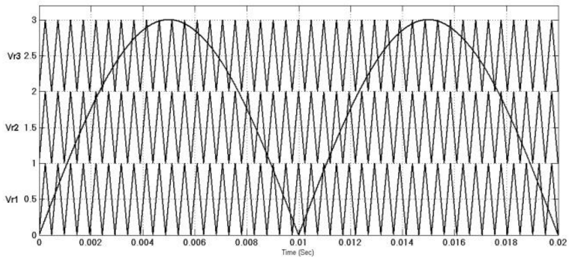


Fig. 3 Hybrid IPD 7 Level Carrier PWM

III. SEQUENTIAL SWITCHING HYBRID MODULATION SCHEME

A. Basic Principle of Modulation:

In the above topology a sinusoidal fundamental frequency is compared with the multiple carrier waves which are in vertical disposition to other as in Fig.2.

In this HIPD topology all the concern switches in H-bridge are operated at two diverse frequencies; three switches of 7-level H-bridge are worked at fundamental switched frequency and staying switches are operated with multilevel sinusoidal switching frequency.

In this topology all the four switches in the H-Bridge are operated at two various frequencies; three switches of 7-level H-Bridge are operated at Fundamental Frequency and remaining three switches are operated at the multilevel sinusoidal PWM frequency.

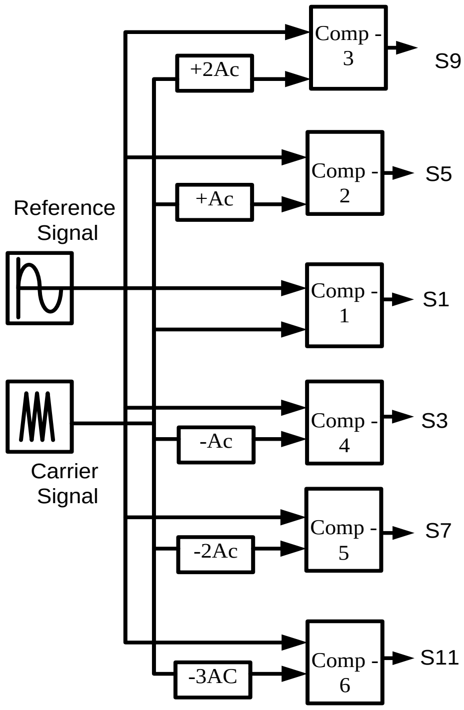


Fig.4 Block Diagram of 7- Level IPDPWM

Fig.4. shows the modulation of IPDPWM it has one reference wave which is compared with the six carrier waves and pulses were generated. This is the level shifted carrier PWM method. In addition to this 7-level HIPDPWM is developed. Table.1 gives the requirement of number of carrier waves for the IPD and Hybrid IPDPWM.

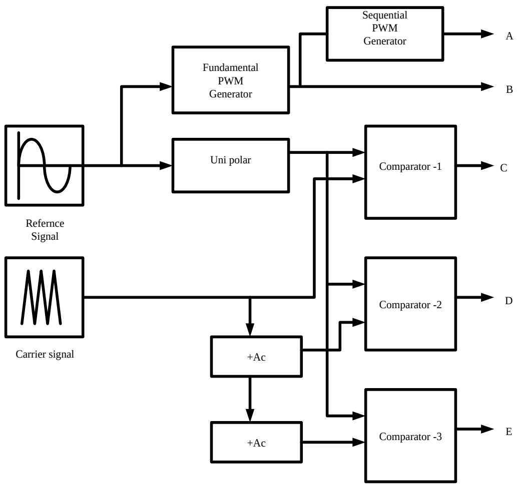


Fig.5. Sequential Switching of Hybrid Modulation.

B. Hybrid Modulation Scheme

A successive type sequential switching pulse type (SSP) will be square wave with 50% of duty ratios and it is a large portion of basic fundamental frequency. This signal makes each power switch to operate at MSPWM as well as FPWM arrangement to equalize the power loss among the power devices.

TABLE. I. REQUIRED NUMBER OF CARRIERS

Type of Method	Reference Wave	Carrier Wave
IPD	1	6
HIPD	1	3

FPWM (Fundamental Frequency Scheme) is additionally a square wave signal, synchronized with the modulated waveform. SSP (Sequential Switching Pulse) and FPWM pulses are same for all inverter cells. The general structure of the SSHM (Sequential Switching Hybrid Modulation) is demonstrated in Fig.5 [1].

C. Base PWM Circulator

A basic base modulation scheme is to get resultant hybrid PWM flow among the power modules. Where as if there should be arise an occurrence of 7-levels HIPDPWM the clock frequency is diminished to $f_0/6$ with three 3:1 multiplexer's, and choose one from the three PWM's focused around the time determination clock signal.

D. Hybrid Modulation Controller

This controller combines SSP, FPWM & MSPWM that achieves SSHM pulses. It is designed by using a simple combinational logic for a 7-level HIPDPWM is expressed (3) as [10]

$$\begin{aligned} &S1=BC'+\bar{A}B && S7=\bar{B}D'+\bar{A}\bar{B} \\ &S2=BC'+\bar{A}\bar{B} && S8=\bar{A}D'+A\bar{B} \\ &S3=\bar{B}C'+\bar{A}\bar{B} && S9=\bar{B}E'+\bar{A}B \\ &S4=\bar{B}C'+A\bar{B} && S10=BE'+AB \\ &S5=BD'+\bar{A}B && S11=\bar{B}E'+\bar{A}\bar{B} \\ &S6=BD'+AB && S12=\bar{B}E'+A\bar{B} \end{aligned} \quad (3)$$

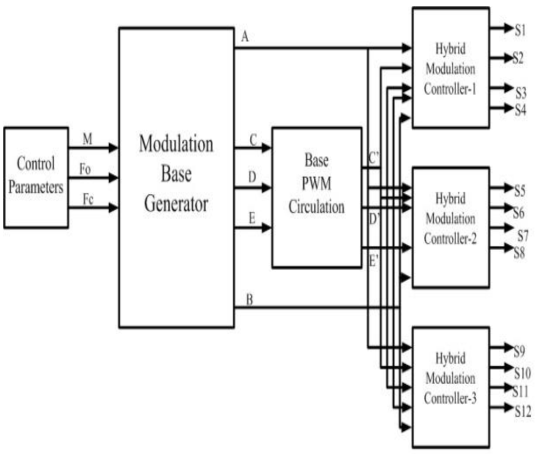


Fig.6. Sequential Switching Hybrid Modulation for Seven Levels

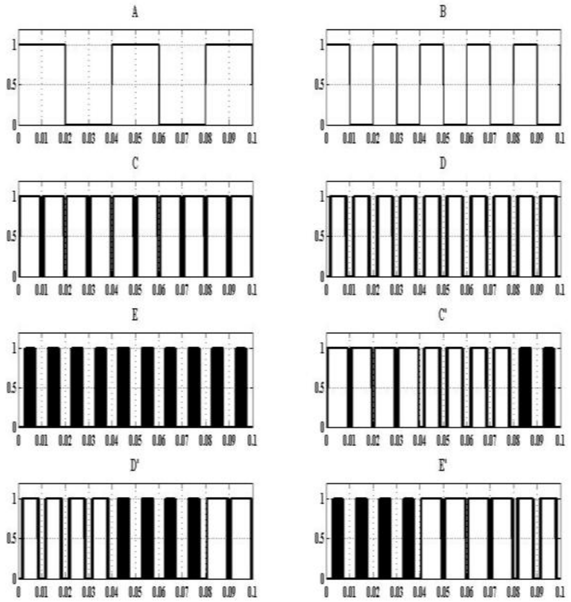
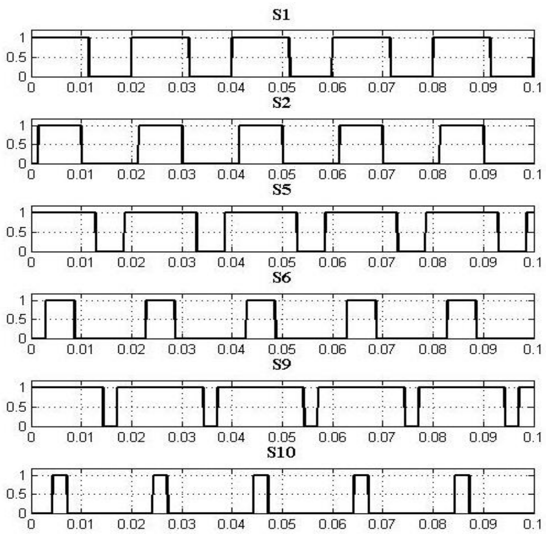


Fig.7. Low and High Frequency IPDPWM Pulses At m_i=1 And F_c=1050.

The switching pulses which are obtained from various modulation schemes are as follows in (a) and (b).

Fig. 8(a), (b) indicates the stepped pulses for 7 level cascaded multilevel inverter. Fig.8 (a) indicates the pulses fed for left half of the H-Bridge and Fig.8 (b) represents the pulses fed for the right half of the H-Bridges in Fig.1.

Fig 9(a) represents the 7-level IPDPWM pulses fed to the switches serving the positive half of the output voltage. Fig. 9(b) indicates the 7-level IPDPWM pulses fed to the switches serving the negative half of the output voltage.



(a)

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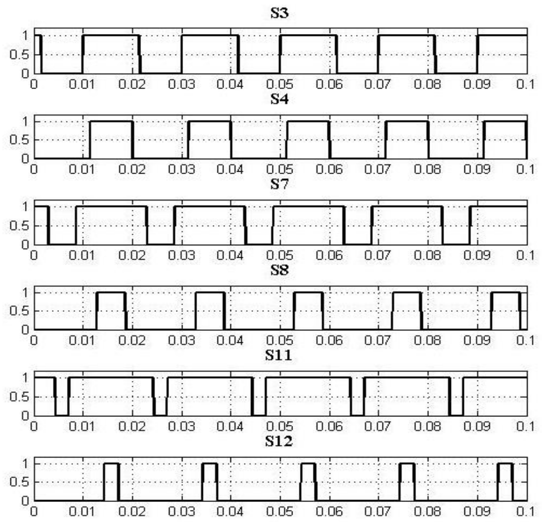
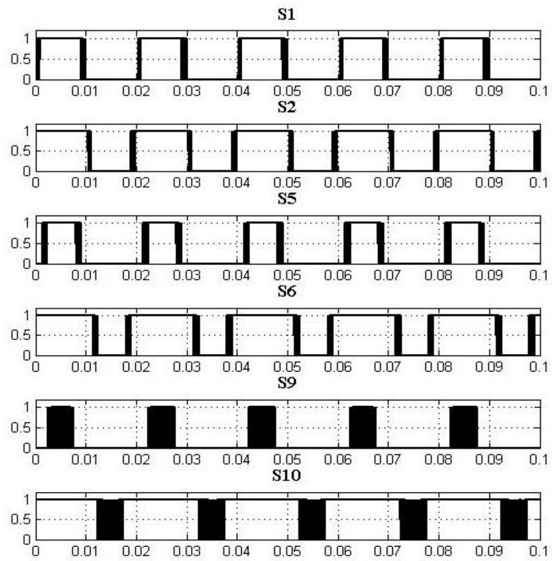
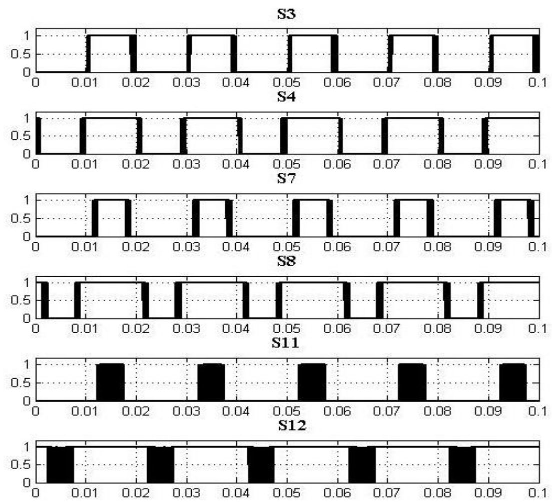


(b)

Fig. 8 (a), (b) Stepped pulses for 7-level CMLI

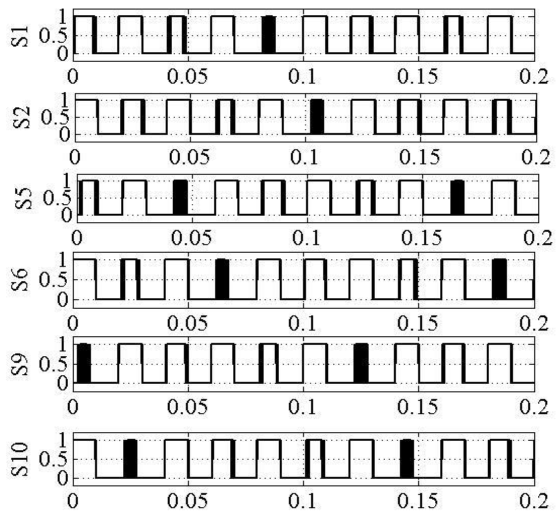


(a)

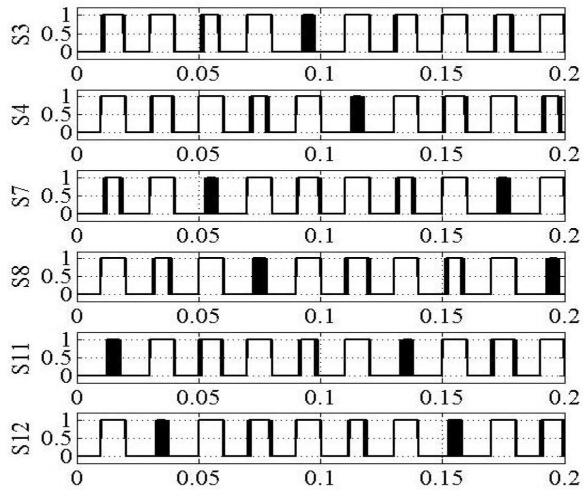


(b)

Fig.9 (a),(b). 7-level Pulses for CMLI using IPD PWM



(a)



(b)

Fig.10 (a), (b). Seven Level Sequential Switching IPDPWM Pulses.

Fig.7 depicts the representation the low and high frequency IPDPWM, in that A is the F0, B is the F0/2, C, D & E are the pulses from the comparators 1, 2 & 3. The C', D' & E' are the fusion of C, D & E, such that for the first cycle the particular pulse will be the yield for the second cycle an alternate pulse will be the yield pulse. This is acquired by utilizing the base PWM flow strategy. Fig.10 is the seven levels IPDPWM pulses produced from the circuit demonstrated in Fig.7. All the three techniques got have encouraged to the MLI with the comparing pulse names given to the separate switches of MLI [8].

IV. SIMULATION

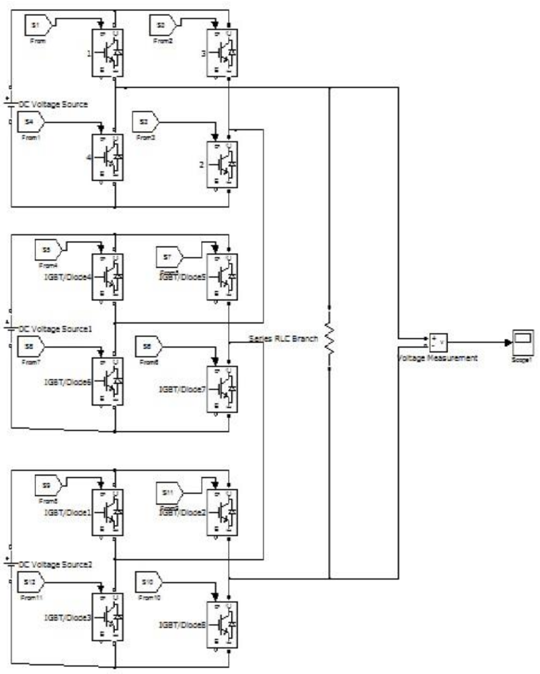


Fig.11. Simulation circuit of MLI.

The simulation is done by using MATLAB/SIMULINK software. The output voltage waveforms are observed for the three PWM methods. Fig.11 shows the MATLAB/Simulink model of cascaded multilevel inverter of 7-Level, in this three H-Bridges are connected in series connection.

V. RESULTS

For justification of comparison, a performance index namely total harmonic distortion (THD) was chosen to evaluate the three techniques and plotted. The THD is calculated using the equation (4). Up to 20^{th} order of harmonics is taken in to consideration [8].

$$THD=\frac{\sqrt{\sum_{n-2}^{50} V_n^2}}{V_1} \quad (4)$$

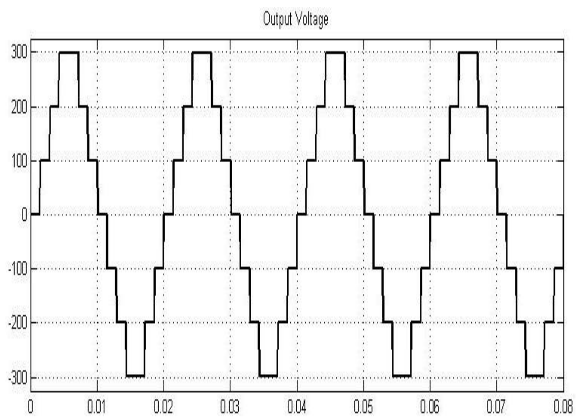


Fig. 12 7-level Line to neutral stepped inverter output voltage waveform

Fig.12 depicts the voltage waveform of the 7-level Line to neutral voltage of the CMLI controlled by the stepped pulses.

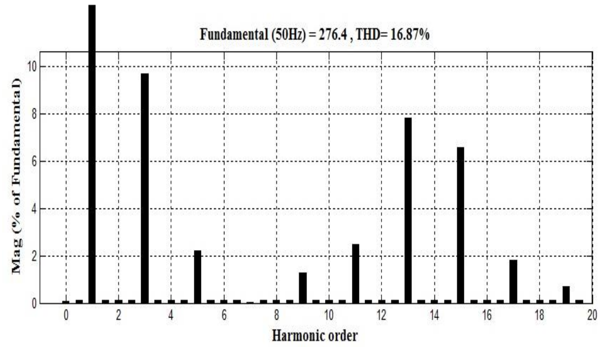


Fig.13 Harmonic spectrum of stepped pulsed CMLI.

Fig.13 shows the Harmonic spectrum of the output voltage which is obtained with the stepped pulses controller with the THD of 16.8% and voltage magnitude of 276.4V.

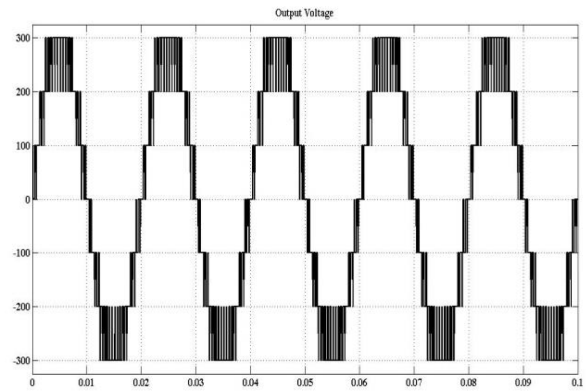


Fig.14 7-level Line to neutral Voltage waveform with IPDPWM

Fig.14 depicts the Line to neutral voltage waveform of the 7-level CMLI controlled by the In-phase disposition PWM.

Fig.15 shows the Harmonic spectrum of the 7-level CMLI output voltage waveform with THD of 18.23% and magnitude of 300V.

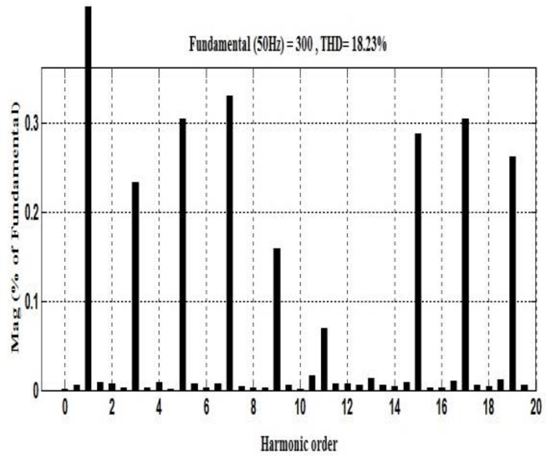


Fig.15 Harmonic spectrum of the 7-level CMLI with IPDPWM

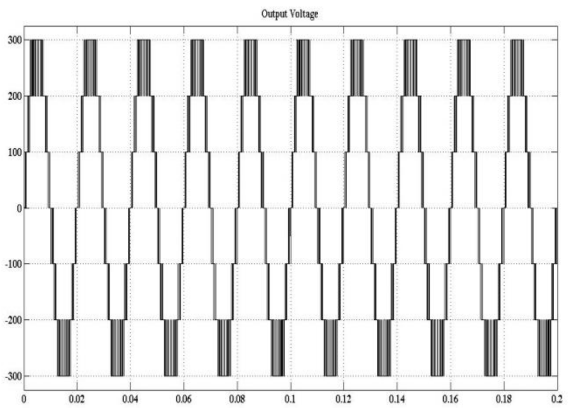


Fig.16 Line to neutral output voltage waveform for a 7-level inverter at mi=1 and fc=1050 Hz of new HIPDPWM

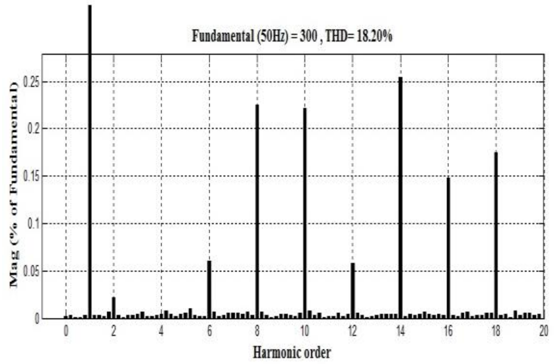


Fig.17. Harmonic spectrum of the line to neutral output voltage of HIPDPWM

Fig.16 shows the phase voltage waveform of the 7-level inverter with the Hybrid level shifted IPDPWM method under R-Load and Fig.17 shows the Spectrum analysis of the corresponding voltage waveform with the THD value of 18.20%.

Table II gives the list of harmonic content in terms of percentages for corresponding harmonic order from fundamental to 19th order with respective triggering methods of 7-level CMLI with the expected output voltage of 300V and fundamental frequency of 50Hz.

TABLE. II HARMONIC CONTENTS

Harmonic Order	**Harmonic percentage**		
	Stepped	**IPD**	**HIPD**
1	100	100	100
3	9.76	0.23	0
5	2.23	0.30	0.01
7	0.02	0.33	0.01
9	1.28	0.16	0
11	2.49	0.07	0
13	7.82	0.01	0
15	6.55	0.29	0.01
17	1.81	0.30	0
19	0.67	0.26	0

VI. CONCLUSION

An optimized hybrid level shifted PWM control scheme for cascaded multilevel inverter is discussed in this paper. A hybrid IPDPWM controller is designed to generate gate pulses for the inverter switches. When compared with the conventional Stepped pulses and the IPDPWM techniques with the hybrid PWM it acts as a moderate in between the other two types of methods. From the obtained data it can be conclude that though the THD value of the HIPDPWM value is slight greater than the conventional triggering method, but while considering the individual harmonic order in HIPDPWM the harmonic percentage is considerably decreased when compared to stepped and IPDPWM.

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