Published by :
http://www.ijert.org

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 5 Issue 01, January-2016

Control Algorithms of Distribution Static Compensator for Power Quality Improvement

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Abstract*—This Paper presents power quality improvement using distribution static compensator (DSTATCOM) based on simple peak detection control algorithm for balanced source conditions and a non-iterative optimized algorithm for unbalanced and distorted supply conditions. This topology contains two control methods. In Simple peak detection control algorithm a three-phase, four-wire distribution static compensator (DSTATCOM) based on the peak detection of load currents for power quality improvement under linear/non-linear loads is considered. In this control algorithm, an extraction of active and reactive power components of load currents is based on a low-pass filter and the voltage unit vector in time domain. It is based on the mathematical formulations for fast and accurate estimation of reference supply currents. A four-wire DSTATCOM is modeled and simulated for linear and non-linear loads and results are presented. Performance of DSTATCOM is found quite satisfactory under balanced and unbalanced loads in three-phase, four-wire distribution system. In Non-iterative Optimized Algorithm a single-step non-iterative optimized algorithm for a three-phase four-wire shunt active power filter under distorted and unbalanced supply conditions is simulated. The main objective of the proposed algorithm is to optimally determine the conductance factors to maximize the supply-side power factor subject to predefined source current total harmonic distortion (THD) limits and average power balance constraint. The proposed algorithm is simple and fast as it does not incorporate complex iterative optimization techniques, hence making it more effective under dynamic load conditions. Moreover, separate limits on odd and even THDs have been considered. A mathematical expression for determining the optimal conductance factors is derived using the Lagrangian formulation. Performance of DSTATCOM is found quite satisfactory and is capable of providing load compensation under steady-state and dynamic load conditions

Keywords—Zero Voltage Regulation, Voltage Source Converter, Static Synchronous Series Compensator, Matlab, Simulink

I. INTRODUCTION

Modern day power systems are complicated networks with hundreds of generating stations and load centers being interconnected through various power transmission lines. An electric power system has three separate components power generation power transmission and power distribution. As per reliability consideration in power system, generation unit must generate adequate amount of power, transmission unit should supply maximum power over long distances without overloading and distribution system must deliver electric power to each consumer's premises form bulk power systems. Distribution system is located at the end of electric power system and is directly to the consumer, so the power quality depends upon the state of distribution system. The reason for this is that failure in the electric distribution network accounts for about 91% of the average consumer's interruptions. Earlier, power system reliability focused on generation and transmission system due to capital investment in these. But today, distribution system is receiving more attention as reliability is concerned. The term electric power quality (PQ) is generally used to assess and to maintain the good quality of power at the level of generation, transmission, distribution, and utilization of AC electrical power. Since the pollution of electric power supply systems is much severe at the utilization level, it is important to study at the terminals of end users in distribution systems. There are a number of reasons for the pollution of the AC supply systems, including natural ones such as lightening, flashover, equipment failure, and faults (around 60%) and forced ones such as voltage distortions and notches (about 40%). A number of customer's equipment also pollute the supply system as they draw non-sinusoidal current and behave as nonlinear loads. Therefore, power quality is quantified in terms of voltage, current, or frequency deviation of the supply system, which may result in failure or mal-operation of customer's equipment. Typically, some power quality problems related to the voltage at the point of common coupling (PCC) where various loads are connected are the presence of voltage harmonics, surge, spikes, notches, sag/dip, swell, unbalance, fluctuations, glitches, flickers, outages, and so on. These problems are present in the supply system due to various disturbances in the system or due to the presence of various nonlinear loads such as furnaces, un interruptible power supplies (UPSs), and adjustable speed drives (ASDs). However, some power quality problems related to the current drawn from the AC mains are poor power factor, reactive power burden, harmonic currents, unbalanced currents, and an excessive neutral current in poly-phase systems due to unbalancing and harmonic currents generated by some nonlinear loads. Because of these problems, power quality has become an important area of study in electrical engineering, especially in electric distribution and utilization systems. It has created a great challenge to both the electric utilities and the manufacturers. Utilities must supply consumers with good quality power for

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 5 Issue 01, January-2016

operating their equipment satisfactorily, and manufacturers must develop their electric equipment either to be immune to such disturbances or to override them. A number of techniques have evolved for the mitigation of these problems either in existing systems or in equipment to be developed in the near future. It has resulted in a new direction of research and development (R&D) activities for the design and development engineers working in the fields of power electronics, power systems, electric drives, digital signal processing, and sensors. It has changed the scenario of power electronics as most of the equipment using power converters at the front end need modifications in view of these newly visualized requirements. Moreover, some of the well-developed converters are becoming obsolete and better substitutes are required. It has created the need for evolving a large number of circuit configurations of front-end converters for very specific and particular applications. Apart from these issues, a number of standards and benchmarks are developed by various organizations such as IEEE (Institute of Electrical and Electronics Engineers) and IEC (International Electro technical Commission), which are enforced on the customers utilities, and Manufacturers to minimize or to eliminate the power quality problems. The techniques employed for power quality improvements in exiting systems facing power quality problems are classified in a different manner from those used in newly designed and developed equipment. These mitigation techniques are further sub classified for the electrical loads and supply systems, since both of them have somewhat different kinds of power quality problems. In existing nonlinear loads, having the power quality problems of poor power factor, harmonic currents, unbalanced currents, and an excessive neutral current, a series of power filters of various types such as passive, active, and hybrid in shunt, series, or a combination of both configurations are used externally depending upon the nature of loads such as voltage-fed loads, current-fed loads, or a combination of both to mitigate these problems. However, in many situations, the power quality problems may be other than those of harmonics such as in distribution systems, and the custom power devices such as distribution static compensators (DSTATCOMs), dynamic voltage restorers (DVRs), and unified power quality conditioners (UPQCs) are used for mitigating the current, voltage, or both types of power quality problems. Power quality improvement techniques used in newly designed and developed systems are based on the modification of the input stage of these systems with power factor corrected (PFC) converters, also known as improved power quality AC–DC converters (IPQCs), multi pulse AC–DC converters, matrix converters for AC–DC or AC–AC conversion, and so on, which inherently mitigate some of the power quality problems in them and in the supply system by drawing clean power from the utility. This book is aimed at providing an awareness of the power quality problems, their causes and adverse effects, and an exhaustive exposure of the mitigation techniques to the customers, designers, manufacturers, application engineers, and researchers dealing with the power quality problems. Power quality is a set of boundaries that allows a system to work in its intended manner without significant loss of performance or life expectance. The power quality problems have been present since the inception of electric power. There have been several conventional techniques for mitigating the power quality problems and in many cases even the equipment are designed and developed to operate satisfactorily under some of the power quality problems. However, recently the awareness of the customers toward the power quality problems has increased tremendously because of the following reasons.

1.The customer's equipment have become much more sensitive to power quality problems than these have been earlier due to the use of digital control and power electronic converters, which are highly sensitive to the supply and other disturbances. Moreover, the industries have also become more conscious for loss of production.
2.The increased use of solid-state controllers in a number of equipment with other benefits such as decreasing the losses, increasing overall efficiency, and reducing the cost of production has resulted in the increased harmonic levels, distortion, notches, and other power quality problems. 3. It is achieved, of course, with much more sophisticated control and increased sensitivity of the equipment toward power quality problems.
4. Typical examples are ASDs and energy-saving electronic ballasts, which have substantial energy savings and some other benefits; however, they are the sources of waveform distortion and much more sensitive to the number of power quality disturbances. The awareness of power quality problems has increased in the customers due to direct and indirect penalties enforced on them, which are caused by interruptions, loss of production, equipment failure, standards, and so on.
5. The disturbances to other important appliances such as telecommunication network, TVs, computers, metering, and protection systems have forced the end users to either reduce or eliminate power quality problems or dispense the use of power polluting devices and equipment.
6. The deregulation of the power systems has increased the importance of power quality as consumers are using power quality as performance indicators and it has become difficult to maintain good power quality in the world of liberalization and privatization due to heavy competition at the financial level.
7. Distributed generation using renewable energy and other local energy sources has increased power quality problems as it needs, in many situations, solid-state conversion and variations in input power add new problems of voltage quality such as in solar PV generation and wind energy conversion systems.
8. Similar to other kinds of pollution such as air, the pollution of power networks with power quality problems has become an environmental issue with other consequences in addition to financial issues.
9. Several standards and guidelines are developed and enforced on the customers, manufacturers, and utilities as the law and discipline of the land.

There are a number of power quality problems in the present-day fast-changing electrical systems. These may be classified on the basis of events such as transient and steady state, the quantity such as current voltage, and frequency, or the load and supply systems. The transient types of power quality problems include most of the phenomena occurring in transient nature (e.g., impulsive or oscillatory in nature), such as sag (dip), swell, short-duration voltage variations, power frequency variations, and voltage fluctuations. The steady-state types of power quality problems include long-duration voltage variations, waveform distortions, unbalanced voltages, notches, DC offset, flicker, poor power factor, unbalanced load currents, load harmonic currents, and excessive neutral current

Interruption- A very short but complete loss of supply is called an interruption. An interruption occur when the supply voltage decrease less than 10% from its original value up to a period of time not exceeding one minute. The number of interruptions of the supply also tends to increase in deregulated environment like voltage sags and a suitable mitigation is essential. Flicker - Variation of input voltage sufficient in duration to allow visual observation of a change in electric light source intensity. Quantitatively, flicker may be expressed as the change in voltage over nominal expressed as a percent. For example, if the voltage at a 120-V circuit increases to 125V and then drops to 117 V, the flicker, *f*, is calculated as $f = 100 \times (125 - 117)/120 = 6.66\%$. Harmonic Distortion: A sinusoidal component of periodic waveform having a frequency that is an integral multiple of fundamental system frequency. The Nonlinear characteristics of devices and loads on the power system give rise to harmonic distortion. Harmonic distortion levels are described by the complete harmonic spectrum with magnitudes and phase angle of each harmonic component. Noise- Superimposing of high frequency signals on the waveform of the power system frequency. The level of electrical noise may produce interference signals, which exceed

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
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telecommunication immunity level. This increases the probability of transmission error rate. Voltage Unbalance- A Voltage variation in a three phase system in which the three voltage magnitudes or the phase angle differences between them are not equal. Induction furnaces, traction loads, or faults can lead to voltage unbalance. Unbalanced system means the existence of negative sequence that is harmful for all the three phase loads. The most affected loads are three phase induction machines. It is observed that power quality is major area of concern for power engineers now days. Reliability of supply is of utmost importance for the utilities to achieve global benefits Different types of custom power devices are proposed and analyzed to improve the power quality. As the major interruptions to customers are caused by failure in distribution system, so, more attention is given on the removal of voltage sags, swells and harmonics at the distribution end. In this thesis work, harmonics problem has been identified which is generally caused by the usage of power electronics based equipment's at the load side. These are termed as nonlinear loads. In order to improve the quality of power by reducing harmonics content in the load current, a custom power device called DSTATCOM is used and the results are obtained by using MATLAB/ SIMULINK. Following are the objectives of the work carried out.

II. PROPOSED MODELS

2.0 For Modeling Circuit these are the Specifications: the following system conditions for simple peak detection control algorithm. Ac mains: 415V (L-L), 50 HZ. Source impedance Load: 1) linear: 10KVA 0.8 power factor. 2) Nonlinear three phase full bridge uncontrolled rectifier with RL =15ΩLL = 100mH. Ripple filter Rf=5Ω,. Dc bus capacitance: 7500µF. Reference DC bus voltage: 700V. Frequency of low pass filter used in DC bus=12HZ. Frequency of low pass filter used in AC bus=12HZ. Interfacing inductor (Lf) =3.5mH. The performance of DSTATCOM using proposed peak detection control algorithm is simulated using MATLAB model for PFC and ZVR modes of operation under linear and non-linear loads. The performance of DSTATCOM is presented for linear and non-linear loads as Follows:

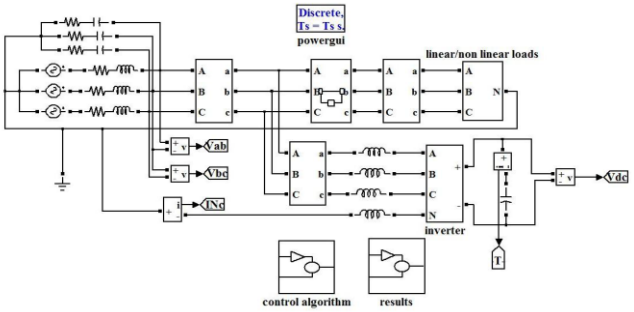

Fig.2.0 Simulink diagram for the simple peak detection method

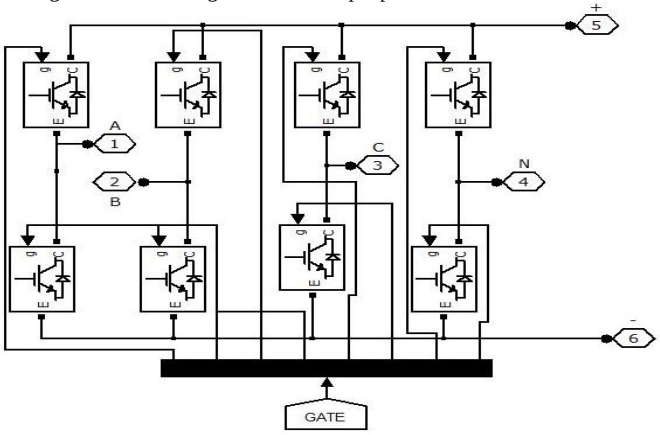

Fig 2.1 Modeling of the inverter

2.1. Performance of DSTATCOM in PFC mode: Fig2.2 and 2.3 shows the response of DSTATCOM for reactive power compensation under lagging power factor in PFC mode. The performance of DSTATCOM is shown as phase voltages at PCC (Vs), balanced supply currents (Is), load currents (ila,ilb and ilc), compensator currents (ica ,ibc and icc) and DC bus voltage (Vdc), load neutral current (Iln), supply neutral current (Isn), at the time of load removal on phase 'a' load at t = 2s. It shows the unity power factor after compensation of load reactive power demand through DSTATCOM and balanced supply currents during load unbalancing.

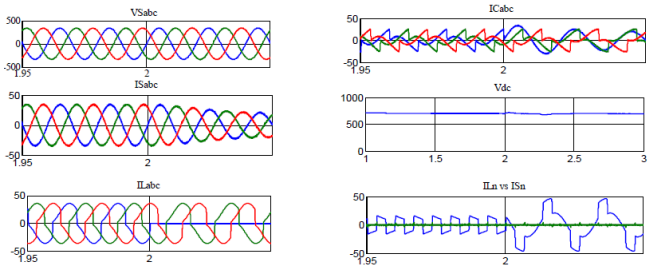

Fig 2.2 DSTATCOM performance in PFC mode

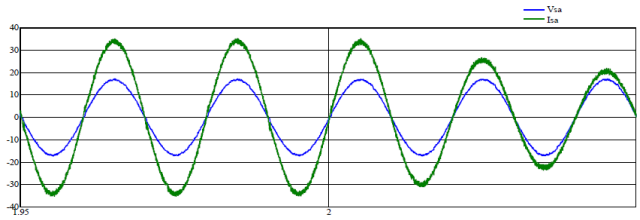

Fig2.3 Unity power factor in PFC mode

2.2. Performance of DSTATCOM in ZVR mode:

Fig 5.5 and 5.6 shows the response of DSTATCOM for reactive power compensation under lagging power factor under ZVR mode. The performance of DSTATCOM is shown as phase voltages at PCC (v s), balanced supply currents (i s), load currents (i_{la} ,i_{lb} and i_{lc}), compensator currents (i ca, i cb and i cc) and DC bus voltage (v_{dc}), load neutral current (iLn),supply neutral current (isn), at the time of load removal on phase 'a' load at t = 2s. The DSTATCOM will supply some extra leading reactive power components in addition to load reactive power demand in ZVR mode. This extra leading reactive power is required to regulate PCC voltage up to desired level. Basically it is generated by the action of PCC voltage PI controller.

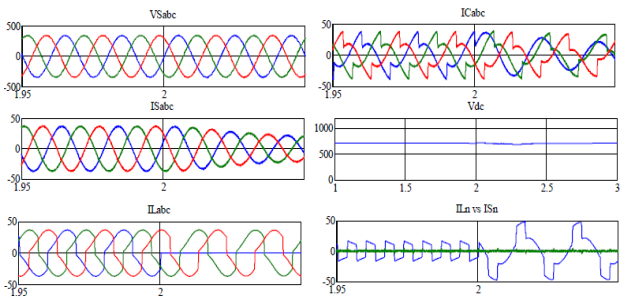

Fig 2.4 DSTATCOM performance in ZVR mode of operation

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
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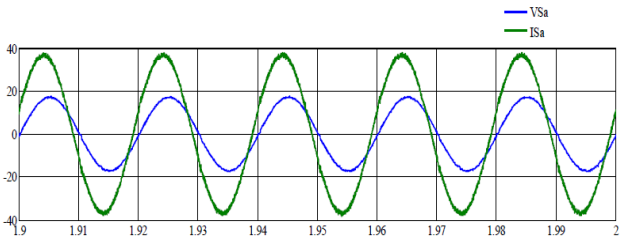

Fig 2.5 Leading power factor in ZVR mode of operation

2.3. A Non iterative optimization based control algorithm

Simulation results are taken for the following system conditions Supply voltage

$$v_{sb} = 415\sqrt{\frac{2}{3}}(1.2\sin(\omega t - 120) + .04\sin 2(\omega t - 120) + .04\sin 4(\omega t - 120) + .04\sin 5(\omega t - 120) \cdot .05\sin 7(\omega t - 120))$$

$$v_{sc} = 415\sqrt{\frac{2}{3}}(.8\sin(\omega t + 120) + .06\sin 2(\omega t + 120) + .06\sin 4(\omega t + 120) + .06\sin 5(\omega t + 120) + .04\sin 7(\omega t + 120))$$

$R_s = 1\Omega \qquad L_s = 10mH$

$R_f = 5\Omega \qquad C_f = 25\mu F$

$L_f = 6mH$

Linear load $\qquad R_{la} = 58\Omega$

$R_{lb} = 29\Omega \qquad L_{lb} = 100mH$

$R_{lc} = 29\Omega \qquad L_{lc} = 100mH$

Non-linear load 3φ full bridge rectifier with load impedance of DC bus capacitor 2000μF DC bus voltage 750v Simulink model for this method is given below

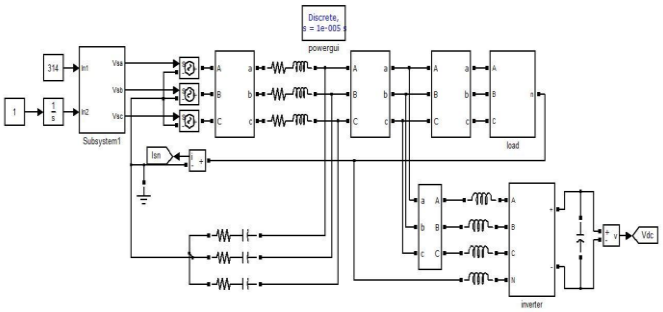

Fig.2.6 Simulink model for non-iterative optimized algorithm

2.4 Performance of DSTATCOM under HF mode:

DSTATCOM under HF mode. The dynamic performance of DSTATCOM with PCC voltages (V_{Sabc}), load current (I_{Labc}), compensation current (I_{Cabc}), source current (I_{Sabc}), DC bus voltage (v_{dc}). Under HF mode the source current wave form should be almost sine wave and the THD values are according to standards.

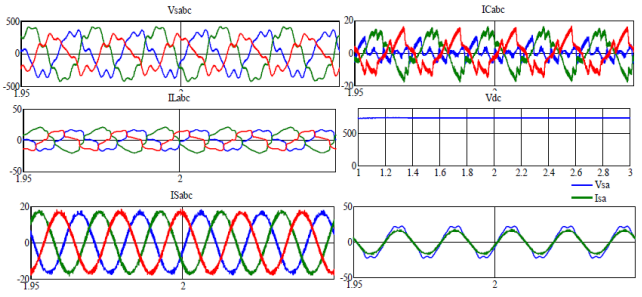

Fig.2.7 Waveforms under HF mode

The THD of source current under HF mode are 2.77%, 2.96%, 2.93% for phases a, b and c. in this mode specified values of THD for odd and even harmonics are zero to maintain the source current waveform as sinusoidal.

2.5 Performance of DSTATCOM under UPF mode:

Fig5.9 shows the response of DSTATCOM under UPF mode. The dynamic performance of DSTATCOM with PCC voltages (V_{Sabc}), load current (I_{Labc}), compensation current (I_{Cabc}), source current (I_{Sabc}), DC bus voltage (v_{dc}). In this mode the source current wave form should be same as PCC source voltage to maintain to the power factor unity. To achieve this we have to add the same amount of harmonics to source current which are present in the source voltage and specified values of THD's are unity to get unity power factor. The THD of source current under UPF mode are 9.13%, 8.11%, 8.12% for phases a, b and c. The source current waveform should be same as source voltage waveform to maintain power factor as unity.

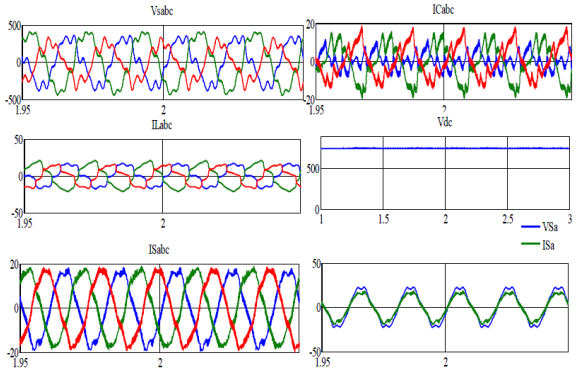

Fig.2.8 Waveforms under UPF mode

III. SIMULATION RESULTS:

In simple peak detection control algorithm under two different modes the THD values for the voltage at the point of common coupling, source current and load currents are shown below for without compensation.

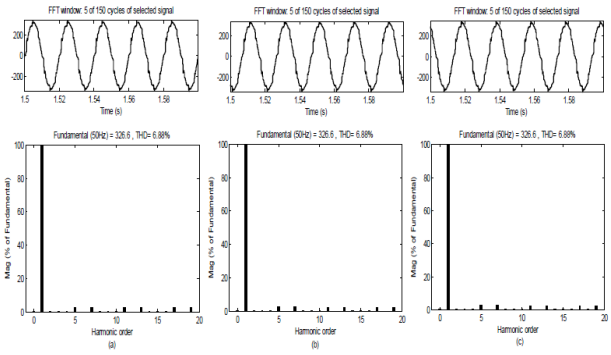

Fig.3.1

(a) Phase a voltage at the PCC (b) Phase b voltage at the PCC (c) Phase c voltage at the PCC

The above shown waveforms are for voltage at PCC. The THD values are very high because of the presence unbalance and non-linearity in the load. The THD of phase 'a", is 6.88%, the THD of phase 'b", is 6.88%, the THD of phase 'c" is 6.88%, where THDs of PCC voltages are not under the limit of IEEE-519 standard. These three phase voltage values are reduced because of the load. We can improve the THD and performance by injecting the harmonic currents and reactive power into the system by using DSTATCOM

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
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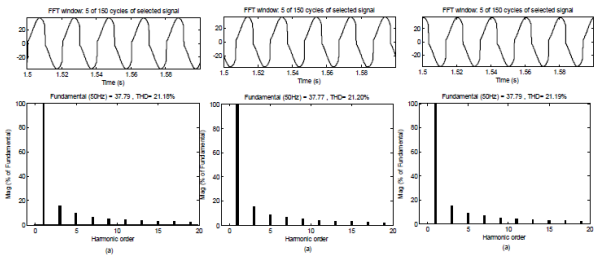

Fig.3.2

(a) Phase ‘a‟ load current. (b) Phase ‘b‟ load current. (c) Phase ‘c‟**.** The above shown waveforms are current waveforms. The load current and source current values are same because there is no compensation. The THD values are very high because of the presence unbalance and non-linearity in the load. The THD of phase ‘a‟, is 16.30%, the THD of phase ‘b‟, is 16.30%, the THD of phase ‘c‟ is 16.31%, where THDs source and load currents are not under the limit of IEEE-519 standard. We can improve the THD of source current by injecting the harmonic currents into the system by using DSTATCOM. The performance of DSTATCOM using peak detection control algorithm is simulated using developed MATLAB model for PFC and ZVR modes of operation under linear and non-linear loads. Fig 6.3 shows the response of DSTACOM for reactive power compensation under lagging power factor in PFC mode. The THD at PCC voltage of phase „a‟ is 1.34%, 1.28% for phase „b‟ and 1.36% for phase „c‟. These results provide satisfactory performance of DSTATCOM for load balancing and harmonic elimination according to IEEE-519 standard Guidelines

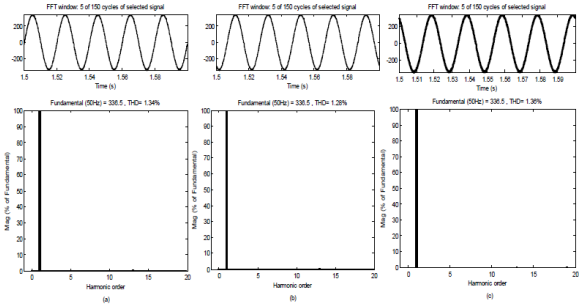

Fig.3.3(a) Phase ‘a’ voltage at PCC. (b) Phase ‘b’ voltage at PCC. (c) Phase ‘c’ voltage at PCC.

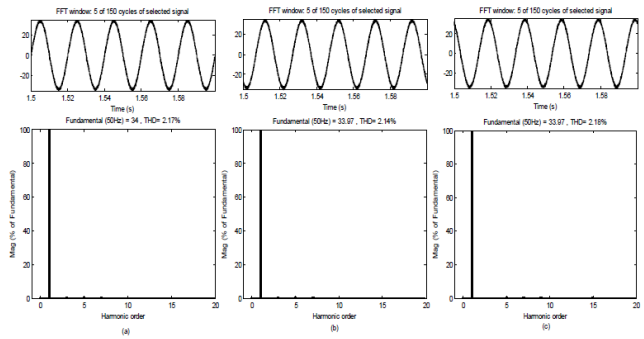

Fig 3.4 (a) Phase ‘a’ source current. (b) Phase ‘b‟ source current. (c) Phase ‘c‟ source current

Fig 3.4 shows the response of DSTACOM for reactive power compensation under lagging power factor in PFC mode. The THD of phase ‘a’ source current is 2.17%, 2.14% for phase ‘b’ and 2.18% for phase ‘c’. These results provide satisfactory performance of DSTATCOM for load balancing and harmonic elimination according to IEEE-519 standard guidelines.

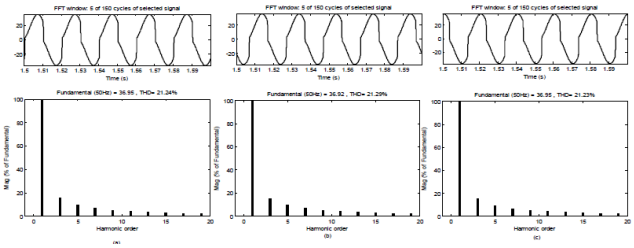

Fig 3.5 (a) Phase ‘a’ load current. (b) Phase ‘b’ load current. (c) Phase ‘c’ load current.

Fig 3.5 shows the response of DSTACOM for reactive power compensation under lagging power factor in PFC mode. The THD of phase ‘a‟ load current is 21.24%, 21.29% for phase ‘b‟ and 21.23% for phase ‘c‟ These results provide satisfactory performance of DSTATCOM for load balancing and harmonic elimination according to IEEE-519 standard Guidelines

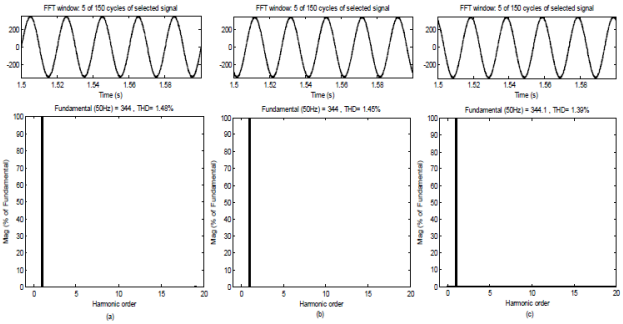

Fig 3.6 (a) Phase ‘a’ voltage at PCC.
(b) Phase ‘b’ voltage at PCC
(c) Phase ‘c’ voltage at PCC.

Fig 3.6 shows the response of DSTACOM for reactive power compensation under lagging power factor in ZVR mode. The THD at PCC voltage of phase ‘a‟ is 1.34%, 1.28% for phase ‘b‟ and 1.36% for phase ‘c‟. The DSTATCOM supplies some extra lading reactive power components in addition t load reactive power demand in ZVR mode. This extra leading reactive power is required to regulate PCC voltage up to desired level.

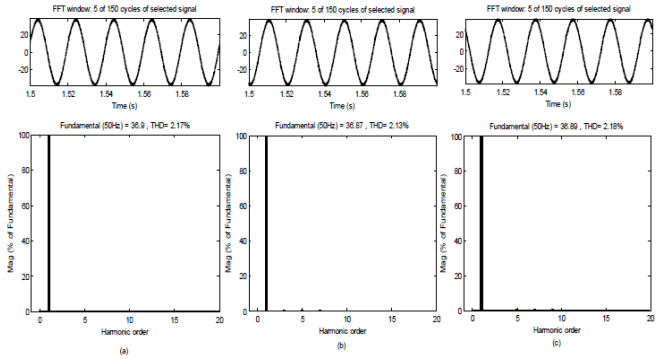

Fig 3.7 (a) Phase ‘a’ source current..
(b) Phase ‘b’ source current.
(c) Phase ‘c’ source current.

Fig 3.7 shows the response of DSTACOM for reactive power compensation under lagging power factor in ZVR mode. The THD of phase ‘a’ source current is 2.17%, 2.13% for phase ‘b’ and 2.18% for phase ‘c’ where supply currents are leading compared with PCC voltage. These results provide satisfactory performance of DSTATCOM for load balancing and harmonic elimination according to IEEE-519 standard guidelines.

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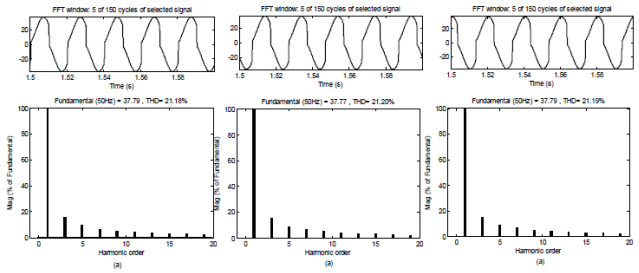

Fig 3.8 (a) Phase 'a' load current.
(b) Phase 'b' load current.
(c) Phase 'c' load current.

Fig 3.8 shows the response of DSTACOM for reactive power compensation under lagging power factor in PFC mode. The THD of phase 'a' load current is 21.18%, 21.27% for phase 'b' and 21.19% for phase 'c' These results provide satisfactory performance of DSTATCOM for load balancing and harmonic elimination according to IEEE-519 standard guidelines. In PFC mode as said in the above chapter by regulating the DC link voltage by using PI controller and by injecting required amount of harmonics by using DSTATCOM we can improve the performance of the system.. As we already shown the power factor become unity in this mode, and also we can improve the THD of the voltage at the point of common coupling, source current, load current. In ZVR mode as said in the above chapter by regulating the voltage at the point of common coupling by using PI controller and by injecting required amount of reactive power by using DSTATCOM we can improve the performance of the system.. As we already shown the power factor become leading in this mode, and also we can improve the THD of the voltage at the point of common coupling, source current, load current.

Quantity		Without compensation		PEC Mode of Operation		ZVR Mode of Operation	
^{v}sa	Mag.	231.5		235.1		239.8	
	THD	6.88%		1.34%		1.34%	
^{v}sb	Mag.	231.4		234.9		239.7	
	THD	6.88%		1.28%		1.28%	
^{v}sc	Mag.	230.8		234.9		239.8	
	THD	6.88%		1.36%		1.36%	
^{i}sa	Mag.	23.46		24.08		26.25	
	THD	16.30%		2.17%		2.17%	
^{i}sb	Mag.	25.63		24.09		26.19	
	THD	16.30%		2.14%		2.13%	
^{i}sc	Mag.	25.63		24.1		26.16	
	THD	16.31%		2.18%		2.18%	
^{i}la	Mag.	23.46		23.61		24.08	
	THD	16.30%		21.24%		21.18%	
^{i}lb	Mag.	25.63		25.8		26.27	
	THD	16.30%		21.24%		21.27%	
^{i}lc	Mag.	25.63		25.81		26.28	
	THD	16.31%		21.23%		21.29%	
^{i}Ln	^{i}sn	2.149	2.149	2.214	0.029	2.188	0.01615

Table.3.1: THD"s of voltage's and current's under PFC and ZVR modes of operation

The above table shows RMS values and THD values of voltage at PCC, source current and load current under without compensation, PFC and ZVR modes of operation. There are two different modes in Non-iterative optimized algorithm. In HF mode the source current waveform is almost sinusoidal and the THD values are also under IEEE-519 standard. In UPF mode the source current waveform is almost same as the voltage at the PCC to make the power factor unity. The obtained THD values are shown below for two different modes.

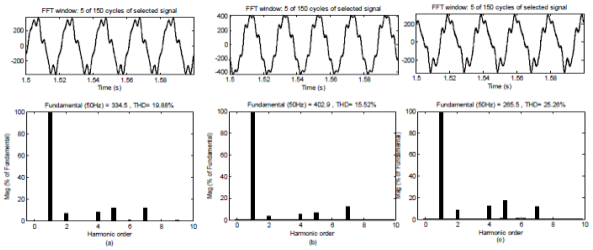

Fig 3.9 (a) Phase 'a' voltage at PCC.
(b) Phase 'b' voltage at PCC
(c) Phase 'c' voltage at PCC.

The above shown waveforms are under HF mode. The THD values of the voltages at PCC are very high because the supply voltage is unbalanced and distorted. The THD of phase 'a' voltage is 19.88%, 15.52% for 'b' phase and 25.26 for phase 'c'

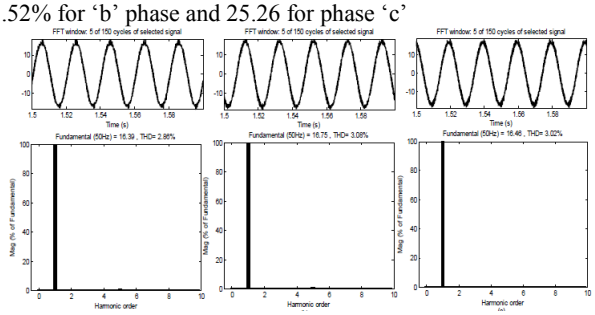

Fig 3.10 (a) Phase 'a' source current.
(b) Phase 'b' source current.
(c) Phase 'c' source current.

The above shown waveforms are under HF mode. In HF mode it eliminates the harmonic current from the source current and makes it sinusoidal. The THD values of phase 'a" source current is 2.86%, 3.08% for phase 'b" and 3.02% for phase 'c", it shows that all the above mentioned THD values are under IEEE standards and the performance is satisfactory.

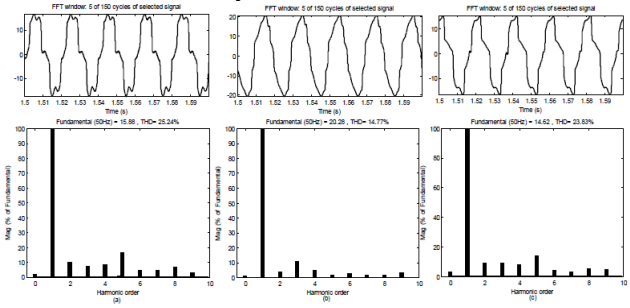

Fig3.11 (a) Phase 'a' load current
(b) Phase 'b' load current.
(c) Phase 'c' load current

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 5 Issue 01, January-2016

The above shown waveforms are under HF mode. The THD values of phase 'a" load current is 25.24%, 14.77% for phase 'b" and 23.83% for phase 'c". In UPF mode the source current waveform is almost similar to source voltage. To obtain this unity power factor we have to inject the same amount of harmonics which are present in the source voltage.

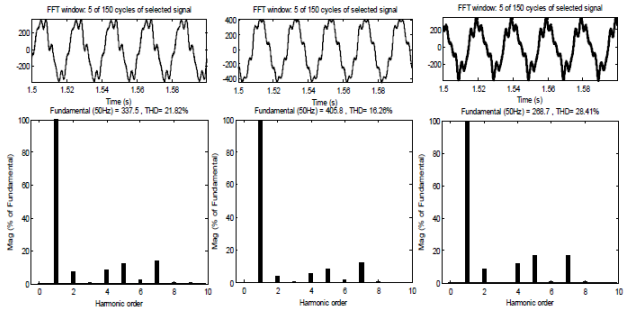

Fig 3.12 (a) Phase 'a' voltage at PCC.
(b) Phase 'b' voltage at PCC
(c) Phase 'c' voltage at PCC.

The above shown waveforms are under UPF mode. The THD values of the voltages at PCC are very high because the supply voltage is unbalanced and distorted. The THD of phase 'a' voltage is 21.82%, 16.26% for 'b' phase and 28.41% for phase 'c'.

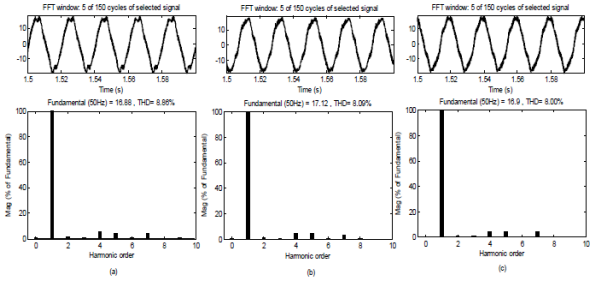

Fig 3.13 (a) Phase 'a' source current.
(b) Phase 'b' source current.
(c) Phase 'c' source current

The above shown waveforms are under UPF mode. It will not reduce the harmonics completely but it makes power factor unity. The THD values of phase 'a' source current is 8.36%, 8.09% for phase 'b' and 8.00% for phase 'c', it shows that all the above mentioned THD values are under IEEE standards and the performance is satisfactory.

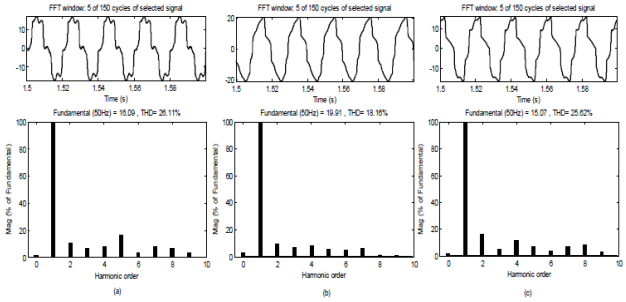

Fig3.14 (a) Phase 'a" load current
(b) Phase 'b" load current.
(c) Phase 'c" load current

Table.3.2: THD's of voltage's and current's under HF and UPF modes of operation

Quantity		Harmonic free method	Unity power factor method
^{v}sa	Mag.	*239.6*	*239.6*
	THD	*10.57%*	*10.57%*
^{v}sb	Mag.	*287.5*	*287.5*
	THD	*7.63%*	*7.63%*
^{v}sc	Mag.	*191.6*	*191.6*
	THD	*13.92%*	*13.92%*
^{i}sa	Mag.	*11.56*	*11.92*
	THD	*2.77%*	*9.13%*
^{i}sb	Mag.	*11.82*	*12.09*
	THD	*2.96%*	*8.41%*
^{i}sc	Mag.	*11.63*	*11.93*
	THD	*2.93%*	*8.12%*
^{i}la	Mag.	*11.23*	*11.37*
	THD	*25.22%*	*26.04%*
^{i}lb	Mag.	*14.36*	*14.09*
	THD	*14.85%*	*18.02%*
^{i}lc	Mag.	*10.32*	*10.65*
	THD	*24.09%*	*25.84%*

From the above shown table we can conclude that the THD's are under IEEE standards and the performance is quite satisfactory.

IV CONCLUSION

A peak detection control algorithm of DSTATCOM has been implemented for the load compensation in a three-phase four-wire distribution system. It has been used for extraction of fundamental active power and reactive power components of load currents. These load current components have been used for estimation of reference supply currents with DC bus voltage control of DSTATCOM. The performance of DSTATCOM has been found quite satisfactory for load balancing, reactive power compensation and harmonics elimination under limit of IEEE-519 and IEC-61000 standards. Proposed control algorithm of DSTATCOM has been found satisfactory under dynamic and steady-state conditions even small change in loads. The DC bus voltage of the DSTATCOM has also been regulated to desired value under varying load conditions. A single-step non-iterative optimized control algorithm has been proposed for a 3 phase 4 wire shunt APF to achieve an optimum performance between power factor and THD. The proposed optimized approach is simple to implement and does not require complex iterative optimization techniques to determine the conductance factors. It is shown mathematically that only three conductance factors (one for the fundamental harmonic and two other for odd and even harmonics) are sufficient to determine the desired reference source currents. The proposed algorithm determines the conductance factors in 10 μs. Because of the smaller computational time, the proposed algorithm performs satisfactorily under dynamically changing load conditions.

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 5 Issue 01, January-2016

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