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CS-CMOS: A Low Noise Logic Family for Mixed Signal Integrated Circuits

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***Abstract*—In low-power CMOS logic circuits operated from a fixed supply voltage can result in uncontrolled conduction over process and temperature variation. The large current-pulses flowing during the logic transitions also cause power-supply noise. Managing the switching-noise in mixed-signal systems fabricated on a single chip is becoming increasingly challenging. Here we introduce a new logic family called CS-CMOS (Current Steering-CMOS) which is obtained by a simple current steering modification to the core CMOS structure. This is a low-noise logic family, so its main application is in the field of mixed signal system-on-chips (SoCs). Existing logic families that minimize the switching-noise generation such as current-steering logic (CSL), current-balanced logic (CBL) etc. require considerably more power than traditional CMOS implementations. But all of these logics reduces switching noise and also improves the switching speed compared to conventional CMOS logic. The current steered CMOS gates (CSCMOS) are specially targeted for use in low-power, wide dynamic range mixed-signal applications where supply noise must be minimized. Analysis for different parameters like power consumption, delay and noise generated are done in cadence using different technologies and compared its performance. Circuit operation and simulation results are presented.**

***Keywords*—Current-balanced logic (CBL), current steering logic (CSL),current-steering CMOS (CS-CMOS), mixed signal system-on-chip (SoC), power supply noise.**

I. INTRODUCTION

VLSI systems-on-chips (SoCs) use CMOS digital logic circuits because they consume very low power, also have high packing density and are easy to design [1]. Most of the power consumed by CMOS gates is due to displacement currents(Iswitching) and overlap current(Isc)[4] during the state transition at the input of the digital circuitry. Displacement current drawn during state-transitions for charging and discharging wire and device capacitances. Fig. l(a) shows displacement and overlap currents that flow into the static CMOS inverter of fig. l(b). Overlap current(Isc) flows when combinations of NMOS and PMOS devices are turned on resulting in a direct path from Vdd to GND. These current spikes increase linearly with the operating frequency and flow
through the power supply wires, ground lines, parasitic inductance and capacitances causing ringing and voltage drop.

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This is the dominant source of substrate noise [5]. However, due to digital switching noise that adversely affects sensitive analog circuitry via substrate coupling, it is difficult to realize high resolution analog circuits on the same substrate with complex digital circuitry[2]. Typical examples are systems that have analog filters, sample and hold, high-resolution ADC and DAC sharing the same substrate, combinatorial and sequential circuits like in a DSP[3].

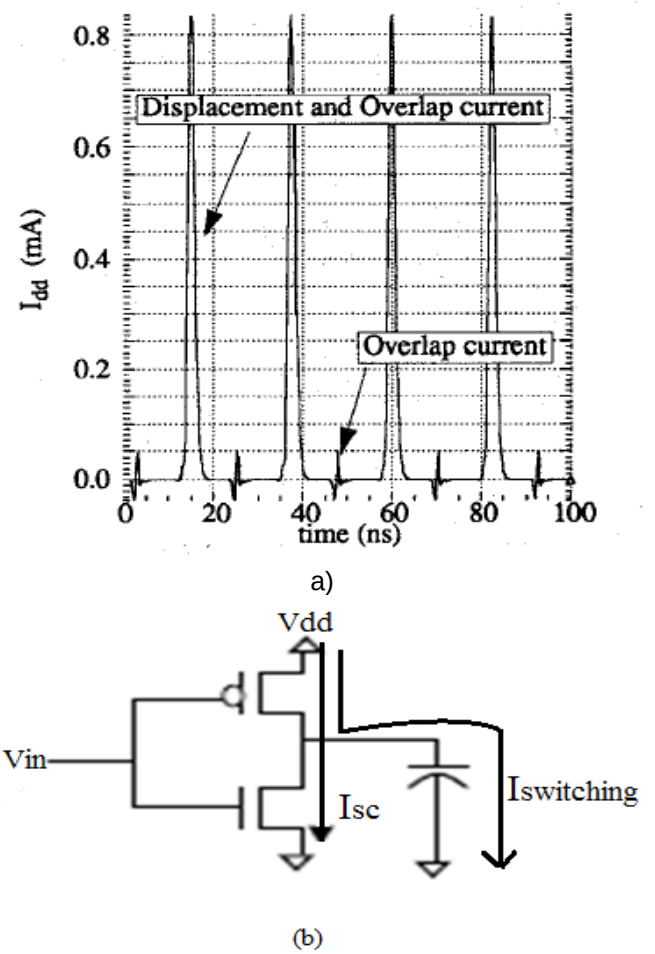

Fig. 1: (a)Displacement current (Iswitching) and overlap current (Isc) that flow into(b) nwell static CMOS inverter

The problem of switching noise is dealt in three parts. They are noise generation, its propagation through the substrate, and injection into analog circuits [5]. The focus here is to minimize the generation of switching noise and keeping the impulse current local to where it is generated [7].

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Among the existing logic families that use this approach are current steering logic (CSL) [4] and current balanced logic (CBL) [6]. Both of these families reduce noise because they draw a constant-current from the supply. But the power consumed is at least 10 times higher than the equivalent CMOS implementation[6]. Differential current mode logic is useful at higher frequencies because of its reduced output voltage swing and power dissipation [9]. Its use is limited because for operating at very low currents it needs a large resistance. Here a new logic family called the current-steering CMOS logic (CS-CMOS) is proposed for mixed-signal applications. The transfer characteristic of the CS-CMOS inverter is discussed in detail. Its low noise properties are compared with those of CSL and CBL and also with the conventional CMOS logic are done.

II. LOW NOISE FAMILY MEMBERS

A. Current-Steering Logic(CSL):

CMOS current steering logic (CSL) has been developed for applications in high-precision mixed-signal integrated circuits. CSL has several interesting features are its operation and performance are nearly independent of the supply voltage. By using a current source, as shown in Fig. 2, the supply current IDD is ideally constant.

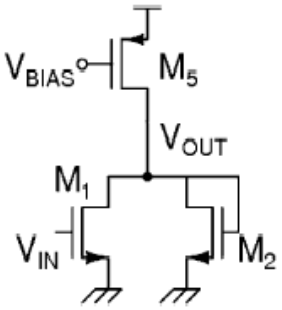

Fig. 2: CSL Logic

At high operating frequencies, CSL circuits may dissipate high power and have lower device count than static CMOS, and higher speeds are achieved using smaller feature sizes for a given bias current. Process variations can be calibrated by adjusting the bias current, and the noise current spikes generated during a state transition are as much as two orders of magnitude smaller than in CMOS static circuits. The low noise characteristic is especially noteworthy in that it allows for a reduction in digital switching noise interference of the sensitive analog circuitry in high-speed, high-precision mixed signal applications.

B. Current Balancing Logic(CBL):

CBL can achieve ideally constant supply current by using a different principle. They may be regarded as pseudo-NMOS circuits [3], [4] to which transistor M3 has been added. The objective is that, during logic transitions, the variation of i_{D3} compensates (or balances and, hence, the designation current balanced logic) the variation of i_{D3}. We find that perfect compensation can be obtained, thus making $i_{D2} + i_{D3} = I_{DD}$ constant as shown in (Fig. 3(b)), if transistors M2 and M3 are matched.

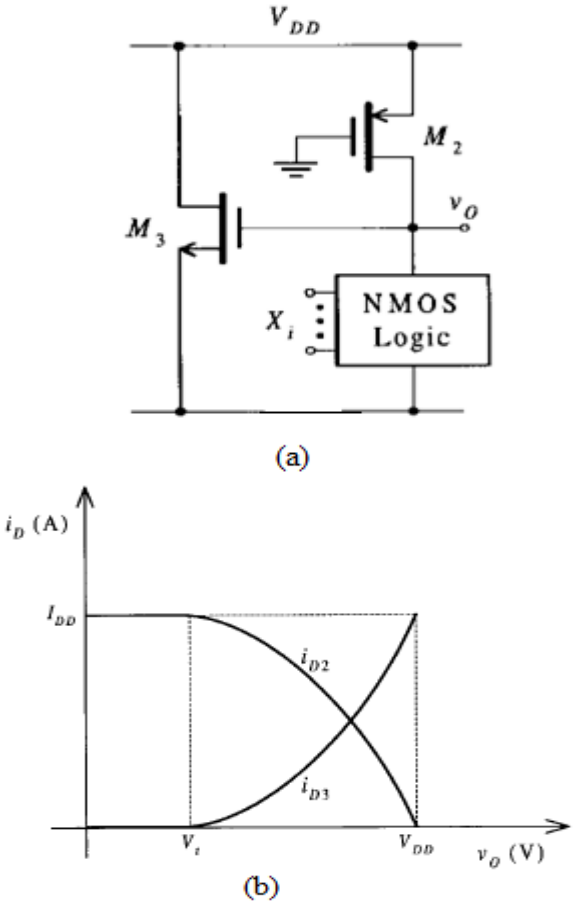

Fig. 3: (a) CBL Logic (b)Current balancing in CBL gate

III. PROPOSED SYSTEM: CS-CMOS LOGIC

CS-CMOS is obtained by a simple current-steering modification to the standard CMOS family. As in a CMOS inverter, a pair of complimentary transistors (M1,M2) connected in series forms the core of the proposed CS-CMOS inverter, as shown in Fig. 4. Since CMOS gates do not draw any appreciable current in their static states, constant-current operation requires additional paths for the d-c bias current to flow. A pair of complimentary transistors (M3,M4) is added in parallel for this purpose. A P-channel transistor (M5) sources a constant current I_B to each gate.

A. Operation of CS-CMOS

The current steering is accomplished by the single-ended output-voltage of the inverter which controls the gate-voltages of M3 and M4 operating in parallel. The reason for steering the current using the output terminal of the inverter rather than its input is that digital gates can have multiple-inputs but only a single-output. Thus the idea of the output of the gate steering the bias current is readily extended to all types of gates in a

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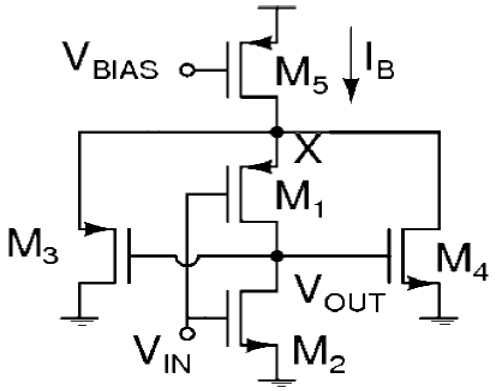

Fig. 4: Current steered CMOS Inverter (CS-CMOS)

straight forward manner. Since only the sub-threshold current of a switched-OFF device flows in the inverter in either static states, the logic output levels (HIGH and LOW) remain like in a standard CMOS gate. Note that the current source I_B shown as ideal in Fig. 4, is realized using a P-channel current-mirror. Thus the supply voltage V_{DD} is required will be greater than Vx to keep the transistor used to implement in saturation.

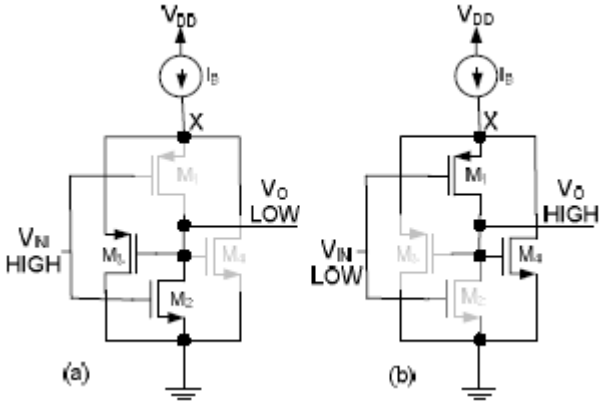

Fig. 5: Circuit diagram of the CS-CMOS inverter,(a)when V_{IN} is high and (b) when V_{IN} is low

When the input V_{IN} is HIGH (Fig.5a), the transistor M1 of the inverter is OFF, M2 is conducting and the output voltage V_o is LOW. Hence M4 is OFF and the P-channel transistor M3 is conducting the bias current I_B. Note that M3 is diode connected in this state. When the input goes LOW (Fig. 5b) the transistor M2 cuts OFF and M1 pulls the output node HIGH. This causes the N-channel transistor M4 to turn ON and it gets diode-connected. Now M3 cuts OFF and the current I_B gets steered from M3 to M4. The voltage V_X at the node X can be kept almost constant in both the static states of the inverter by the appropriate choice of the aspect ratios of M3 and M4. $V_X = (V_{ON3} + V_{T3})$ and $(V_{ON4}+V_{T4})$ in the input LOW and HIGH states respectively. It should be pointed out that during the transitions the N-channel transistors M2 and M4 with their sources grounded operate in common-source configuration whereas the P-channel transistors M1 and M3 with their sources coupled and fed by the current source I_B operate like a differential pair. If we consider M2 as an active load of this differential pair, it is easy to identify the circuit as a Schmitt trigger containing positive feedback via the output and the node X. This causes the well known hysteresis in the transfer characteristics of the inverter.

TABLE I: DEVICE DIMENSIONS FOR CS-CMOS, CSL AND CBL IN 180nm TECHNOLOGY

DEVICE	CS-CMOS W m/L m	CSL W m/L m	CBL W m/L m
M1	2/0.3	2/0.18	0.42/0.18
M2	1/0.25	0.42/0.18	0.42/5
M3	0.42/0.18	-	-
M4	0.42/0.18	-	-
M5	1/0.36	1/0.36	0.42/0.18

It is clear that, if V x > V T 1 + V T 2, the inverter is biased like a regular CMOS circuit in which there will be an input voltage range in which both M1 and M2 will conduct. For V x < V T 1 + V T 2, when V_{IN} increases from LOW to HIGH, M1 will shut OFF before M2 turns ON and for decreasing VIN , M2 will shut OFF before M1 turns ON. This choice will result in hysteresis as well as increased propagation delay. The ideal choice is to make Vx = VT1+VT2 where the complementary devices turn ON and OFF simultaneously. For a given set of threshold voltages this condition can be met by proper choice of device dimensions. Such a choice is shown in Table I.

IV. SIMULATION RESULTS

In CS-CMOS logic, the circuit configuration reduced the switching noise and propagation delay than CMOS. The switching noise is reduced by applying a constant current drawn from the current source (here M5 act as constant current source) which is placed between supply voltage and logic circuitry. Hence we minimize the output current spikes which is higher in conventional CMOS circuitry. The other low noise members like CSL and CBL have also very low switching noise and almost similar power consumption as that of CS-CMOS. But the area and power consumption is more compared with the standard CMOS logic. Analysis for different parameters like power consumption, delay and noise generated are done in cadence using different technologies like 180, 90 and 45nm and compared its performance.

TABLE II: POWER ANALYSIS DONE IN DIFERENT TECHNOLOGIES

LOGIC	180nm	90nm	45nm
CMOS	614.7nW	91.04nW	6.205nW
CS-CMOS	104.9 W	26.67 W	127.7nW
CSL	125.1 W	38.67 W	364nW
CBL	482.8 W	315.4 W	6.806 W

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TABLE III: DELAY ANALYSIS DONE IN DIFERENT TECHNOLOGIES

LOGIC	180nm	90nm	45nm
CMOS	20.01ns	69.6ps	15.505ps
CS-CMOS	10ns	49.76ps	9.18ps
CSL	10.002ns	19.01ps	3.960ps
CBL	48.695ps	12.022ps	1.47ps

The table II and III shows the power and delay analysis done in 180, 90 and 45nm technologies in CADENCE Tool. The dynamic power consumption is calculated in table II. Here we can see that the power consumed in CMOS circuitries less than that of CS-CMOS logic. But when consider the low noise family members, we can notice that CS-CMOS has less power consumption than CSL and CBL logic. Also we can see that the propagation delay is much reduced in low noise logic family members. Hence the switching speed is considerably increased. The comparison between CMOS, CSL and CBL with that of CS-CMOS logic for power consumption and propagation delay are tabulated here. And also presented the graph showing propagation delay and optimised Power-Delay product are plotted against bias current.

The noise analysis done by plotting the graph between power spectral density and some range of frequencies. Here we used the frequency range from .1 Hz to 100 GHz. From the noise response we calculated the corresponding noise at 1 MHz frequency for different logic circuitries. Noise analysis done is shown in table IV.

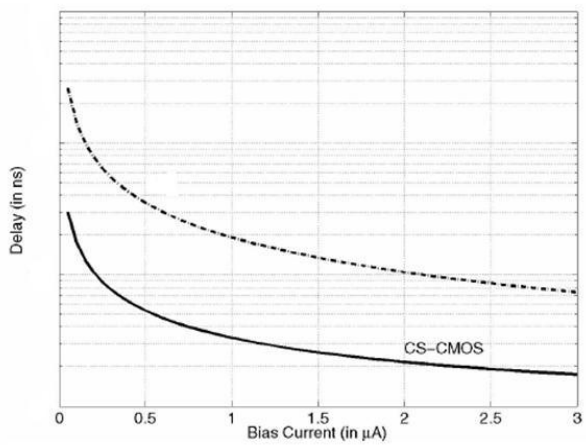

Fig. 7: Delay Analysis of CS-CMOS and CMOS Inverters in 180nm Technology

It can be clearly observed from the fig:7 and 8 that CS-CMOS is better than CSL, CBL and CMOS in speed and Power Delay Product by almost an order of magnitude. Since the key objective was to minimize switching noise, the peak-to-peak current variation in the power supply for CMOS & CS-CMOS

TABLE IV: NOISE ANALYSIS DONE IN DIFERENT TECHNOLOGIES

LOGIC	180nm(V^2/Hz)	90nm(V^2/Hz)	45nm(V^2/Hz)
CS-CMOS	1.812f	2.378f	79.142f
CSL	1.909f	2.844f	82.77f
CMOS	43.768a	57.077a	163.99a

are compared for the same average current drawn by the circuits. Comparison of the peak to peak ripple in the power supply current for CMOS and CS-CMOS are shown in figure 8. If we balance the power consumption and delay of the CS-CMOS logic by proper switching and sizing, we achieved a better and optimized power-delay product.

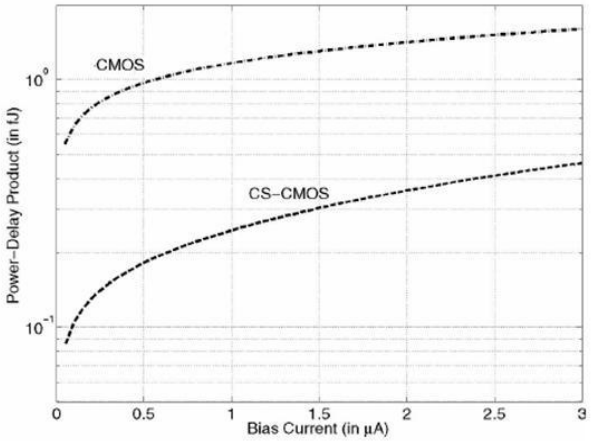

Fig. 8: Comparison of Power-Delay Product of CMOS and CS-CMOS as a function of bias current in 180nm Technology

V. CONCLUSION

A new current steering logic family namely CS-CMOS is described which is obtained by a minimal modification to the standard CMOS logic. The constant-current operation enables a substantial reduction of switching noise. The simulation results and corresponding graphs are demonstrated for the propagation delay, power and noise advantages of this family over previously proposed low noise logic families namely CSL and CBL. And also done a comparison between the conventional CMOS logic with CS-CMOS. However, the circuit configuration improves switching speed around the logical threshold by introducing positive feedback. The logic levels is controlled by the bias current flowing through a diode connected transistor having a higher threshold voltage. The switching speeds and its noise reduction are better than any other logic. This family is suitable for use in low-noise mixed-signal integrated circuits.

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