International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 2 Issue 1, January- 2013

CURRENT MODELING OF INDEPENDENT DOUBLE GATE FINFET

G.SAMBASIVA RAO (ASSISTANT PROFESSOR)
Y.PHANI KUMAR (ASSISTANT PROFESSOR)
ASIST, PARITALA

ABSTRACT

The scaling of the Mosfets played an important role to have better control of the flow of electrons in a channel of field-effect transistors (FETs) did lead to the design of two gates in junction field-effect transistors, field plates in a variety of metal semiconductor field-effect transistors and high electron mobility transistors, and finally a gate wrapping around three sides of a narrow fin-shaped channel in a FinFET.With the enhanced control, performance trends of all FETs are still challenged by carrier mobility dependence on the strengths of the electrical field along the channel. Moreover, the inherent non-planar nature of a FinFET demands independent double gate FinFET modeling for accurate analysis of the device performance. Using the Silvaco modeling tool with We demonstrated that 3D modeling produces more accurate results. As 3D modeling results came close to experimental measurements taking several values of gate voltage and shown that the dual-gate FinFET has reduced the required size carrying higher transconductance than the single-gate device.

IJERT

1. INTRODUCTION

MOSFETs (Metal Oxide Semiconductor Field-Effect Transistors) have existed since the beginning of the 1960's, and are still, the most important type of transistor in the world. No other types of technology have yet been able to compete with the well known MOSFET technology. The worlds request for faster and smaller electronics has put an enormous pressure on the semiconductor industry to keep shrinking the transistor, especially since smaller also means faster and more logic on chip. However, the scaling of conventional single-gate MOSFETs is approaching the practical limits such as leakage and loss of gate control. With the scaling of the channel length below 50nm complex channel profiles are required to achieve desired threshold voltages and to eliminate short channel effects. In bulk MOSFETs, bulk doping concentration need to be increased to suppress the short channel effects; this degrades mobility, worsens subthreshold swing and increases the parasitic junction capacitance [1]. Essentially, the short channel effects reflect the extent of drain bias influence on the channel potential. The search for alternative devices is for this reason extremely important in order to keep up the development in the semiconductor industry. Strong candidates to replace the conventional bulk MOSFET is the FinFET ("Fin"FET). The replacement is needed in order to meet the ever growing demands for high-speed, low power CMOS (Complementary Metal Oxide Semiconductor) circuitry.

Alternative device structures based on silicon-on-insulator (SOI) technology have emerged as an effective means of extending MOS scaling beyond bulk limits for mainstream high-performance or low-power applications. Partially depleted (PD) SOI was the first SOI technology introduced for high-performance microprocessor applications. The ultra-thin-body fully depleted (FD)SOI and the non-planar FinFET device structures promise to be the potential "future" technology/device choices The scaling of the single-gate MOSFET into the sub-100nm range has been possible by for instance increasing the doping in the body and by using steep doping gradients. However, this will be detrimental for the charge carrier mobility, and thus lower the drain current and speed of the transistor. The FinFET has advantages compared to the bulk MOSFET in terms of short-channel effects and much improved gate control due to the use of volume inversion in the entire thin, lightly doped silicon body in all regimes of operation. The FinFET become superior to the ordinary MOSFET at short gate lengths for this reason.

2. MOSFET Scaling

Among the technologies that have changed the world and people's daily life in the past half century, integrated circuit (IC) technology played most important role. In the past five decades, the IC developed from small scale IC (SSI), medium scale IC (MSI), large scale IC (LSI), finally to very-large scale IC (VLSI) or ultra-large scale IC (ULSI). The number of components per chip also rises from only several transistors in the first IC to typically several hundred millions in today's advanced microprocessors. Predicted by the well-known Moore's law [2], which was first mentioned in the 1965's speech, the numbers of components per chip will double every 18 to 24 months. Concurrent with the increasing complication of IC, is the miniaturization of the individual components, which are mainly the MOSFETs. The gate length of MOSFET shrunk from more than ten microns in the early 1960s to ~35nanometers in today's most advanced 45nm technology. The industry as well as the research community uses "MOSFET scaling" to call this shrinkage of MOSFET size, which is believed to be one of the driving forces of VLSI technology. In the following part, the historical development of MOSFET and future scaling trend will be reviewed.

2.1 The reason for MOSFET scaling and difficulties

It was 13 years after the Bell Lab invention of bipolar junction transistor (BJT) that the first MOSFET was proposed and fabricated using a thermally oxidized silicon structure [3]. Despite the big success that BJT has already achieved, MOSFET was quickly adopted in the IC application. The superiority of MOSFET over BJT consists of several aspects. Similar to increasing the integration level of IC, scaling down the size of MOSFET is very important in lowering the cost and improving the performance. MOSFET scaling has been the driving force of the booming semiconductor industry and benefits both manufacturers and consumers.

Reducing the length of the channel, which is controlled by gate voltage and acts as a current switch between source and drain, is mostly mentioned in the scaling of MOSFET. Channel length is the same as the gate length because of the self-alignment poly-silicon gate (Si) process. It is easy to comprehend that shorter gate length will result in faster switching speed because less time is needed for carriers to flow from the source to the drain. However, short gate length will bring other undesirable effects such as threshold voltage roll-off, flattened sub-threshold slope, increased leakage current and drain-induced barrier lowering (DIBL). All these effects are categorized as short-channel effects (SCE), which is the main obstacle during MOSFET scaling. The scaling approach said that both lateral and vertical dimensions of the transistor need to be reduced by the same scaling factor in order to avoid the SCE when fabricating smaller device, and by the same scaling factor, the supply voltage is reduced and the substrate doping concentration is increased.

Until the late 1990s, the IC industry enjoyed the improvement of circuit performance due to the MOSFET scaling. As the gate length scaled into the deep-submicron regime from the late 1990s to the present day, scaling has become increasingly difficult and the benefits of scaling are not as evident as before. SCE is the main reason that retards the improvement of IC performance during MOSFET scaling. In order to alleviate the high off-state current and threshold voltage roll-off, the substrate doping concentration needs to be increased. However, high doping concentration degrades the carrier mobility as well as increases the junction capacitance. Very thin gate oxide is also needed to suppress the SCE. But when the gate oxide thickness is at the order of several nanometers, the tunneling current increases exponentially, which increases the stand-by power further. Although the semiconductor industry is still working hard to push the scaling further using conventional bulk CMOS device, new structures and non-classical CMOS devices inevitably come into the horizon as the semiconductor industry and technology itself needs to gain new force to go further ahead. The non-classic CMOS devices mainly include SOI and DG MOSFET.

2.2 Non-classical CMOS devices

Figure 1.1 is the schematic cross-section of an SOI device, where it can be observed that the active layer of SOI is electrically isolated from the substrate. Regarding SCE, the SOI material has several advantages compared to bulk silicon material. Firstly, buried oxide (BOX) cuts off most of the leakage current path for a MOSFET fabricated on it, which is extremely useful as the leakage current of scaled bulk MOSFETs increases dramatically. The small drain junction area also reduces drain

IJERT

voltage penetration to the channel region and hence reduces the threshold voltage roll-off due to DIBL. Small source and drain junction area also largely reduces the source/drain junction capacitance, which is favorable to increase the circuit operation frequency.

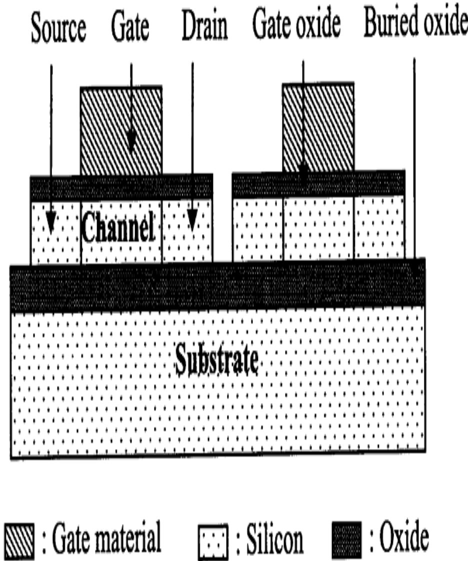

Figure 1.1 Schematic cross-section of an SOI device

Another alternative for pushing the CMOS scaling forward is DG CMOS, as illustrated in Figure 1.2. Compared to SOI MOSFET, DG MOSFET has mainly two advantages. Because of the extremely good control of silicon body potential when both the top and the bottom gate voltages are applied, significant improvement of threshold roll-off. Secondly, it was found that the carriers are not just confined at the top and bottom silicon interface of a DG MOSFET with sufficiently thin silicon body. Because of the coupling between the two gates, the carrier is induced not just at the interface, which is called "volume inversion". This in particular provides the device with enhanced trans-conductance performances, since inverted carriers within the volume of the silicon undergoes less scattering than those at the silicon surface [4].

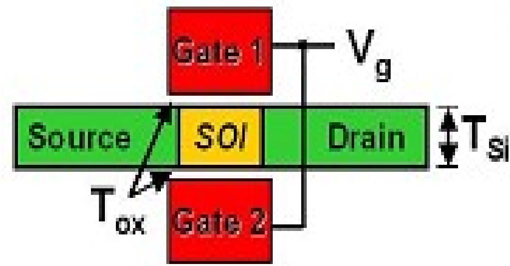

Figure 1.2 Structure of DG MOSFET

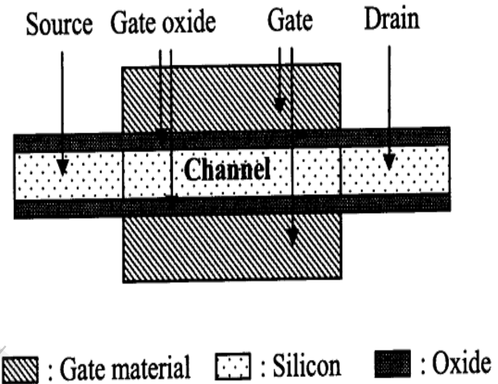

Figure 1.3 Schematic Illustrations of a DG MOSFET cross-section

IJERT

2.3 DG MOSFET technology

Fabrication of DG MOSFET is not straightforward. According to direction of the current carrying plane, three ways to fabricate a DG MOSFET [5] are plotted in Figure 1.3(c). In Figure 1.4 (a), the current flow in the plane, parallel to the silicon wafer is shown. Uniform silicon channel thickness can be easily achieved in this structure. Fabrication of this type of DG MOSFET has been demonstrated using selective epitaxial growth [6]. The non-planar structures in Figure 1.4 (b) and (c) allow an easy formation of and access to both top and bottom gate or a wraparound gate. The most successful example of structure (c) was the Fin-FET.

ISSN: 2278-0181
Vol. 2 Issue 1, January- 2013

The authors realized that biasing SOI substrate as the bottom gate was not realistic for circuit application and proposed using double SIMOX method to produce a silicon layer between two BOX layers as the bottom gate layer. However, the method was also not realistic for modern technology because of the difficulty to pattern the bottom gate and to form very thin bottom gate oxide by oxygen implantation.

Various methods have been proposed to fabricate a DG MOSFET without using an SOI substrate as the bottom gate. Wong and his colleagues in IBM proposed a self-aligned method of using epitaxial silicon grown from seed window on substrate as the silicon channel [7], but this DG MOSFET process suffered from excess complexity. In the last 6-7 years, most of the efforts were put on the fabrication of FinFET [8], where the current flows in the direction as depicted in Figure 1.3. The name of FinFET is after the shape of the silicon body. In this structure, the width of the silicon body is typically narrower than its height to achieve good channel potential control by the gates at both sides of the silicon fin and hence most of the current flows at side surface of the silicon fin. The idea of controlling the SCE by using narrow silicon island was actually first proposed by Leobandung and Chou at 1996 [9], where SOI MOSFET with 35nm-wide and 50nm-high silicon body was fabricated and characterized.

While still facing some challenges, such as reducing the series resistance rising from the thin silicon body and offering multiple threshold voltage to support high-performance applications, DG MOSFET technology has the opportunity to be widely applied in main-stream products as new progress unceasingly emerges [10]. Applications including DRAM and non-volatile memory have already been found for FinFET.

2.4 DG MOSFET modeling

Given such a promising importance, device modeling on DG MOSFET becomes a necessity for the very possible future application. This thesis will focus on the device modeling of the DG FinFET. The following is a review on the DG MOSFET modeling.

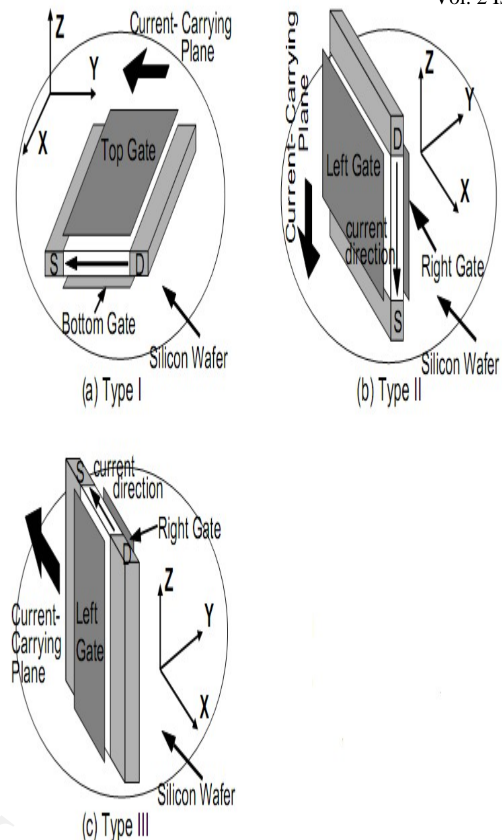

Figure 1.4 Three representative structures of DG MOSFET

IJERT

Like modeling the bulk MOSFET, electrostatics is the first consideration for DG MOS device modeling. Lots of work has shown that Boltzmann statistics is an adequate approximation of Fermi-Dirac statistic to calculate the carrier density, whereby the latter the derivation of analytical model will be impossible. Furthermore, the quantum-confinement effects (QCEs) can also be ignored without affecting the general results or the basic trend for devices with Si film thicker than 5-10nm [11] and might eventually be treated as a correction [11]. Thus solving the electrostatic state of a one-dimensional DG device is simplified to solve the Poisson-Boltzmann equation.

Given its advantage of offering more physical insight than its numerical counterparts, analytical solutions to the DG MOS devices incorporating varying degrees of simplifying assumptions have been attempted before. For example, mobile charge is ignored in [12], thus limiting the application of the solution to the subthreshold regime of operation. In [13], the

surface potential solution is analytically given for both sub-threshold and strong inversion, but the first derivative of the solution is not continuous at the transition point.

Threshold voltage (V_{th}) is one of the basic parameters that characterize the device performance and is important to the circuit designers. V_{th} for bulk MOSFET is classically defined at the surface potential of two times of the body Fermi potential [14], where the surface potential is assumed to be pinned. Following this method, V_{th} to DG MOSFET was proposed [14]. However, this definition of V_{th} loses its physical meaning as the channel doping concentration in the DG device is preferred to be intrinsic. Another popular approach is to define an "operational" V_{th} [15] as the gate voltage required to induce a certain level of drain current per unit channel width of a MOSFET. Since a reference current in the sub-threshold regime of operation is usually selected [13], the resulting V_{th} is more relevant for studying the leakage current than for predicting the turn-on behavior in the quasi-linear regime of operation.

3. INDEPENDENT DOUBLE GATE FINFET

The device structure of the FinFET is shown in Fig. 2.1. As DELTA, the channel was formed on the side “vertical” surface of the Si-fin, and the current flows in parallel to the wafer surface. The device used the elevated S/D process first applied on DELTA [16]. The heart of the FinFET is a thin (~20nm) Si fin, which serves as body of the MOSFET. A heavily-doped poly-Si film wraps around the fin and makes electrical contact to the vertical faces of the fin. The poly-Si film greatly reduces the S/D series resistance and provide a convenient means for local interconnect and making connections to the metal. A gap is etched through the poly-Si film to separate the source and drain. The width of this gap, further reduced by the dielectric spacers determines the gate length. The channel width is basically twice the fin height (plus the fin width). The conducting channel is wrapped around the surface of the fin. Hence the name-FinFET. Because the S/D and gate are much thicker (taller) than the fin, the device structure is quasi-planar. The starting material is a SOI wafer with a 400-nm thick buried oxide layer and 50-nm thick silicon film. The measured standard deviation of the silicon film thickness is around 20 A. Although the silicon film thickness determines the channel width, the variation is acceptable for the device uniformity. The variation in the gate length will be a larger source of process variation.

The CVD Si_3N_4 and SiO_2 stack layer is deposited on the silicon film to make a hard mask or cover layer. The cover layer will protect the Si-fin through the fabrication process steps. The fine Si-fin is patterned by electron beam (EB) lithography with 100 keV acceleration energy. The resist pattern is slightly ashed at 5 W and 30 sec to reduce the Si-fin width. Then, using top SiO_2 layer as a hard etching mask, the SOI layer is etched. The Si is exposed only at the sides of the Si-fin. Fabricate Si-fin width with the EB dose as a parameter. Fine Si-fins down to 20 nm are obtained. In-situ phosphorus-doped-amorphous Si (for S/D pads) is deposited at 480ºC. To suppress the native oxide growth on the Si-fin side surfaces, the wafers are loaded at 300ºC. After –Si deposition, SiO_2 is deposited at 450ºC. The process temperatures are low enough to suppress impurity diffusion into the Si-fin. Using EB lithography, the S/D pads with a narrow gap in between them are delineated. The SiO_2 and amorphous Si layers are etched and the gap between the S/D pads is formed.

IJERT

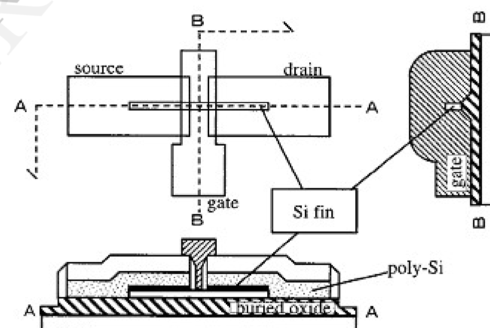

Figure 2.1 FinFET typical layout and schematic cross sectional structures.

While the cover layer protects the Si-fin, the amorphous Si is completely removed from the side of the Si-fin. The amorphous Si in contact to with the Si-fin at its side surfaces becomes the impurity diffusion source that forms the transistor S/D later. By using the two-dimensional (2-D) device simulator, the behavior of electrons and holes is calculated. The current density contour shows that the current quickly spreads into the pads. This suggests that the parasitic resistance is reduced.CVD SiO_2 is deposited to make spacers around the S/D pads. The height of the Si fin is 50nm, and the total

S/D pads thickness is 400nm. Making use of the difference in the heights, the SiO_2 spacer on

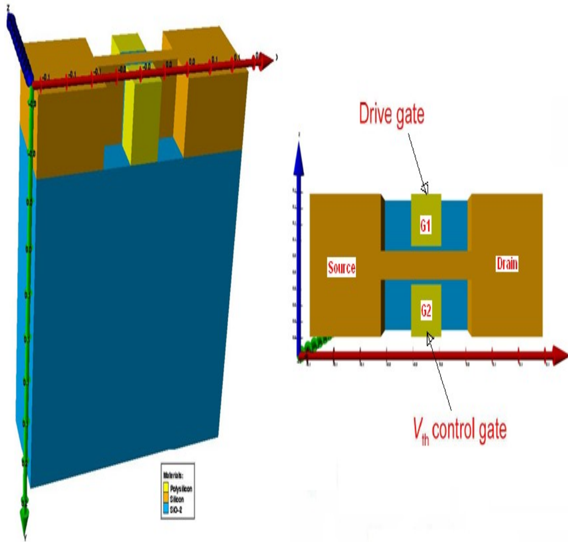

Figure 2.2 Structure of IDDG FinFET

the sides of the Si-fin is completely removed by sufficient over etching of SiO_2 while the cover layer protects the Si-fin. The Si surface is exposed on the sides of the Si-fin again. During this over etching, SiO_2 on the S/D pads and the buried oxide are etched.

By measuring the buried oxide thickness, we confirmed the amount of the etched SiO_2. A brief summary of the typical sizes: 100nm gap between the S/D pads, 40nm spacer length, and 20nm gate length. Also, the gate oxidation should thin the Si-fin width slightly. Notice that the channel width of the devices is twice the height of the Si-fins or approximately 100nm. By oxidizing the Si surface, gate oxide as thin as 1nm is grown. Because the area of Si-fin side surface is too small, we use dummy wafers to measure the oxide thickness with ellipsometry. During gate oxidation, the amorphous Si of the S/D pads is crystallized. Also, phosphorus diffuses from the S/D pads into the Si-fin and forms the S/D extensions under the oxide spacers. Then, boron-doped Si Ge is deposited at 475ºC as the gate material. Because the source and drain extension is already formed and covered by thick SiO_2 layer, no high temperature steps are required after gate deposition. Therefore, the structure is suitable to use with new high gate dielectric and metal gates that are not compatible with each other under high temperature.

3.1 I-V model

Fig. 2.3 presents a schematic structure of a symmetric DG FinFET, where x is the direction across the channel thickness and y is the direction along the channel. Here symmetric mea minantly in the y direction, and is assumed negligible ns that the two gates have the same work function, the top and bottom gate oxides are of equal materials and thicknesses, and the same voltage bias is applied to both gates. Midgap work function gate materials are assumed. It is assumed that the quasi-Fermi level is constant along the x direction, since current flows predo in the x direction. Because there is no contact to the silicon body, the energy levels are referenced to the electron quasi-Fermi level of the n+ source. For simplicity's sake, the formulation is based on Maxwell–Boltzmann carrier charge distribution statistics. Although the previously mentioned secondary effects will not be included here, they may be taken into account later to describe devices with ultra small silicon film thicknesses where these effects become relatively important.

IJERT

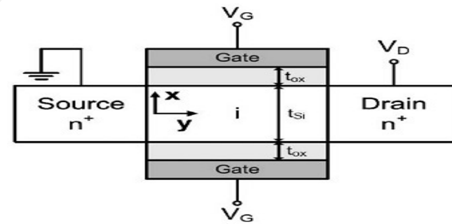

Figure 2.3 Schematic structure of the symmetric DG FinFet

3.2 Calculation of the potentials

Considering an n-MOSFET, neglecting the contribution of holes and considering potentials $\Phi >> kT$, the one-dimensional Poisson equation across the transverse direction x (body thickness) of this device, under the quasi-equilibrium approximation, leads to the following two equations [17]

$$V_{GF} = \phi_S + \frac{\sqrt{2kTn_i\varepsilon_s}}{C_{ox}}\sqrt{e^{-\beta V}\left(e^{\beta\phi_S} - e^{\beta\phi_o}\right)} \qquad (1)$$

and

$$\phi_S = \phi_o - \frac{2}{\beta}\ln\left\{\cos\left[\sqrt{\frac{q^2 n_i}{2lT\varepsilon_S}}e^{\frac{\beta(\phi_o - V)}{2}}\frac{t_{si}}{2}\right]\right\} \qquad (2)$$

where V_{GF} is the difference between the gate-to-source voltage and the flat-band voltage, $\beta = q/kT$ is the inverse of the thermal voltage, Φ_S is the surface potential (x = $t_{Si}/2$), Φ_o is the potential extremum at the center of the silicon film (x =0), C_{ox} is the gate oxide capacitance per unit area, ε_s is the permittivity of the semiconductor, t_{Si} is the semiconductor film thickness, V is the difference between electron and hole quasi-Fermi levels along the channel which is the channel voltage equal to 0 at the source and to V_{DS} at the drain. The above system of two equations (1) and (2) must be solved to obtain the surface potential, Φ_S, and the center-of-film potential extreme, Φ_o, both at the source, y = 0, and at the drain, y = L, ends of the channel.

The potentials may be evaluated either exactly by iterative numerical methods, or approximately by using recently proposed analytical expressions, in which case the resulting current model would be described by a completely analytical expression. The solution at the source end, with V = 0, gives: $\Phi_S = \Phi_{S0}$ and $\Phi_o = \Phi_{o0}$. Analogously, solving at the drain end with V = V_{DS} produces: $\Phi_S = \Phi_{SL}$ and $\Phi_o = \Phi_{oL}$.

3.3 Pao–Sah's type formulation

The drain current can be expressed following Pao and Sah's idea that including both the drift and diffusion carrier transport components in the silicon film leads to a current description with smooth transitions between operating regions. Under the approximation that the mobility is independent of position in the channel, the current may be expressed as [18]

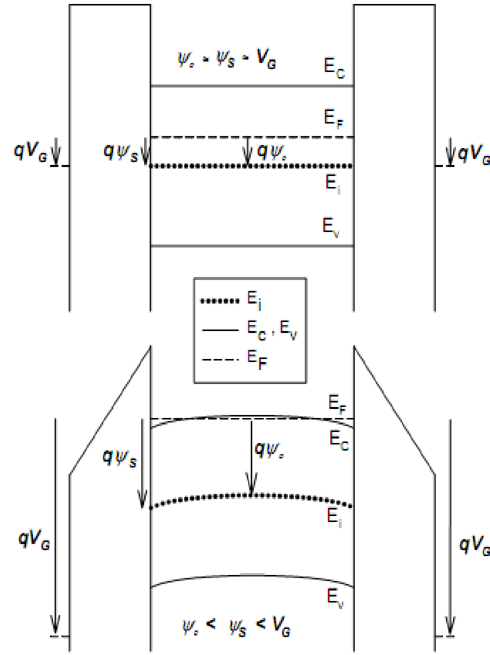

Figure 3.4 DG FinFET channel potential across the silicon film thickness.

IJERT

$$I_D = \mu\frac{W}{L}\int_0^{V_{DS}} Q_I\, dV \qquad (3)$$

where μ is the effective electron mobility, W is the channel width, L is the effective channel length, and Q_I is the total (integrated in the transverse direction) inversion charge density inside the silicon film at a given location,y, along the channel.

It is defined by

$$Q_I \equiv -2q\int_0^{\frac{t_{si}}{2}}(n - n_i)dx = -2q\int_{\phi_o}^{\phi_S}\frac{n - n_i}{F}d\phi \qquad (4)$$

where n_i is the intrinsic carrier density and F is the electric field. Since $n >> n_i$ and there is no fixed charge in the undoped body, Q_I can be taken as being the total semiconductor charge:

$Q_I=2\varepsilon F_S=-2C_{ox}(V_{GF}-\Phi_S)$

(5)

where F_S is the electric field at the surface, and the ‘‘2’’comes from the symmetry of the device. An equivalent to Pao–Sah's equation may be obtained for the DG SOI MOSFET by substituting (4) into (3), and remembering that $n >> n_i$

$$I_D = 2\mu \frac{W}{L} \int_0^{V_{DS}} \int_{\phi_o}^{\phi_S} \frac{qn}{F} \, d\phi dV \quad (6)$$

where the electric field F in the semiconductor film is given by

$$F = -\frac{d\phi}{dx} = -\sqrt{\frac{2kTn_i}{\varepsilon_S} e^{-\beta V)} (e^{\beta\phi} - e^{\beta\phi_o})} \quad (7)$$

and

$$n=n_i e^{\beta(\Phi-V)} \quad (8)$$

For convenience, we rewrite (7) as

$$F = -\sqrt{\frac{2kTn_i}{\varepsilon_S} e^{\beta(\phi-V)} + \alpha} \quad (9)$$

where $$\alpha = -\sqrt{\frac{2kTn_i}{\varepsilon_S} e^{\beta(\phi_o-V)}} \quad (10)$$

is defined as an interaction factor representing the charge coupling between the two gates, following our previous formulation [19].

3.4 Pierret and Shields' type current model

We now proceed to evaluate the partial derivative of (9) with respect to channel voltage, following the procedure developed by Pierret and Shields [20]

$$\frac{\partial F}{\partial V} = \frac{1}{2F}\frac{d\alpha}{dV} - \frac{1}{F}\frac{qn_i}{\varepsilon_S} e^{\beta(\phi-V)} \quad (11)$$

In the above equation we have written the total derivative $d\alpha/dV$ because α does not depend on w. Substituting (8) into (11) yields

$$\frac{qn}{F} = \varepsilon_S \left(\frac{1}{2F}\frac{dx}{dV} - \frac{\partial F}{\partial V} \right) \quad (12)$$

Further substitution of (12) into (6) gives

$$I_D = 2\mu_n \frac{W}{L} \varepsilon_S \int_0^{V_{DS}} \int_{\phi_o}^{\phi_S} \left(\frac{1}{2F}\frac{dx}{dV} - \frac{\partial F}{\partial V} \right) d\phi dV \quad (13)$$

Let us separate, for manipulation convenience, the two terms in the integrand of the double integral in (13) into two integrals, I_1 and I_2, such that $I = I_1 - I_2$. The first integral yields

$$I_1 = \int_0^{V_{DS}} \int_{\phi_o}^{\phi_S} \frac{1}{2F}\frac{dx}{dV} d\phi dV = \frac{1}{2}\int_0^{V_{DS}} \frac{d\alpha}{dV} \left(\int_{\phi_o}^{\phi_S} \frac{1}{F} d\phi \right) dV = \frac{1}{2}\int_0^{V_{DS}} \frac{d\alpha}{dV}\frac{t_{si}}{2} dV = \frac{t_{si}}{4}(\alpha_0 - \alpha_L) \quad (14)$$

where α_0 and α_L represent the values of the coupling coefficient a evaluated at the source and at drain ends, respectively. Next we proceed to calculate the integral I_2, defined by

$$I_2 = \int_0^{V_{DS}} \int_{\phi_o}^{\phi_S} \frac{\partial F}{\partial V} d\phi dV \quad (15)$$

IJERT

ISSN: 2278-0181
Vol. 2 Issue 1, January- 2013

This integral I_2, may be further broken up into four integrals:

$$I_2 = \int_0^{V_{DS}} \int_{\phi_o}^{\phi_S} \frac{\partial F}{\partial V} d\phi dV =$$

$$\int_0^{V_{DS}} \int_{\phi_m}^{\phi_{S0}} \frac{\partial F}{\partial V} d\phi dV + \int_0^{V_{DS}} \int_{\phi_{S0}}^{\phi_S} \frac{\partial F}{\partial V} d\phi dV$$

$$-\int_0^{V_{DS}} \int_{\phi_m}^{\phi_{o0}} \frac{\partial F}{\partial V} d\phi dV - \int_0^{V_{DS}} \int_{\phi_{o0}}^{\phi_o} \frac{\partial F}{\partial V} d\phi dV \tag{16}$$

where Φm is any value less than Φ_{o0} and its value is not important. Since the first and the third terms in the above equation both have constant limits of integration, the order of integration may be inverted, yielding

$$\int_0^{V_{DS}} \int_{\phi_m}^{\phi_{S0}} \frac{\partial F}{\partial V} d\phi dV = \int_{\phi_m}^{\phi_{S0}} \int_0^{V_{DS}} \frac{\partial F}{\partial V} dV d\phi$$

$$= \int_{\phi_m}^{\phi_{S0}} [F(\phi, V = V_{DS}) - F(\phi, V = 0)] d\phi \tag{17}$$

And

$$\int_0^{V_{DS}} \int_{\phi_m}^{\phi_{o0}} \frac{\partial F}{\partial V} d\phi dV = \int_{\phi_m}^{\phi_{S0}} \int_0^{V_{DS}} \frac{\partial F}{\partial V} dV d\phi$$

$$= \int_{\phi_m}^{\phi_{o0}} [F(\phi, V = V_{DS}) - F(\phi, V = 0)] d\phi \tag{18}$$

Now we change the order of integration in the second term of I_2 in (16)

$$\int_0^{V_{DS}} \int_{\phi_{S0}}^{\phi_S} \frac{\partial F}{\partial V} d\phi dV = \int_{\phi_{S0}}^{\phi_{SL}} \int_{V_S}^{V_{DS}} \frac{\partial F}{\partial V} dV d\phi \tag{19}$$

where V_S is the moving value of V at which the potential is $\Phi = \Phi_S$. Now integrating (19) produces

$$\int_0^{V_{DS}} \int_{\phi_m}^{\phi_{S0}} \frac{\partial F}{\partial V} d\phi dV =$$

$$\int_{\phi_{S0}}^{\phi_{oL}} [F(\phi, V = V_{DS}) - F(\phi, V = V_S)] d\phi \tag{20}$$

Similarly, the fourth term of I_2 in (16) may be written as

$$\int_0^{V_{DS}} \int_{\phi_{o0}}^{\phi_o} \frac{\partial F}{\partial V} d\phi dV =$$

$$\int [F(\phi, V = V_{DS} - F)(\phi, V = V_o)] d\phi \tag{21}$$

where Vo is the moving value of V at which the potential is $\Phi = \Phi_o$. Substituting (17), (18), (20), and (21) into (16) and reordering yields

$$\int_0^{V_{DS}} \int_{\phi_m}^{\phi_{S0}} \frac{\partial F}{\partial V} d\phi dV =$$

$$\int_{\phi_{oL}}^{\phi_{SL}} F(\phi, V = V_{DS}) d\phi -$$

$$\int_{\phi_{o0}}^{\phi_{S0}} F(\phi, V = 0) d\phi - \int_{\phi_{S0}}^{\phi_{SL}} F(\phi, V = V_S) d\phi$$

$$+ \int_{\phi_{o0}}^{\phi_{oL}} F(\phi, V = V_o) d\phi \tag{22}$$

Since $\Phi = \Phi_S$ for $V = V_S$, we recognize that $F(\Phi = \Phi_S, V = V_S) = F_S$. Therefore, the third term in (22) may be integrated using (5),

$$\int_{\phi_{S0}}^{\phi_{SL}} F(\phi, V = V_S) d\phi = \int_{\phi_{S0}}^{\phi_{SL}} F_S d\phi$$

IJERT

$$= \int_{\phi_{S0}}^{\phi_{SL}} \frac{C_{ox}}{\varepsilon_S}(V_{GF} - \phi) d\phi$$

$$= \frac{C_{ox}}{\varepsilon_S}\left[V_{GF}(\phi_{SL} - \phi_{S0}) - \frac{1}{2}\left(\phi_{SL}^{\ 2} - \phi_{S0}^{\ 2}\right)\right] \qquad (23)$$

Analogously, integrating the fourth term of (22) yields

$$\int_{\phi_{o0}}^{\phi_{0L}} F(\phi, V = V_o) d\phi = 0 \qquad (24)$$

because the integrand is zero since it is the electric field at $\Phi = \Phi o$. The integral in second term of (22) may be evaluated using (9) and (10):

$$\int_{\phi_{o0}}^{\phi_{S0}} F(\phi, V = V_o) d\phi = \int_{\phi_{o0}}^{\phi_{S0}} \sqrt{\frac{2kTn_i}{\varepsilon_S} e^{\beta\phi} + \alpha_0} \, d\phi$$

$$= \frac{2}{\beta}\sqrt{\frac{2kTn_i}{\varepsilon_S}}\left[\sqrt{e^{\beta\phi_{S0}} - e^{\beta\phi_{o0}}} - e^{\frac{\beta\phi_{o0}}{2}}\right.$$

$$\left. X \arctan\left(\sqrt{e^{\beta(\phi_{S0} - \phi_{o0})} - 1}\right)\right] \qquad (25)$$

Analogously, the integral in the first term of (22) is:

$$\int_{\phi_{oL}}^{\phi_{SL}} F(\phi, V = V_{DS}) d\phi = \int_{\phi_{oL}}^{\phi_{SL}} \sqrt{\frac{2kTn_i}{\varepsilon_S} e^{\beta(\phi - V_{DS})} + \alpha}$$

$$= \frac{2}{\beta}\sqrt{\frac{2kTn_i}{\varepsilon_S}} e^{-\frac{\beta V_{DS}}{2}}\left[\sqrt{e^{\beta\phi_{SL}} - e^{\beta\phi_{oL}}} - e^{\frac{\beta\phi_{oL}}{2}}\right.$$

$$\left. X \arctan\left(\sqrt{e^{\beta\phi_{SL}} - e^{\beta\phi_{oL}} - 1}\right)\right] \qquad (26)$$

Finally, combining of (10), (13), (14), (15), (16), (22), (23), (24), (25), (3.2.26) yields the general current–voltage equation valid for all bias conditions:

$$I_D =$$

$$\mu\frac{W}{L}\left\{2C_{ox}\left[V_{GF}(\phi_{SL} - \phi_{S0}) - \frac{1}{2}\left(\phi_{SL}^{\ 2} - \phi_{S0}^{\ 2}\right)\right]\right\}$$

$$- t_{si} l T n_i \varepsilon_S \left[e^{\beta(\phi_{0L} - V_{DS})} - e^{\beta\phi_{o0}}\right]$$

$$+ \frac{4}{\beta}\sqrt{2kTn_i\varepsilon_S}$$

$$* \left[\sqrt{e^{\beta\phi_{S0}} - e^{\beta\phi_{o0}}} - e^{\frac{\beta\phi_{o0}}{2}} X \arctan\left(\sqrt{e^{\beta\phi_{SL}} - e^{\beta\phi_{oL}} - 1}\right)\right]$$

$$- \frac{4}{\beta}\sqrt{2kTn_i\varepsilon_S} e^{-\frac{\beta V_{DS}}{2}}\left[\sqrt{e^{\beta\phi_{SL}} - e^{\beta\phi_{oL}}} - e^{\frac{\beta\phi_{oL}}{2}}\right.$$

$$\left. X \arctan\left(\sqrt{e^{\beta\phi_{SL}} - e^{\beta\phi_{oL}} - 1}\right)\right] \qquad (27)$$

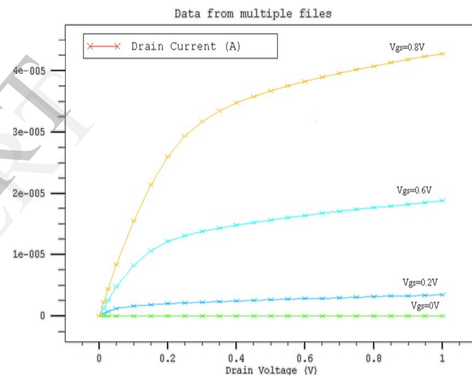

Figure 3.5 Drain current, as a function of drain voltage for several values of gate voltage.

After some algebraic and trigonometric manipulations of (2), (5) and (7), the last three terms of (27) may be further simplified to

$$I_D =$$

$$\mu\frac{W}{L}\left\{2C_{ox}\left[V_{GF}(\phi_{SL} - \phi_{S0}) - \frac{1}{2}(\phi_{SL}^{\ 2} - \phi_{S0}^{\ 2})\right]\right\}$$

$$+ 4\frac{kT}{q} C_{ox}(\phi_{SL} - \phi_{S0}) \qquad (28)$$

$$+ t_{si} kTn_i \left[e^{\beta(\phi_{oL} - V_{DS})} - e^{\beta\phi_{o0}}\right]$$

IJERT

Fig. 3.5 presents the drain current as a function of drain voltage for several values of gate voltage, as calculated by the present analytic model together with exact results from fourth-order Sympson-type numerical integration of the carrier charge along the channel, for $0< V_{DS} < 1$ V with increments of 1 mV. The surface and center-of-film potentials needed in (28), and the carrier charge, needed for the direct numerical integration, were calculated from the iterative solution of (1) and (2).

4. CONCLUSION

This work presents the current modeling of FinFET . As the physical gate length is scaled into deep sub-micron regime, this scaling process become increasingly difficult as several major limits from both process and device performance are approaching. Therefore, non-classical CMOS devices were introduced to extend the roadmap of MOSFET scaling. This thesis focused on the modeling of DG FinFET, which is one of the most promising candidates for future application. The gate length of FinFET can be shrunk down to 20nm. The device simulation has been done by using SILVACO software TOOL.

IJERT

5. REFERENCES

[1] G. E. Moore, "Cramming more components onto integrated circuits," *Electronics,* Vol. 38, Number 8, April 19, 1965.

[2] D. L. Critchlow, "MOSFET Scaling—The Driver of VLSI Technology," *Proceedings of the IEEE,* Vol. 87, No. 4, pp.659-667, Apr. 1999

[3] D. J. Frank, S. E. Laux and M. V. Fischetti “Monte Carlo Simulation of a 30 nm Dual-Gate MOSFET: How Short Can Si Go?” IBM Research Division, NY 10598

[4] D. Kahng, "A Historical Perspective on the Development of MOS Transistors and Related Devices," *IEEE Transactions on Electron Devices,* Vol. ED-23, pp.655-657,1976.

[5] G. K. Celler, Sorin Cristoloveanu, "Frontiers of Silicon-on-Insulator", *Journal of Applied Physics,* Vol. 93, No. 9, pp4955, May 2003.

[6] F. Balestra, S. Cristoloveanu, M. Benachir, J. Brini, T. Elewa, "Double-gate silicon-on-insulator transistor with volume inversion: A new device with greatly enhanced performance," *IEEE Electron Device Letters,* Vol. EDL-8, No. 9, pp.410-412, Sept. 1987.

[7] H.-S. P. Wong, "Beyond the Conventional Transistor", *IBM J. RES & DEV.,* Vol. 46, No. 2/3, pp.133-168, March/May 2002.

[8] H.-S. Wong, K. Chan, and Y. Taur, "Self-Aligned (Top and Bottom) Double-Gate MOSFET with a 25 nm Thick Silicon Channel," *IEEE International Electron Device Meeting,* pp.427-430 1997.

[9] Y.K. Choi, N. Lindert, P. Xuan, S. Tang, "Sub-20nmCMOS FinFET Technologies," *IEEE International Electron Device Meeting,* pp. 19.1.1 -19.1.4, 2001.

[10] Y.Liu, M. Masahara, K. Ishii, T. Tsutsumi, "Flexible Threshold Voltage FinFETs with Inde pendent Double Gates and an Ideal Rectangular Cross-Section Si-Fin Channel," *IEEE International Electron Device Meeting,* pp.18.8.1-18.8.3, 2003.

[11] Taur Y. An analytical solution to a double-gate MOSFET with undoped body. IEEE Electron Device Lett 2000;21:245–7.[10] Taur Y. Analytic solutions of charge and capacitance in symmetric and asymmetric double-gate MOSFETs. IEEE Trans ElectronDevices 2001;48:2861–9.