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Data Encoding Techniques for Lower Power Dissipation in Network on Chip

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***Abstract*—In this project, a low-power data encoding scheme is proposed. In general, system-on-chip (soc) based system has so many disadvantages in power-dissipation as well as clock rate wise such transfer the data from one system to another system in on-chip. At the same time, a higher operated system does not support the lower operated bus network for data transfer. However an alternative scheme is proposed for high speed data transfer. But this scheme is limited to SOCs. Unlike soc, network-on-chip (NOC) has so many advantages for data transfer. It has a special feature to transfer the data in on-chip named as transitional encoder. Its operation is based on transitions of input data. At the same time it supports systems which are operated at higher frequencies. The proposed system yields lower dynamic power dissipation due to the reduction of switching activity and coupling switching activity when compared to existing system. Even-though many factors which are based on power dissipation, the dynamic power dissipation is only considerable for reasonable advantage. The proposed system is synthesized as well as simulated using Quartus II 9.1 simulated design software. Besides, the proposed system will be extended up-to inter-link PE communication (data transfer from one PE to other) with help of routers and PEs which are performed by various operations. To implement this system, a real NOC which contains the proposed encoders & decoders for data transfer with regular traffic scenarios should be considered.**

***Index Terms*—Coupling switching activity, data encoding, interconnection on chip, low power, network-on-chip (NoC),power analysis.**

I. INTRODUCTION

As VLSI technologies continue to scale, wire densities increases to support ever-small transistor geometries and casuses on-chip wires to present increasing latency and energy problem. In particular, the high latency of cross-chip communication can still limit total performance by increasing the delay between on-chip unit. Such scalable bandwidth requirement can be satisfied by using on-chip packet-switched micro-network of interconnects, generally known as Network-on-Chip (NoC) architecture. The basic idea came from the traditional large-scale multi-processors and distributed computing networks. The scalable and modular nature of NoC and their support for efficient on-chip communication lead to the NoC-based system implementations. In order to meet typical SoCs or multi-core processing and basic module of network interconnection like switching logic, routing algorithm and the packet definition should be light-weighted to result in easily implemental solutions. Another approach to exceed such a limitation of communication and overcome such an enormous wiring delay in future technology is to adopt network-like interconnections which is called Network-on-Chip (NoC) architecture. Basic concept of such kind of interconnections is from the modern computer network evolution as mentioned before. By applying network-like communication which inserts some routers in-between each communication object, the required wiring can be shortened. Therefore, the switch-based interconnection mechanism provides a lot of scalability and freedom from the limitation of complex wiring. Replacement of SoC busses by NoCs will follow the same path of data communications when the economics prove that the NoC either reduces SoC manufacturing cost, SoC time to market, SoC time to volume, and SoC design risk or increases SoC performance. According to the NoC approach has a clear advantage over traditional busses and most notably system throughput. And hierarchies of crossbars or multilayered busses have characteristics somewhere in between traditional busses and NoC, however they still fall far short of the NoC with respect to performance and complexity.The success of the NoC design depends on the research of the interfaces between processing elements of NoC and interconnection fabric. The interconnection of a SoC established procedures has some weak points in those respects of slow bus response time, energy limitation, scalability problem and bandwidth limitation. Bus interconnection composed of a large number of components in a network interface can cause slow interface time though the influence of sharing the bus. In addition the interconnection has a defect that power consumption is high on the score of connecting all objects in the communication. Moreover it is impossible to increase the number of connection of the elements infinitely by reason of the limitation of bandwidth in a bus.

As a consequence, the performance of the NoC design relies greatly on the interconnection paradigm .Though the network technology in computer network is already well developed, it is almost impossible to apply to a chip-level

intercommunication environment without any modification or reduction. For that reason, many researchers are trying to develop appropriate network architectures for on-chip communication. To be eligible for NoC architecture, the basic functionality should be simple and light-weighted because the implemented component of NoC architecture should be small enough to be a basic component constructing a SoC. In order to be low powered one has to consider many parameters such as clock rate, operating voltages,power management.

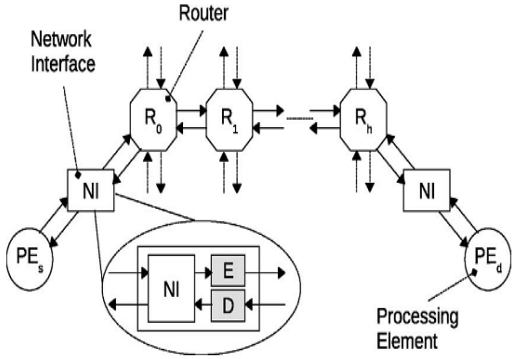


Fig: Fundamental concept of NOC

As shown in Fig the NI is augmented with an encoder(E) and a decoder (D) block. With the exception of the header flit, the encoder encodes the outgoing flits of the packet in such a way as to minimize the power dissipated by the inter-router point-to-point links which form the routing path of the current packet. Since the routers are not equipped with any encoding/decoding logic, the header flit is not encoded as it contains control information (destination address, packet size, and so on) which have to be processed by the routers through the routing path. Similarly to the above description, all the incoming flits in the network interface (with the exception of the header flit) are decoded by the encoder block. It should be pointed out that the proposed scheme is de-signed to be applied in the context of no VC based implementations. In fact, if VCs are used, the assumption that the flits belonging to different packets are not interleaved in the same link is not valid anymore. At any rate, it does not mean that the proposed scheme cannot be applied in VC based implementations but, instead, that the potential power savings are reduced.

II. Related Works and Contributions

In the next several years, the availability of the chips with 1000 cores is foreseen [6]. In these chips, a significant fraction of the total system power budget is dissipated by interconnection network. Therefore, the design of power-efficient interconnection networks has been the focus of many works published in the literature dealing with NoC architecture. These works concentrate on different components of the interconnection networks such as routers, NI, and links. Since the focus of this paper is on reducing the power dissipation by the links, in this section, briefly review some of the works in the area of link power reduction. These include the techniques that make use of shielding [7], [8], increasing line-to-line spacing [9], [10], repeater insertion [11]. They all increases the chip area. The data encoding scheme is another method that was employed to reducing the link power dissipation. The data encoding techniques may be classified into two types. In the first type, encoding techniques concentrate on lowering the power due to self-switching activity of individual bus lines while ignoring the power dissipation owing to their coupling switching activity. In this type, bus invert (BI) [12] and INC-XOR [13] have been proposed for the case that random data patterns are transmitted through these lines. On the other hand, gray code [14], T0 [15], working-zone encoding [16], and T0-XOR [17] were suggested for the case of correlated data patterns. Application-specific approaches have also been proposed [18]–[22].This category of encoding is not suitable to applied in the deep sub micron meter technology nodes where the coupling capacitance constitutes a major part of the total interconnect capacitance. This causes the power consumption due to the coupling switching activity to become a large fraction of the total link power consumption, making the above mentioned techniques, which ignore such contributions, inefficient [23].The works in the second type concentrate on reducing power dissipation through the reduction of the coupling witching [10], [22] Among these schemes [10], [24]– [28], the switching activity is reduced using many extra control lines. For example, data bus width grows from 32 to 55 in [24]. The techniques proposed in [20] have a smaller number of control lines but the complexity of their decoding logic is high. The technique is described as follows: first, the data are both odd inverted and even inverted, and the transmission is performed using the kind of inversion that reduces more the switching activity. In [30],the coupling switching activity is reduced up to 39%. In this paper, compared to [30], we use a simpler encoder and decoder while achieving a higher activity reduction. Let us now discuss in more detail the works with which we compare our proposed data encoding schemes. In [12], the number of transitions from 0 to 1 for two consecutive flits (the flit that just traversed and the one which is about to traverse the link) is counted. If the number is larger than half of the link width, the inversion will be performed to reduce the number of 0 to 1 transitions when the flit is transferred via the link. This technique is only concerned about the self-switching without worrying the coupling switching. Note that the coupling capacitance in the state-of–the-art silicon technology is considerably larger (e.g., four times) compared with the self-capacitance, and should be considered in any scheme proposed for the link power reduction.

TABLE I
EFFECT OF ODD INVERSION ON CHANGE OF TRANSITION T YPES

Time	Normal			Odd Inverted		
	Type I			Types II, III, and IV		
$t-1$	00, 11	00, 11, 01, 10	01, 10	00, 11	00, 11, 01, 10	01, 10
t	10, 01	01, 10, 00, 11	11, 00	11, 00	00, 11, 01, 10	10, 01
	T1*	T1**	T1***	Type III	Type IV	Type II
$t-1$	Type II			Type I		
t	01, 10			01, 10		
	10, 01			11, 00		
$t-1$	Type III			Type I		
t	00, 11			00, 11		
	11, 00			10, 01		
$t-1$	Type IV			Type I		
t	00, 11, 01, 10			00, 11, 01, 10		
	00, 11, 01, 10			01, 10, 00, 11		

III. Proposed Encoding Schemes

In this section, present the proposed encoding scheme whose goal is to reduce power dissipation by minimizing the coupling transition activity on the links of the interconnection network. Let us first describe the power model that contains the different components of power dissipation of a link.. One can classify four types of coupling transitions. A Type I transition occurs when one of the lines switches when the other remains unchanged. In a Type II transition, one line switches from low to high, other makes transition from high to low .A Type III transition corresponds to the case where both lines switch simultaneously. Finally, in a Type IV transition both lines do not change. The effective switched capacitance varies from type to type and hence, the coupling transition activity, is a weighted sum of different types of coupling transition contributions .Here, we calculate the occurrence probability for different types of transitions. Consider that flit ($t-1$) and flit (t) refer to the previous flit which was transferred through the link and the flit is about to pass through the link, respectively.We consider only two adjacent bits of the physical channel.Sixteen different combinations of these four bits could occur (Table I). Note that the first bit is the value of the generic i th line of the link, whereas the second bit represents the value of its (i + 1)th line. The number of transitions for Types I, II, III, and IV are 8, 2, 2, and 4, respectively. For a random set of data, each of these sixteen transitions has the same probability. Therefore, the occurrence probability for Types I, II, III, and IV are 1/2, 1/8, 1/8, and 1/4, respectively. In the rest of this section, we present three data encoding schemes designed for reducing the dynamic power dissipation of the network links along with a possible hardware implementation of the decoder.

A.SCHEME I:

In Scheme I, we focus on reducing Type I transitions while in Scheme II, both Types I and II transitions are taken into account for deciding between half and full invert, depending the amount of switching reduction. Finally, in Scheme III, we consider the fact that Type I transitions show different behaviors in the case of odd and even invert and make the inversion which leads to the higher power saving.

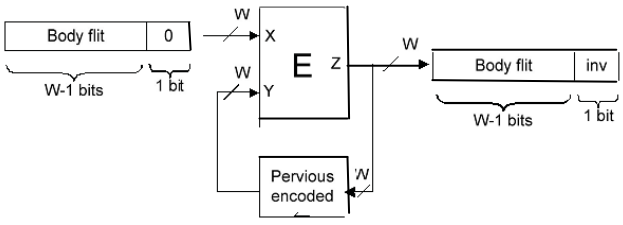


Fig:Circuit diagram of encoder architecture of scheme I

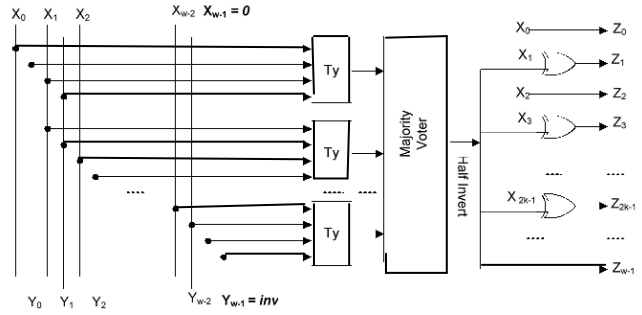


Fig: Internal view of encoder block

In scheme I, we focus on reducing the numbers of Type I transitions (by converting them to Types III and IV transitions) and Type II transitions (by converting them to Type I transition). The scheme compare the current data with the previous data one to decide whether odd inversion or no inversion of the current data can lead to the link power reduction.

Table I reports, for each transition, the relationship between the coupling transition activities of the flit when transmitted and when its bits are odd inverted. Data are organized as follows. The first bit is the value of the generic i th line of the link, whereas the second bit represent the value of its (i + 1)th line. For each partition, the first line represents the values at time $t-1(t)$.

As Table I shows, if the flit is odd inverted, Types II, III, and IV transitions convert to Type I transitions. In the case of Type I transitions, the inversion leads to one of Types II, III, or Type IV transitions. In particular, the transitions indicated as T∗1, T∗∗1,andT∗∗∗1 in the table convert to Types II, III, and IV transitions, respectively.

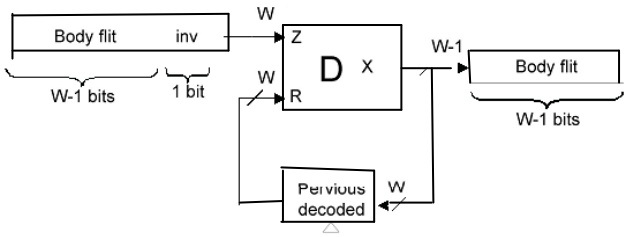


Fig: circuit diagram of decoder architecture

B.SCHEME II:

In the proposed encoding scheme II, we make use of both odd (as discussed previously) and full inversion. The full inversion operation converts Type II transitions to Type IV transitions. The scheme compares the current data with the previous one to decide whether the odd, full, or no inversion of the current data can give rise to the link power reduction.

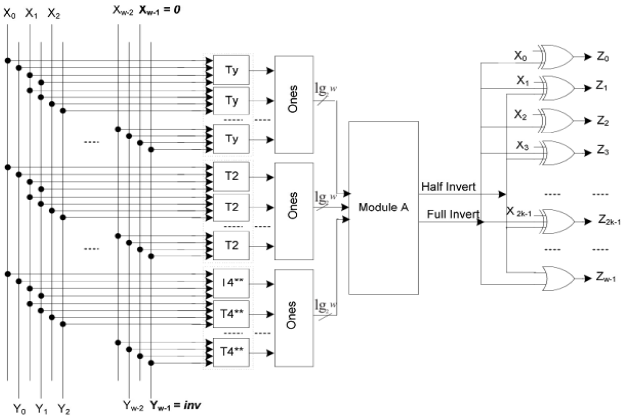


fig:Encoder architecture scheme II

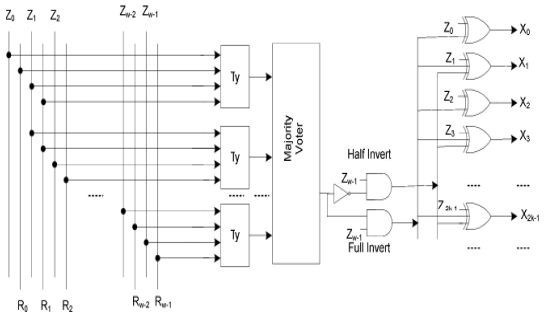


fig:Internal view of the decoder block scheme II

The w bits of the incoming body flit are indicated by Z I (R I), i = 0 , 1 ,...,w− 1. The w th bit of the body flit is indicated by inv which shows if it was inverted (inv = 1) or left as it was (inv = 0). For the decoder, we only need to have the Ty block to determine which action has been taken place in the encoder. Based on the outputs of these blocks , the majority voter block checks the validity of the inequality .If the output is "0" ("1") and the inv = 1,it means that half (full) inversion of the bits has been per-formed. Using this output and the logical gates, the inversion action is determined. If two inversion bits were used, the overhead of the decoder hardware could be substantially reduced.

This module determines if odd, even, full, or no invert action corresponding to the outputs "10,""01," "11," or "00," respectively, should be performed. The outputs "01," "11," and "10" show that whether respectively, are satisfied. In this paper, Module C was designed based on the conditions given .Similar to the procedure used to design the decoder for scheme II, the decoder for scheme III may be designed .This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception .

TABLE II
EFFECT OF EVEN INVERSION ON CHANGE OF TRANSITION TYPES

Time	Normal			Even Inverted		
	Type I			Types II, III, and IV		
$t-1$	01, 10	00, 11, 01, 10	00, 11	01, 10	00, 11, 01, 10	00, 11
t	00, 11	10, 01, 11, 00	01, 10	10, 01	00, 11, 01, 10	11, 00
	T1*	T1**	T1***	Type II	Type IV	Type III
$t-1$	Type II			Type I		
t	01, 10			01, 10		
	10, 01			00, 11		
$t-1$	Type III			Type I		
t	00, 11			00, 11		
	11, 00			01, 10		
$t-1$	Type IV			Type I		
t	00, 11, 01, 10			00, 11, 01, 10		
	00, 11, 01, 10			10, 01, 11, 00		

C.SCHEME III:

In the proposed encoding Scheme III, we add even inversion to Scheme II. The reason is that odd inversion converts some of Type I (T∗∗∗1) transitions to Type II transitions. As can be observed from Table II, if the flit is even inverted, the transitions indicated as T∗∗1/ T∗∗∗1 in the table are converted to Type IV/Type III transitions. Therefore, the even inversion may reduce the link power dissipation as well. The scheme compares the current data with the previous one to decide whether odd, even, full, or no inversion of the current data can give rise to the link power reduction.

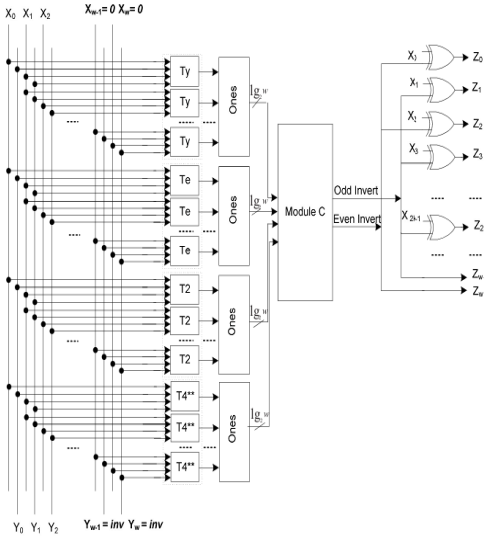
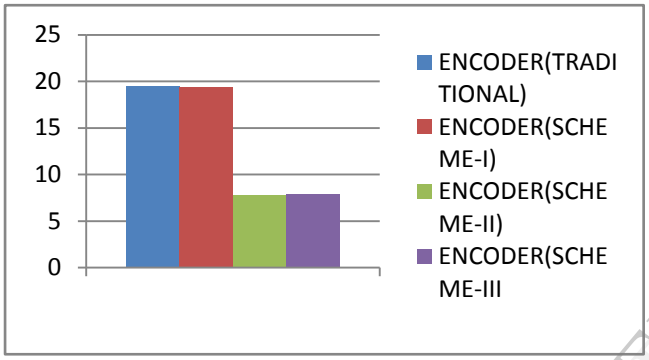


Fig:Encoder architecture scheme III

IV. RESULTS

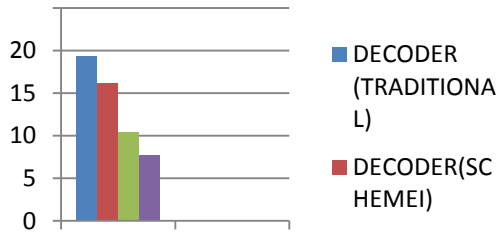
DYNAMIC POWER DISSIPATION FOR ENCODER:

ENCODER (TRADITIONAL)	ENCODER(PROPOSED) SCHEME –I	ENCODER(PROPOSED) SCHEME –II	ENCODER(PROPOSED) SCHEME – III
19.45 mw	19.43mw	7.76mw	7.87mw



DYNAMIC POWER DISSIPATION FOR DECODER :

DECODER (TRADITIONAL)	DECODER(PROPOSED) SCHEME –I	DECODER(PROPOSED) SCHEME -II	DECODER(PROPOSED) SCHEME –III
19.35mw	16.19mw	10.37mw	7.66mw



V. CONCLUSION

In this paper, a set of new data encoding schemes aimed at reducing the power dissipated by the links of an NoC. As compared to the previous encoding schemes the rationale behind the proposed schemes is to minimize not only the switching activity, but also the coupling switching activity which is mainly responsible for link power dissipation. By using the proposed encoding schemes in NoC architecture their application does not require any modification neither in the routers nor in the links. As per the performance evaluation results, the proposed system has lower dynamic power dissipation than classical one.

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