

DC Drive Control Using High Resolution Digital Pulse Width Modulator Based On FPGA

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Abstract—Digital pulse width modulator (DPWM) have many advantages in Power Electronics field. So there is increasing use of DPWM in Power Electronics application. However, the clock frequency requirements may exceed the operational limits when the power converter switching frequency is increased, while using classical DPWM architectures. This paper present a design to increase the resolution of the DPWM implemented on field programmable gate arrays (FPGA). There are some designs based on FPGA having very large code length. The proposed circuits are based on the on-chip digital clock manager block (DCM) present in the low-cost Spartan-3 FPGA series. The use of DCM block helps to introduce new method of generating DPWM. Implementation of this will be very helpful considering industrial applications where DPWM are mostly required.

Index Terms—Field programmable gate arrays (FPGA), power conversion, pulse-width modulated power converters.

I. Introduction:

Pulse Width Modulation (PWM) is now becoming an integral part of almost all embedded systems. It is widely accepted as control technique in most of the electronic appliances.

These techniques have been extensively researched during past few

years [1]. There are so many methods available depending on architecture and requirement of the system. Their design implementation depends upon application type, power consumption, semiconductor devices, performance and cost criteria all determining the PWM method [1].

Digital pulse-width modulators (DPWMs) have become a basic building block in digital control architectures of any power converter [2]. Digital control can be implemented by making use of Digital Signal Processing (DSP), Field Programmable Gate Array (FPGA), custom hardware and custom hardware plus software. The DPWM frequency is mainly determined by the power converter operating conditions, whereas the DPWM resolution determines the accuracy in the output voltage/current control. As a consequence, the DPWM resolution has a direct impact in the power converter performance.

Many traditional DPWM architectures are present which includes: counter comparator based architecture, Delay line architecture, Hybrid DPWM architecture, segmented delay line architecture, dithering, etc. [3]. Traditional DPWM based on counters and comparators generate the power converter gating signals according to several predefined thresholds [4]. Now days, power converters are evolving toward designs with higher switching frequencies in order to reduce the size of inductors and capacitors.

Several FPGA-based solutions have also been proposed in the literature [5], [6]. One common solution is to use a coarse resolution counter-based stage plus one or several on-chip digital clock manager (DCM) blocks. The PWM signal is set at the beginning of the counter period, and it is reset after a given number of clock cycles plus a certain fraction of the clock period established by the DCM.

The aim of this technique is to provide a fully synchronous high-resolution DPWM architecture in order to avoid the need of using unfeasible high clock frequencies, providing a more convenient final implementation. This technique is based on the resources available in modern FPGAs. The DCM based architecture allows operating the circuit at higher clock frequencies [7]. Higher switching frequency helps in enhancing the dynamic performance and hence provides higher DPWM resolution.

II. DCM Block:

Spartan-3 devices provide flexible, complete control over clock frequency, phase shift and skew through the use of the DCM feature. To accomplish this, the DCM employs a Delay-Locked Loop (DLL), a fully digital control system that uses feedback to maintain clock signal characteristics with a high degree of precision despite normal variations in operating temperature and voltage.

Each member of the Spartan-3 family has four DCMs, except the smallest, the XC3S50, which has two DCMs. The DCMs are located at the ends of the outermost Block RAM column(s). The DCM supports three major functions [8]:

- **Clock-skew Elimination:** Clock skew describes the extent to which clock signals may, under normal circumstances, deviate from zero-phase alignment. It occurs when slight differences in path delays cause the clock signal to arrive at

different points on the die at different times. This clock skew can increase set-up and hold time requirements as well as clock-to-out time, which may be undesirable in applications operating at a high frequency, when timing is critical.

The DCM eliminates clock skew by aligning the output clock signal it generates with another version of the clock signal that is fed back. As a result, the two clock signals establish a zero-phase relationship. This effectively cancels out clock distribution delays that may lie in the signal path leading from the clock output of the DCM to its feedback input.

- **Frequency Synthesis:** Provided with an input clock signal, the DCM can generate a wide range of different output clock frequencies. This is accomplished by either multiplying and/or dividing the frequency of the input clock signal by various different factors.

- **Phase Shifting:** The DCM provides the ability to shift the phase of all its output clock signals with respect to its input clock signal.

The schematic of DCM block is shown in below figure,

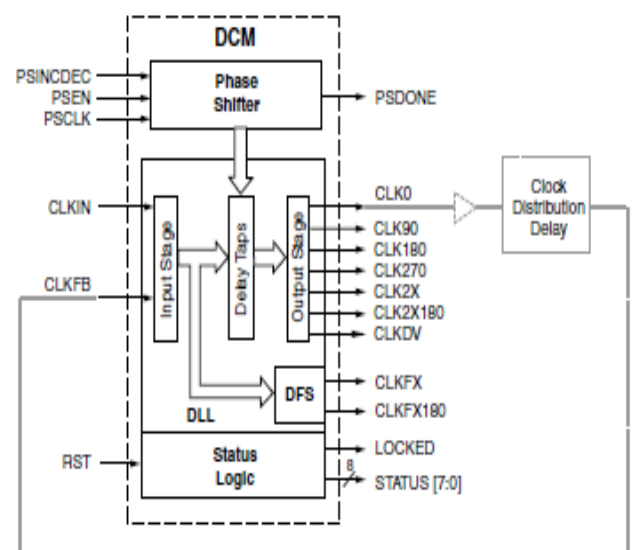


Figure 1: DCM Functional blocks and associated signals. [8].

III. High-Resolution DPWM architecture using DCM block:

The key of this architecture is the on-chip DCM block provided in almost every state of the art FPGA. The following DCM clock management features [9] will be used.

1) Phase shifting: The DCM provides four phase-shifted clock signals derived from the source clock CLKIN. In addition to CLK0 for zero-phase alignment to the CLKIN signal, the DCM also provides the CLK90, CLK180, and CLK270 outputs for 90°, 180°, and 270° phase-shifted signals, respectively. Besides, all the outputs of the DCM can be phase shifted with finer resolution.

2) Frequency synthesis: The DCM can generate a wide range of output clock frequencies (CLKFX output port), performing clock frequency division and multiplication. Besides phase shifting, the DCM is able to condition the clock input CLKIN in order to obtain clock outputs with 50% duty cycle. The clock feedback signal CLKFB is used to compare and lock the output signals with the input CLKIN signal. The fine phase shifting can be fixed (specified at design time and set during the FPGA configuration process) or variable. It is set by means of the DCM attribute PHASE_SHIFT, an integer in the range [-255, +255]. Below figure shows the fine phase shift effects in the fixed mode of operation. A phase-shifted output with a resolution of $(1/256)^{\text{th}}$ of the input clock period can be obtained. The variable phase-shifting feature has been used in [10]. However, this operating mode requires several clock cycles to change the duty cycle, degrading the dynamic performance. Besides, an asynchronous circuit is used to divide the clock cycle into four quadrants as CLK0, CLK90, CLK180 and CLK270.

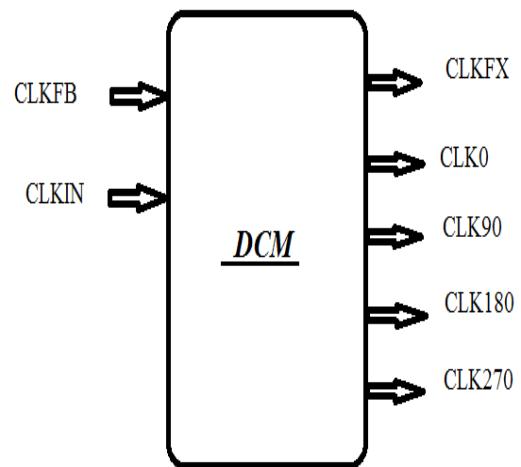


Figure 2: Simplified pinout description of DCM block.

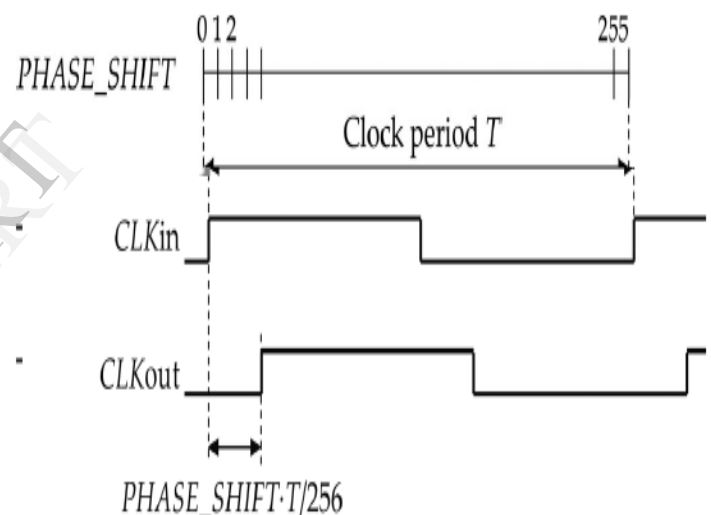


Figure 3: Fixed fine phase shifting effect.

• Detail Block Diagram of Proposed system:

Below figure 4 shows the detailed block diagram of the proposed system.

The first block in this system is DCM block which is present on almost all FPGA kit. It acts as an onchip clock manager block. Spartan-3 devices provide flexible, complete control over clock frequency, phase shift and skew through the use of the DCM feature.

To accomplish this, the DCM employs a Delay-Locked Loop (DLL), a fully digital control system that uses feedback to maintain clock signal characteristics with a high degree of precision despite normal variations in operating temperature and voltage.

Various quadrant phase shifted output of DCM is given as input to multiphase circuit. The multiphase circuit makes use of D-ff and multiplexer circuit to generate RESET signal which is then given to SR-ff to generate a PWM output.

The next block is PWM generator block which makes use of counter, comparator and D-ff to generate SETD, CLR D and SET signals. We can generate PWM output by making use of SET signal and RESET signal (which is output of multiphase circuit).

The generated PWM signals are then transmitted to a Drive circuit which then controls the external hardware. The hardware may consist of circuitry whose functioning is depends on PWM. The hardware circuitry may consists speed controlling of DC motor, Inverter or other power electronic devices which can controlled by PWM. By proper design of PWM we can consume very less power and it may help in power saving application.

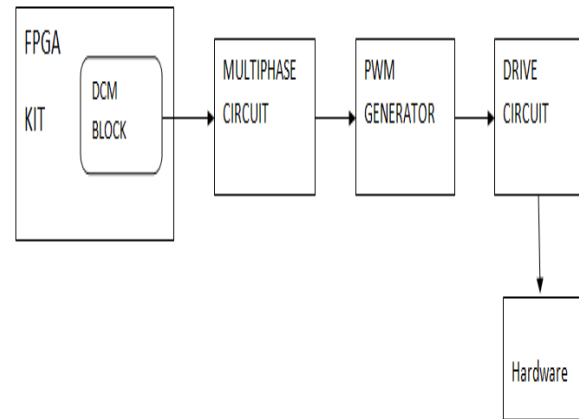


Figure 4: System block diagram.

IV. DCM-based HRPWM approach.

In order to introduce the proposed DCM-based high resolution DPWM architecture, the following architecture can be implemented, which is shown in below figure (i.e. figure 5). In this the quadrant phase-shifted outputs of a single DCM are used.

The duty cycle command $dc(m:0)$ has $m+1$ bits, ranging from m to 0 , where m is most significant bit of duty cycle command, and the counter "CNT" has $m-1$ bits. "CLR D" signal is set when the $m-1$ most-significant bits (MSBs), $dc(m:2)$, are equal to CNT; and SETD signal is set when CNT is equal to zero and $dc(m:2)$ is different from zero.

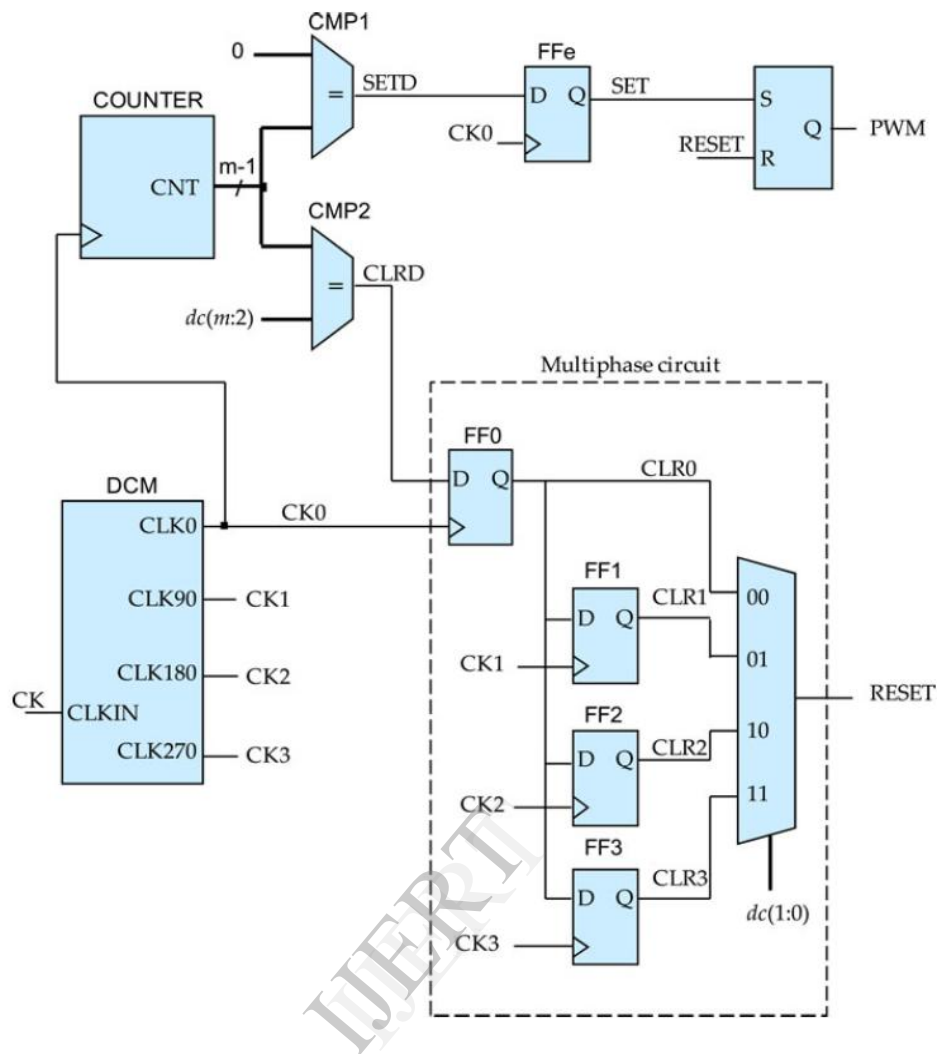


Figure5. DCM -based HRPWM first approach.

Figure 6 shows how the circuit works with $m = 4$, and $dc = "10010"$. Basically, when the counter CNT is equal to the $m-1$ MSBs of the duty command dc , signal CLR0 activates. The resulting pulse is captured in the next clock cycle by FF0, and phase shifted 90° , 180° , and 270° by flip-flops FF1, FF2, and FF3, respectively. These four FFs implement a multiphase synchronous circuit [11]. The two least-significant bits (LSBs) of the duty command are used by the multiplexer to select the phase-shifted signal that clears the SR latch. The advantage of this proposal in relation to others is that the digital circuit that generates the reset of the

SR latch is synchronous. The use of asynchronous circuits to reset the latch makes harder to calculate timing using static timing analysis and can result in glitching since controlling the logic and routing delays in an FPGA is more difficult than in ASIC implementations. We can improve an above shown architecture in order to improve the HRPWM resolution. For the improvement of resolution of PWM certain relationship has to be maintaining between total numbers of different components of circuit. This relation is explained in below section.

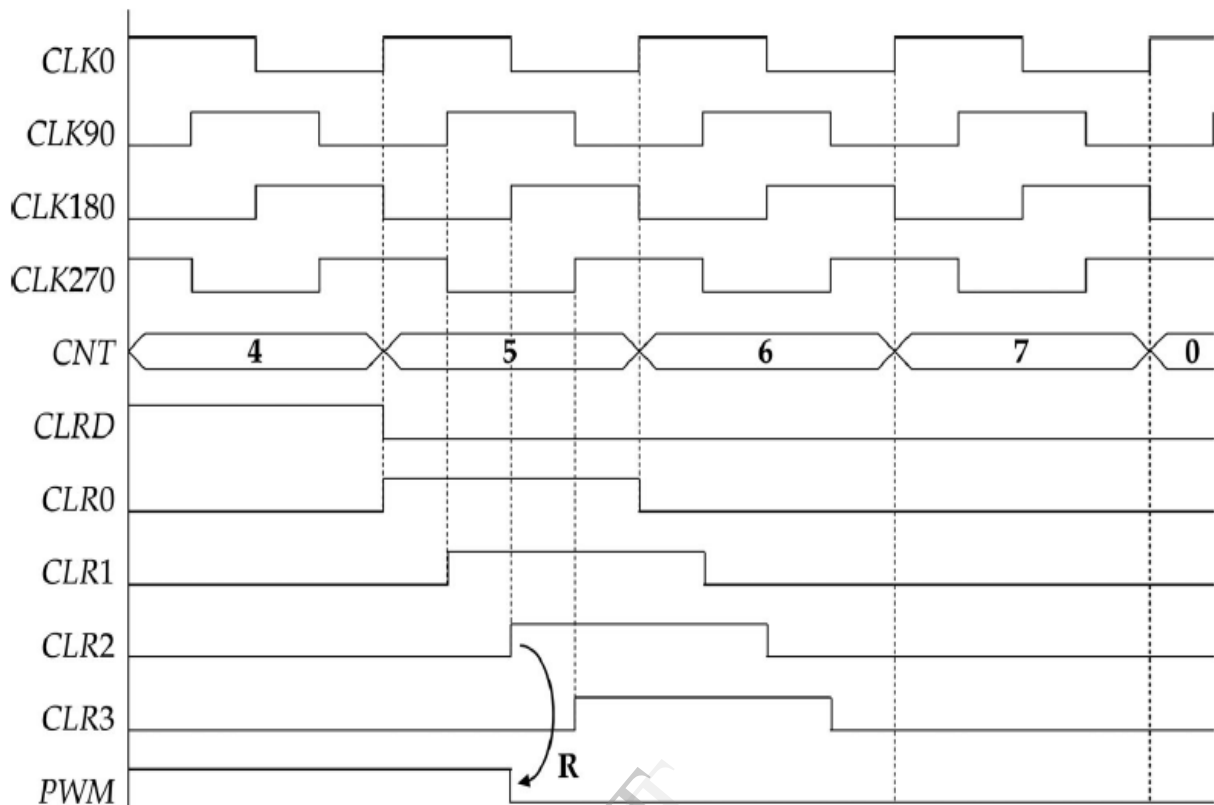


Figure 6: DCM-based HRPWM operation with $dc = "10010."$

V. Generalisation of DCM based architecture:

The previous architecture can be scaled to enhance the HRPWM resolution. Let $n = m+k$ be the bits of the duty cycle command dc , with $k \geq 2$. Basically, the proposed circuit is made up of a synchronous m -bit counter, r DCMs, $p = 4 \times r$ edge-triggered flip-flops, a p -to-1 multiplexer, and an SR latch whose output is the PWM signal. The modulus of the counter is configurable. The CLR_D signal is set when the counter is equal to the m MSBs of dc . The SET_D signal is set when the counter is zero and dc is different from zero. These signals are used to generate the SET and RESET signals that control the SR latch.

The counter and all DCMs are clocked by the same input clock signal "CK." Quadrant phase-shifted outputs CLK₀,

CLK₉₀, CLK₁₈₀, and CLK₂₇₀ of DCMs are used to generate a set of p phase-shifted clocks $\{CK_i\}$ with $0 \leq i < p$. All clock signals CK_i have the same period TCK with 50% duty cycle. CK_i is phase-shifted TCK/p time with respect to CK_{i-1} . The fine phase shifting in the fixed mode shifts the phase of all DCM output signals by a fixed fraction of the input clock period. Being the minimum phase shift $1/256$ of TCK ($k \leq 8$), the phase-shift value for DCM _{j} must be set to $j \times 64/r$ with $0 \leq j < r$.

The p flip-flops implement a multiphase synchronous circuit. FF_i is triggered by the rising edge of CK_i . A p -to-1 multiplexer uses the k LSBs of dc to select the CLR _{i} signal that clears the SR latch. CLR _{i} is delayed by a fraction $1/p$ of TCK with respect to CLR _{$i-1$} . In order to improve speed, the circuit is designed, such as the minimum allowable delay for

paths, in which the source and destination clocks are different, is $TCK/2$, regardless the phase number. By doing so, the maximum clock frequency is not limited by the multiphase circuit but for the DCM, and it can be easily scaled to the required p number.

For a particular FPGA series, the value of p is constrained by the number of DCM blocks available, the number of global clock lines that each DCM block can drive up, and the need to ensure that the routing delay of the multiplexer inputs is less than TCK/p for a monotonic behaviour.

VI. Implementation:

This section describes an implementation example carried out to show the feasibility

of the DCM-based HRPWM architecture proposed in this study. As the implementation depends on the FPGA, let assume that the high-resolution DPWM is implemented in the Xilinx XC3S100E Spartan-3E FPGA of the S-3E Starter Kit board by Digilent. This board includes a 50-MHz clock oscillator that is used as the input clock. As the FPGA has four DCMs, the parameter k can be up to 4.

As an example, Fig. 7 shows an implementation with $m = 8$, and $k=3$. DCMx4 multiplies its input clock frequency by 4. The CLKFX output of DCMx4 is connected to the input clock of the counter, DCM0 and DCM1.

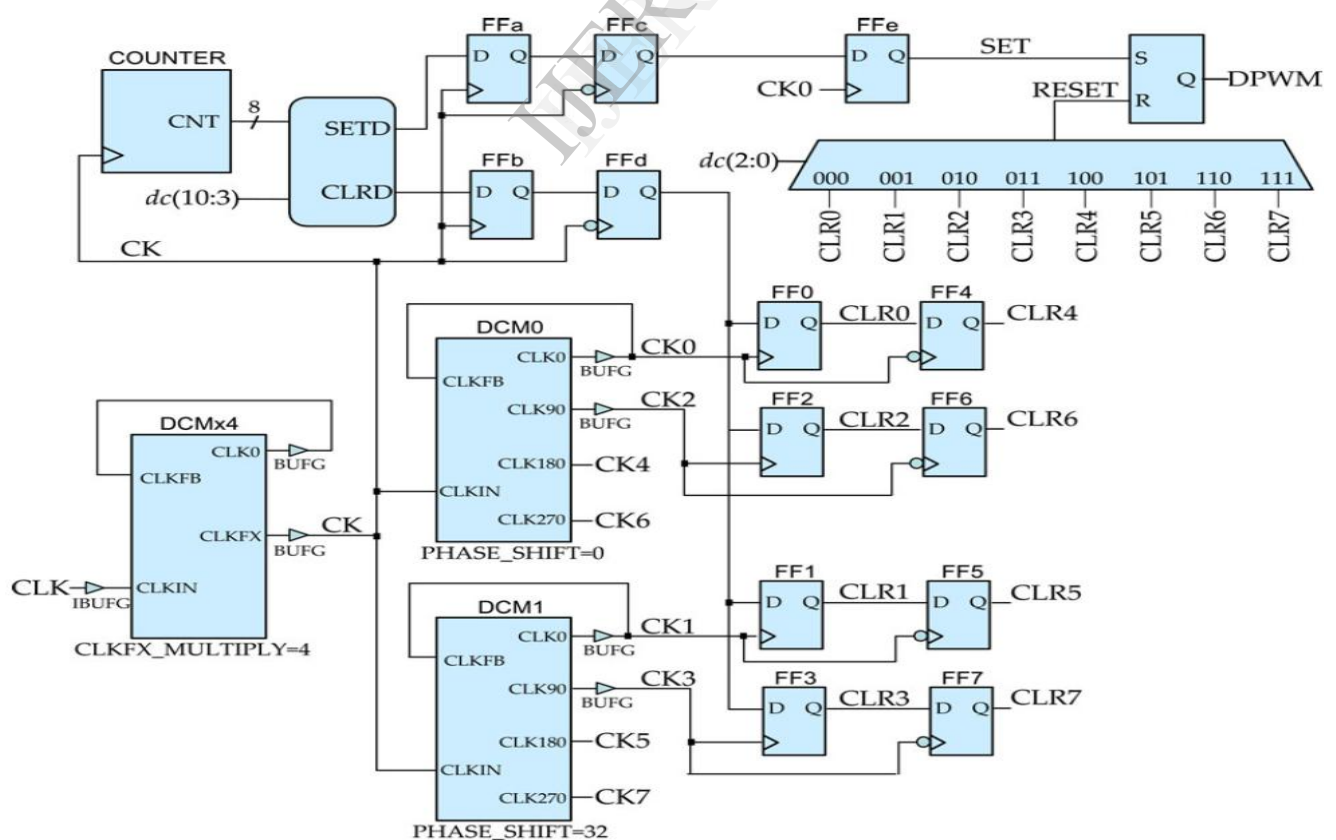


Figure 7: Implemented high-resolution DPWM with $m = 8$ and $k = 3$.

The binary counter has 8 bits, and SETD and CLR0 signals are generated from the counter output and the eight MSBs of dc as explained earlier. FFa and FFb store these signals. Negative edge-triggered flip-flops FFc and FFd avoid malfunctions due to the phase offset between CK and CK0 (± 200 ps max. according to the data sheet).

DCM0 and DCM1 generate eight phased clocks {CK0, . . ., CK7}. PHASE-SHIFT attribute of DCM0 is set to 0. DCM0 generates clocks CK0, CK2, CK4, and CK6. PHASE-SHIFT attribute of DCM1 is set to 32, and its outputs are shifted 32/256 of TCK. DCM1 generates clocks CK1, CK3, CK5, and CK7. In the implementation step of the design flow, DCM0 and DCM1 are manually placed at DCM_X0Y0 and DCM_X1Y0, respectively, in order to be close to each other and reduce routing delays. These two DCMs can drive up to four global clock lines. Then, the circuit must work with the rising and falling edges of only four phased clocks {CK0, CK1, CK2, CK3}, and FF4, FF5, FF6, and FF7 must be negative-edge triggered. This introduces nonlinearity in the on-time step due to duty-cycle variation but this effect cannot be solved due to the routing architecture of this FPGA.

The maximum clock frequency required for this type of implementation is limited to 200 MHz, which is the maximum operating frequency for the CLK90 and CLK270 DCM outputs according to the FPGA datasheet [8]. However, it is important to note that if there were paths in the implementation in which the difference between active clock edges of source and destination flip-flops were lower than the one present in this design ($TCK/2$), the timing constraint would be more restrictive than the one expressed in (2) and the maximum clock frequency would be reduced. For instance, a clock difference of $TCK/4$, as it occurs in Figure 3, would lead to the 168-MHz

maximum operating frequency. In this case, the multiphase circuit would limit the operation instead of making the most of the FPGA DCM resources.

VII. Results:

The proposed system is implemented on Spartan 3E family of FPGA (XC developed by Xilinx). The testing of final results are done on Xilinx software. For the proposed system the PWM variation is totally based on value of 'dc'. Below figure shows some outputs according to variation of value of dc(12:0).

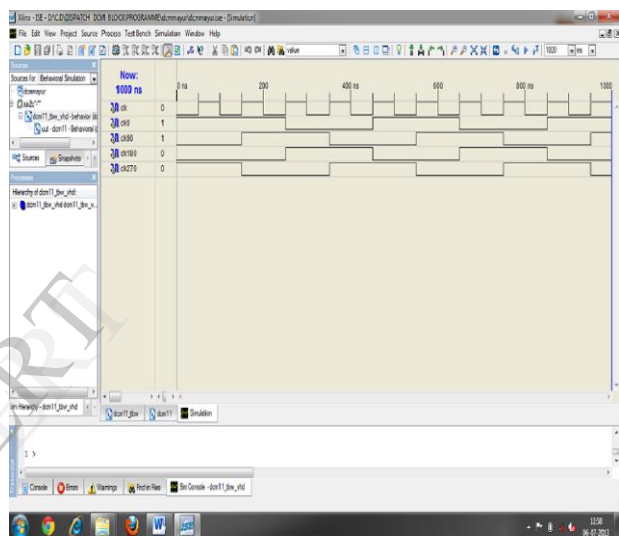


Figure 8: Quadrant phase shifted output.

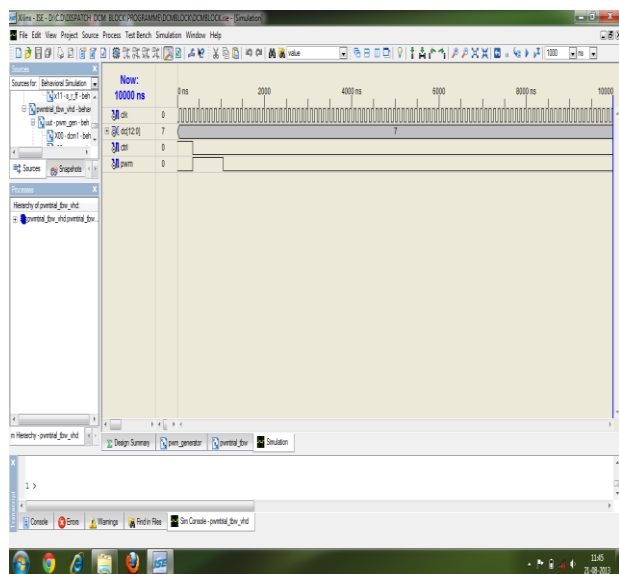


Figure 9: PWM waveform for dc=000000000011

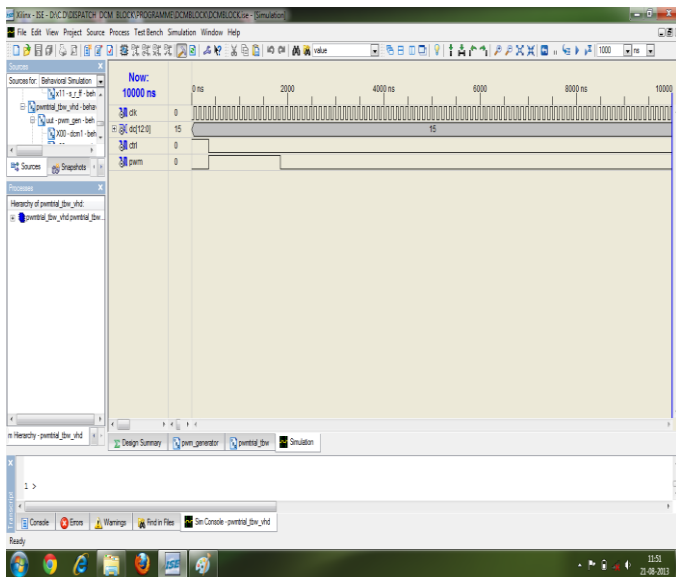


Figure 10: PWM waveform for dc=000000001011

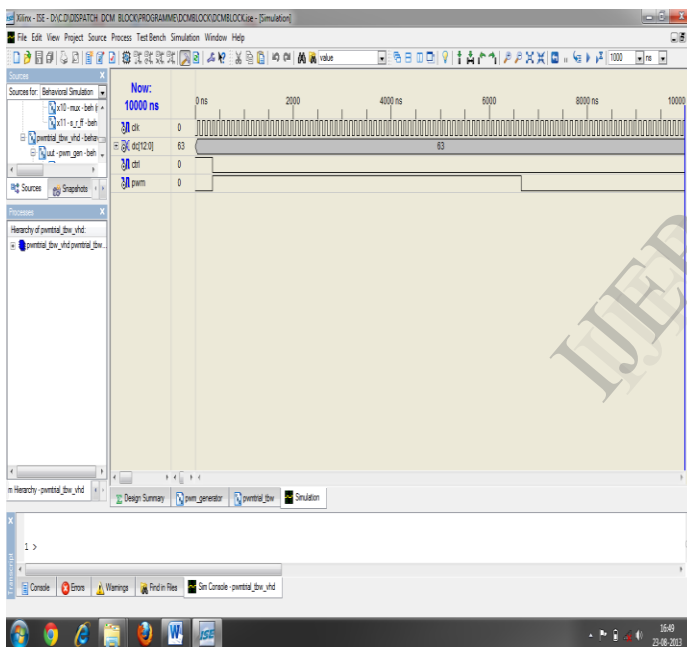


Figure 11: PWM waveform for dc=0000000111011.

VIII. Conclusion:

To make the development in power Electronics and Digital Electronics field, the development in resolution of DPWM's is necessary. These high resolution DPWM's are used in high frequency and high precision power convertors. In this paper, we have proposed a fully synchronous HRPWM implementations using different FPGA resource i.e. the DCM block. The DCM-based architecture

is implemented using the resources present in low-cost FPGAs, and the maximum clock frequency is determined by the DCMs. These solutions are complementary and cover a wide spectrum of cost/performance applications.

The proposed DCM-based synchronous architectures have been implemented on a Xilinx Spartan-3E.

IX. References:

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