Design 16-bit CMOS Digitally Controlled Oscillator

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***Abstract*— In this paper, a new differential delay cell has been proposed and 16-bit Digital Controlled Oscillator is designed. The 16 bit DCO consist of 4-stage of differential delay cell in ring string and a digital control scheme is used to improved noise characteristics. The structure of the DCO utilizes dual delay path techniques to achieve high oscillation frequency and a wide tuning range. The proposed DCO circuits have been simulated in SPICE with 0.35 µm and 0.5 µm technologies operating at supply voltage of 3.5 V and 5 V respectively. CMOS DCO using 0.35 µm and 0.5 µm parameters achieves a controllable frequency range of [1.9512-4.4239] GHz and [1.7324-4.8649] GHz with a tuning range of 2.4727 GHz (≈56%) and 3.1325 GHz (≈64%). The range of measured output noise is -176.562 to -181.979 dB/Hz and -173.565 to 180.463dB/Hz with the variation of controlled word from 'FFFFH' to '0000H' in 0.35 µm and 0.5 µm respectively.**

Keywords- CMOS, digital controlled oscillator, Dual delay path technique, pll, voltage controlled oscillator.

I. INTRODUCTION

With the growing density of component in submicron technology, the need for high operating speed and low power is increased. With rising electronic computing power of very large scale integration (VLSI) system such as laptops, cell phones etc. the need for high frequency operation in such system has rapidly increased.

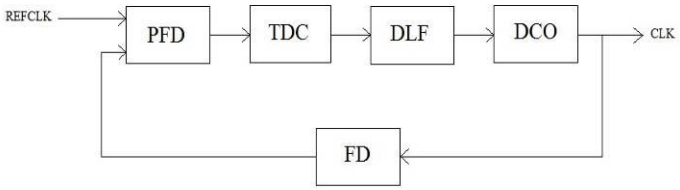


Figure 1. Block diagram of a ADPLL

In order to afford such high performance circuits the functional block such as clock recovery and clock generator must operate at high frequency. Digital phase locked loop are widely used in many Communication System to clock and data recovery. As shown in figure 1 the ADPLL consists of five blocks: a phase frequency detector (PFD), a time to digital convertor (TDC), a digital loop filter (DLF), a DCO and a frequency divider (FD). Digital controlled oscillator (DCO) is most critical block in ADPLL. To implement a wide frequency range ADPLL, the DCO must have a wide oscillation frequency range. Digital controlled oscillators (DCO's) have been recently widely used in frequency synthesis and clock recovery due to accurate frequency locking and stability in operation as compared to analog counter parts. This is achieved either through charging MOSFET driving strength or fine tuning capacitive loading [1]. The design topology of most DCO's are based on inverter based ring oscillators [2], and these suffer from the phase noise and reduce their effectiveness in communication system. A low noise, 900 MHz, voltage controlled oscillator (VCO) fabricated in a 0.6 µm CMOS technology using a differential delay cell with 450 MHz (≈50%) tuning range operating in the range of 750 MHz to 1.2 GHz [3]. In this paper, 16-bit DCO design using differential delay cell in 0.35 & 0.5 µm CMOS process technology have been presented. This design used the differential delay cell along with 16-bit digital control word and provides controllable frequency range of [1.9512-4.4239] GHz and [1.7324-4.8649] GHz with a tuning range of 2.4727 GHz (≈56%) & 3.1325 GHz (≈64%).

The paper is organized as: Section II, represents the detail circuit of proposed differential delay cell and dual delay path technique. In section III the results of DCO have been obtained and compared. Finally conclusions have been presented in section IV.

II. DCO CIRCUITS

A. DCO design with differential delay cell:

Figure 2 shows a four input differential delay cell. The cell can be divided into three sub-blocks; the differential input block, the CMOS Latch block and the acceleration block. The differential input block is composed of two NMOS transistors M5 and M6 and it is used to accept the signal which comes from the Digital Loop filter, the block of ADPLL.

A pair of PMOS Load transistor M1 and M4 is used to constitute a CMOS latch block. The strength of Latch block is controlled by the digital bits of pass transistor band implemented by two sets of Parallel MOSFET switches for the two feedback path by a 16-bit control register. The CMOS latch block is major block in the delay cell and its strength will affect the oscillation frequency. A pair of PMOS transistor M2 and M3 is added to PMOS load of the delay cell which is act as an acceleration block. Acceleration block is speed up the oscillation frequency and reduce the noise.

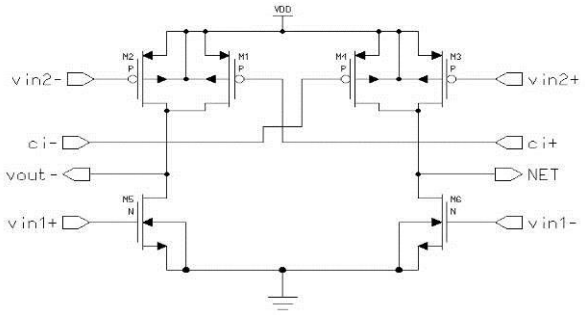


Figure 2. The four input differential delay latch cell for digitally controlled oscillator (DCO)

B. High Speed DCO with Dual Delay Path

In the conventional ring oscillator, the oscillation frequency is determined as:

$$F_{osc} = 1/2N\tau \qquad (1)$$

Here F_{osc} is the oscillation frequency. N is the number of stages and τ is the unit delay time of a delay cell. Therefore the frequency of oscillator is depending on delay time of one delay element. The delay time cannot be smaller than that of a single inverter; so the maximum frequency of the oscillator is limited by the delay time of the basic inverter delay cell. To overcome this frequency limitation problem, skewed delay scheme is used [3][4]. Figure 3 shows the DCO structure with dual delay path technique. In the same DCO, the skewed delay paths and normal delay paths existed and to construct the dual delay path scheme. The DCO uses the even stage skewed dual delay path scheme which enable higher operating frequency and wider tuning range. The skewed signal is taken from outputs of two stages before the current delay cell. This skewed signal turn on the PMOS prematurely during output transition. This compensate for the performance of PMOS which is usually slower than NMOS. The output node of the delay cell will be pre charged by the PMOS transistor M3 or M4. As a result, the output node can charge to high voltage faster and can obtain higher operating frequency. This technique reduced the rise time of the output signal and contributes to reducing the phase noise of the overall oscillation [3][4]. When the skewed signal increases, the speed and power consumption also increase when the skew is excessive, speed is reduced because most of current flow directly from the power supply of ground. For practical applications, skewed should be small compared with the total period to get higher speeds with allowable power consumption penalty [4]. In figure 3, the normal delay paths are shown by thick lines and skewed path are represented as thin lines.

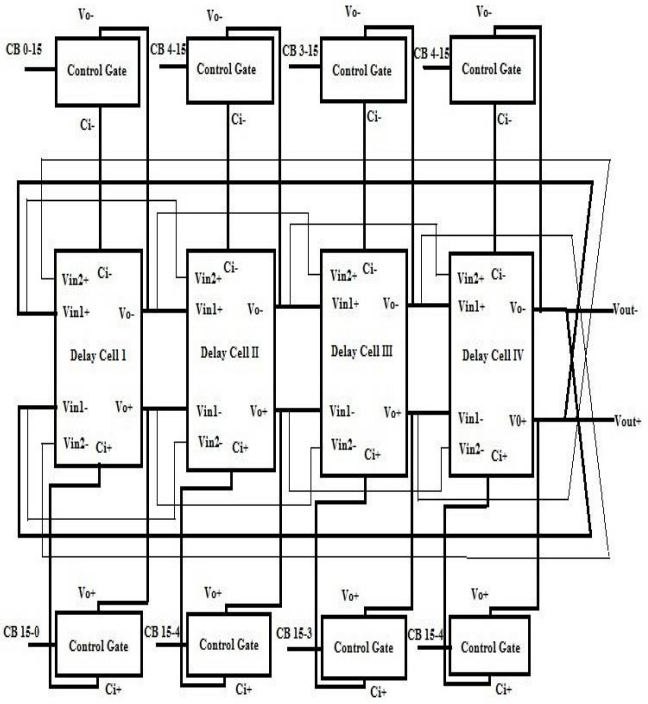


Figure 3. DCO structure with dual delay path scheme.

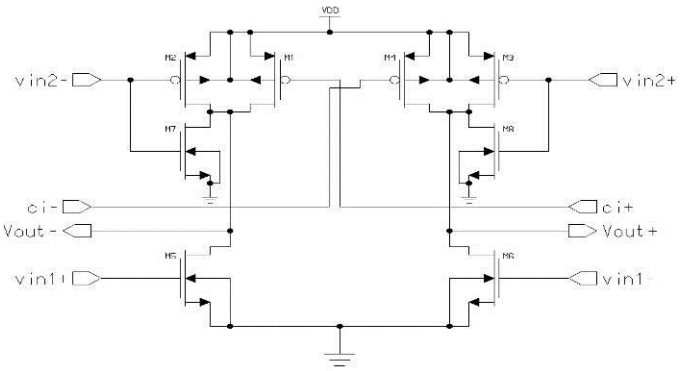


Figure 4. The proposed four input differential delay latch cell for digitally controlled oscillator (DCO).

Figure 4 shows the proposed delay cell. In the purposed delay cell, modified the acceleration block and allowed the output node discharge faster. A pair of NMOS M7 and M8 is added to the acceleration block. They are used to pre discharge the output nodes. Consequently the acceleration block can reduce the rise time, even fall time of the output. Due to the effect of pre-discharge, the oscillation frequency of the new delay cell is higher than conventional delay cell. Figure 5 shows the detailed DCO Design using a 4-stage ring of proposed differential delay cell.

The range of measured output noise is -176.562 to -181.979 dB/Hz and -173.565 to 180.463dB/Hz with the variation of controlled word from 'FFFFH' to '0000H' in 0.35 µm and 0.5 µm respectively. These simulation results show the speed performance of the proposed DCO is better than conventionalDCO.

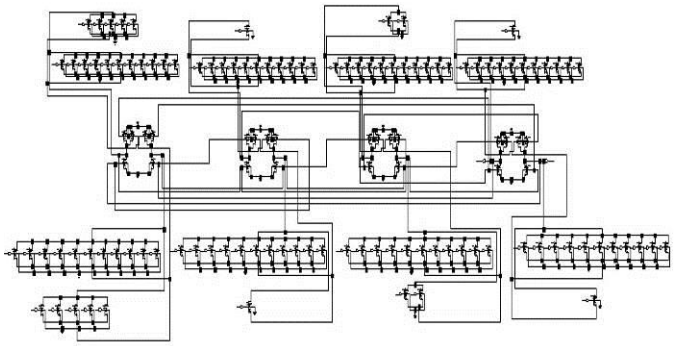


Figure 5

III. RESULTS AND DISCUSSIONS

The 16-bit digital controlled oscillator (DCO) has been simulated using Spice in 0.35 and 0.5 µm (micrometer) technologies with supply voltage of 3.5V and 5V respectively. Table 1 and 2 shows the impact of each control bit on the output frequency of 16-bit DCO structure. The frequency range of [1.9512-4.4239] GHz and [1.7324-4.8649] GHz with a tuning range of 2.4727 GHz (≈56%) and 3.1325 GHz (≈64%) is achieved in 0.35 and 0.5 µm technologies. Figure 6 & 7 shows the relationship between control word and output frequency. The output waveform of 16-bit DCO's are shown in figure 8 and 9. It has been observed from the results that with decrease in control bits the output frequency increased and output noise decreased.

Control bits				Conventional DCO	Proposed DCO
CB12-15	CB 8-11	CB 4-7	CB 0-3	Frequency (GHz)	Frequency (GHz)
F	F	F	F	1.7787	1.9512
F	F	3	3	1.7838	1.9545
F	0	0	0	1.8226	1.9923
D	0	0	0	1.8846	2.0659
C	0	0	0	1.9214	2.1017
A	8	8	8	1.9717	2.1587
A	8	0	0	1.9743	2.1623
A	4	0	0	1.9830	2.1725
9	0	0	0	2.0341	2.2278
6	6	6	6	2.1470	2.3559
5	5	0	0	2.2078	2.4248
5	1	0	0	2.2236	2.4421
4	8	0	0	2.2576	2.4827
4	5	0	0	2.2706	2.4987
3	8	0	0	2.3324	2.5752
1	5	1	2	2.8942	3.0495
0	0	0	0	4.0345	4.4239

Table 1 16-bit DCO Impact of control bit on output frequency in 0.35 µm technology

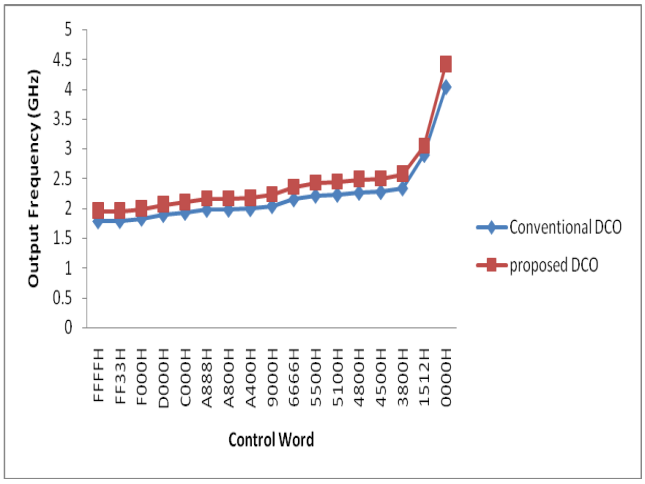


Figure 6 Relationship between output frequency and control word.

Control bits				Conventional DCO	Proposed DCO
CB12-15	CB 8-11	CB 4-7	CB 0-3	Frequency (GHz)	Frequency (GHz)
F	F	F	F	1.5672	1.7324
F	F	3	3	1.5692	1.7335
F	0	0	0	1.6073	1.7758
D	0	0	0	1.7012	1.8792
C	0	0	0	1.7516	1.9353
A	8	8	8	1.8386	2.0304
A	8	0	0	1.8397	2.0323
A	4	0	0	1.8552	2.0482
9	0	0	0	1.9350	2.1368
6	6	6	6	2.1468	2.3756
5	5	0	0	2.2589	2.5001
5	1	0	0	2.2836	2.5292
4	8	0	0	2.3516	2.6088
4	5	0	0	2.3829	2.6460
3	8	0	0	2.5312	2.8153
1	5	1	2	3.4821	3.8913
0	0	0	0	4.4916	4.8649

Table 2 16-bit DCO Impact of control bit on output frequency in 0.5 µm technology

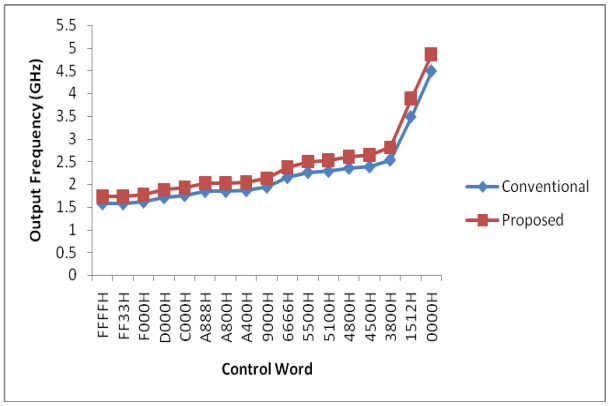
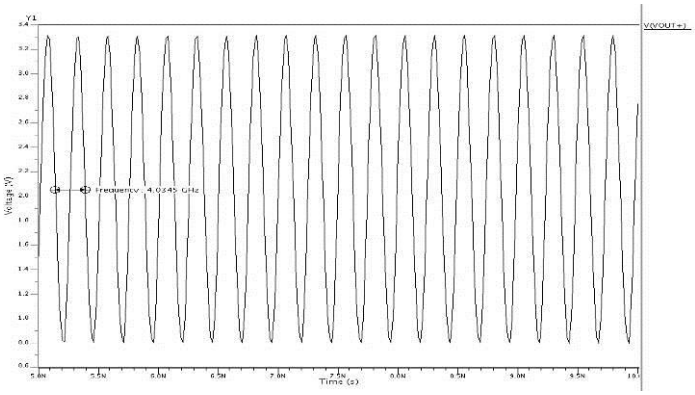
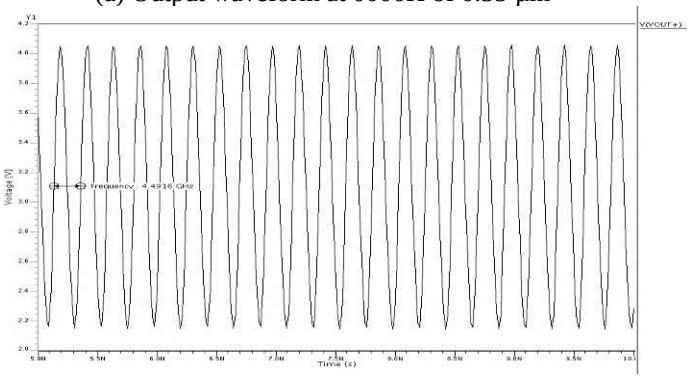


Figure 7 Relationship between output frequency and control word.

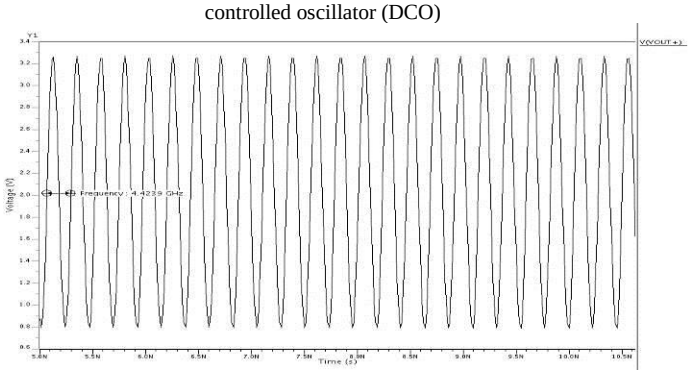


(a) Output waveform at 0000H of 0.35 µm

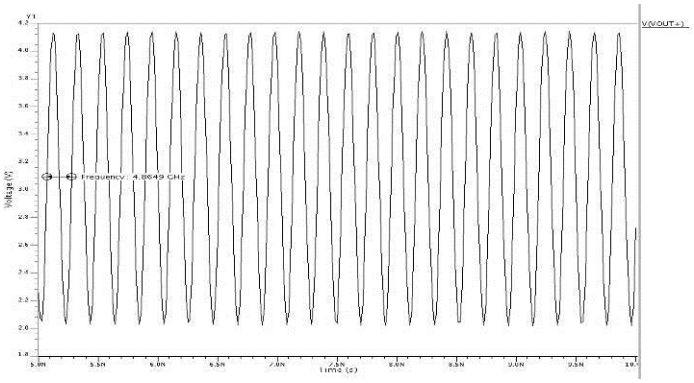


(b) Output waveform at 0000H of 0.5 µm

Figure 8. (a)-(b) Output waveform for 16-bit conventional digital controlled oscillator (DCO)



(a) Output waveform at 0000H of 0.35 µm



(b) Output waveform at 0000H of 0.5 µm

Figure 9. (a)-(b) Output waveform for 16-bit proposed digital controlled oscillator (DCO)

IV. CONCLUSIONS

In this paper, a new 16-bit DCO was designed with differential delay cell. In new differential delay cell, a pair of NMOS transistor is added to acceleration block which reduce rise time and fall time of output signal. This increases the oscillation frequency and reduces the output noise of DCO. DCO circuits have been designed in Spice with 0.35µm and 0.5µm technologies with supply voltage of 3.5V and 5V respectively. CMOS DCO using 0.35 µm and 0.5 µm parameters achieves a controllable frequency range of [1.9512-4.4239] GHz and [1.7324-4.8649] GHz with a tuning range of 2.4727 GHz (≈56%) and 3.1325 GHz (≈64%). The range of measured output noise is -176.562 to -181.979 dB/Hz and -173.565 to 180.463dB/Hz with the variation of controlled word from 'FFFFH' to '0000H' in 0.35 µm and 0.5 µm respectively. The proposed DCO shows the features of wider operating frequencies and lower output noise for high frequency application.

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