Design & Analysis of full adders using adiabatic logic

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Abstract: In this paper we are going to compare the adiabatic logic designs & designing a new full adder using ECRL & PFAL logics after that the simulations were done using Microwind & DSCH. Thus the efficiency of the circuits are shown & compared using different nano meter technologies.

Keywords: Adiabatic, ECRL Adder, PFAL Adder, Full adder, Low Power Adders,

I. Introduction:

The main objective of this thesis is to provide new low power solutions for Very Large Scale Integration (VLSI) designers. Especially, this work focuses on the reduction of the power dissipation, which is showing an ever-increasing growth with the scaling down of the technologies. Various techniques at the different levels of the design process have been implemented to reduce the power dissipation at the circuit, architectural and system level.

Furthermore, the number of gates per chip area is constantly increasing, while the gate switching energy does not decrease at the same rate, so the power dissipation rises and heat removal becomes more difficult and expensive. Then, to limit the power dissipation, alternative solutions at each level of abstraction are proposed.

The dynamic power requirement of CMOS circuits is rapidly becoming a major concern in the design of personal information systems and large computers. In this thesis work, a new CMOS logic family called *ADIABATIC LOGIC*, based on the adiabatic switching principle is presented. The term adiabatic comes from thermodynamics, used to describe a process in which there is no exchange of heat with the environment. The adiabatic logic structure dramatically reduces the power dissipation. The adiabatic switching technique can achieve very low power dissipation, but at the expense of circuit complexity. Adiabatic logic offers a way to reuse the energy stored in the load capacitors rather than the traditional way of discharging the load capacitors to the ground and wasting this energy.

This thesis work demonstrates the low power dissipation of Adiabatic Logic by presenting the results of designing various design/ cell units employing Adiabatic Logic circuit techniques. A family of full-custom conventional CMOS Logic and an Adiabatic Logic units for example, an inverter, a two-input NAND gate, a two-input NOR gate, a two-input XOR gate, a two-to-one multiplexer and a one-bit Full Adder were designed in Mentor Graphics IC Design Architect using standard TSMC 0.35 μm technology, laid out in Microwind IC Station.

All the circuit simulations has been done using various schematics of the structures and post-layout simulations are also being done after they all have been laid-out by considering all the basic design rules and by running the LVS program. Finally, the analysis of the average dynamic power dissipation with respect to the frequency and the load capacitance was done to show the amount of power dissipated by the two logic families.

II. Motivation:

In the past few decades ago, the electronics industry has been experiencing an unprecedented spurt in growth, thanks to the use of integrated circuits in computing, telecommunications and consumer electronics. We have come a long way from the single transistor era in 1958 to the present day ULSI (Ultra Large Scale Integration) systems with more than 50 million transistors in a single chip.

The ever-growing number of transistors integrated on a chip and the increasing transistor switching speed in recent decades has enabled great performance improvement in computer systems by several orders of magnitude. Unfortunately, such phenomenal performance improvements have been accompanied by an increase in power and energy dissipation of the systems. Higher power and energy dissipation in high performance systems require more expensive packaging and cooling technologies, increase cost, and decrease system reliability. Nonetheless, the level of on-chip integration and clock frequency will continue to grow with increasing performance demands, and the power and energy dissipation of high-performance systems will be a critical design constraint.

For example, high-end microprocessors in 2010 are predicted to employ billions of transistors at clock rates over 30GHz to achieve TIPS (Tera Instructions per seconds) performance [1]. With this rate, high-end microprocessor's power dissipation is projected to reach thousands of Watts. This thesis investigates one of the major sources of the power/energy dissipation and proposes and evaluates the techniques to reduce the dissipation.

Digital CMOS integrated circuits have been the driving force behind VLSI for high performance computing and other applications, related to science and technology. The demand for digital CMOS integrated circuits will continue to increase in the near future, due to its important salient features like low power, reliable performance and improvements in the processing technology.

The word *ADIABATIC* comes from a Greek word that is used to describe thermodynamic processes that exchange no energy with the environment and therefore, no energy loss in the form of dissipated heat. In real-life computing, such ideal process cannot be achieved because of the presence of dissipative elements like resistances in a circuit. However, one can achieve very low energy dissipation by slowing down the speed of operation and only switching transistors under certain conditions. The signal energies stored in the circuit capacitances are recycled instead, of being dissipated as heat. The adiabatic logic is also known as *ENERGY RECOVERY CMOS* .

It should be noted that the fully adiabatic operation of the circuit is an ideal condition which may only be approached asymptotically as the switching process is slowed down. In most practical cases, the energy dissipation associated with a charge transfer event is usually composed of an adiabatic component and a non-adiabatic component. Therefore, reducing all the energy loss to zero may not possible, regardless of the switching speed. With the adiabatic switching approach, the circuit energies are conserved rather than dissipated as heat. Depending on the application and the system requirements, this approach can sometimes be used to reduce the power dissipation of the digital systems.

Here, the load capacitance is charged by a constant-current source (instead of the constant-voltage source as in the conventional CMOS circuits).
Here, R is the resistance of the PMOS network. A constant charging current corresponds to a linear voltage ramp. Assume, the capacitor voltage V_C is zero initially.

III. Adiabatic Logic Gate:

In the following, we will examine simple circuit configurations which can be used for adiabatic switching. Figure 3.2 shows a general circuit topology for the conventional CMOS gates and adiabatic counterparts. To convert a conventional CMOS logic gate into an adiabatic gate, the pull-up and the pull-down networks must be replaced with complementary transmission-gate (T-gate) networks. The T-gate network implementing the pull-up function is used to drive the true output of the adiabatic gate, while the T-gate network implementing the pull-down function drives the complementary output node. Note that all the inputs should also be available in complementary form. Both the networks in the adiabatic logic circuit are used to charge-up as well as charge-down the output capacitance, which ensures that the energy stored at the output node can be retrieved by the power supply, at the end of each cycle. To allow adiabatic operation, the DC voltage source of the original circuit must be replaced by a pulsed-power supply with the ramped voltage output.

IV. Adiabatic Logic Types:

Practical adiabatic families can be classified as either PARTIALLY ADIABATIC or FULLY ADIABATIC [12]. In a PARTIALLY ADIABATIC CIRCUIT, some charge is allowed to be transferred to the ground, while in a FULLY ADIABATIC CIRCUIT, all the charge on the load capacitance is recovered by the power supply. Fully adiabatic circuits face a lot of problems with respect to the operating speed and the inputs power clock synchronization.

ECERL-Efficient Charge Recovery Logic:

Efficient Charge – Recovery Logic (ECRL) proposed by Moon and Jeong [13], shown in Figure 4.1, uses cross-coupled PMOS transistors. It has the structure similar to Cascode Voltage Switch Logic (CVSL) with differential signaling.

It consists of two cross-coupled transistors *M1* and *M2* and two NMOS transistors in the

An AC power supply *pwr* is used for ECRL gates, so as to recover and reuse the supplied energy. Both *out* and */out* are generated so that the power clock generator can always drive a constant load capacitance independent of the input signal. A more detailed description of ECRL can be found in. Full output swing is obtained because of the cross-coupled PMOS transistors in both precharge and recover phases. But due to the threshold voltage of the PMOS transistors, the circuits suffer from the non-adiabatic loss both in the precharge and recover phases. That is, to say, ECRL always pumps charge on the output with a full swing. However, as the voltage on the supply clock approaches to

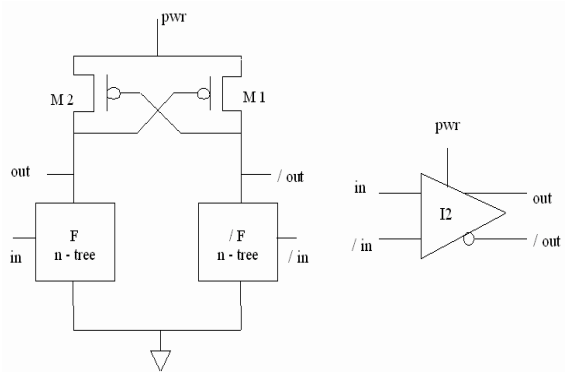


Figure1: The Basic Structure of the Adiabatic ECRL Logic.

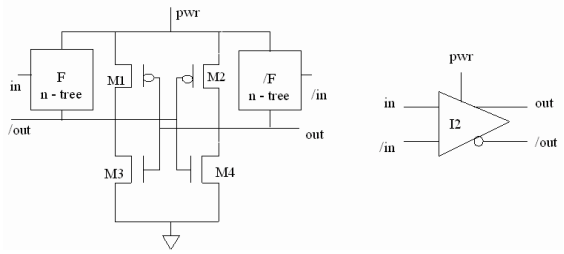
So the recovery path to the supply clock to the supply clock is disconnected, thus, resulting in incomplete recovery. V_{tp} is the threshold voltage of PMOS transistor. The amount of loss is given as

$$E_{ECRL} = C|V_{tp}|^2 / 2$$

Thus, from Equation (4.2), it can be inferred that the non-adiabatic energy loss is dependent on the load capacitance and independent of the frequency of operation.

V. Positive Feedback Adiabatic Logic:

The partial energy recovery circuit structure named Positive Feedback Adiabatic Logic (PFAL) [15] has been used, since it shows the lowest energy consumption if compared to other similar families, and a good robustness against technological parameter variations. It is a dual-rail circuit with partial energy recovery. The general schematic of the PFAL gate is shown in Figure 4.3. The core of all the PFAL gates is an adiabatic amplifier, a latch made by the two PMOS *M1-M2* and two NMOS *M3-M4*, that avoids a logic level degradation on the output nodes *out* and */out*. The two n-trees realize the logic functions. This logic family also generates both positive and negative outputs. The functional blocks are in parallel with the PMOSFETs of the adiabatic amplifier and form a transmission gate. The two n-trees realize the logic functions. This logic family also generates both positive and negative outputs.



The two major differences with respect to ECRL are that the latch is made by two PMOSFETs and two NMOSFETS, rather than by only two PMOSFETs as in ECRL logic, and that the functional blocks are in parallel with the transmission PMOSFETs. Thus the equivalent resistance is smaller when the capacitance needs to be charged. The energy dissipation by the CMOS Logic family and Adiabatic PFAL Logic family can be Seen.

VI. Adiabatic Full Adder using PFAL & ECRL:

A partially adiabatic logic family PFAL one-bit Full Adder block can be implemented as shown in the Figure 5.23 (for SUM block) and Figure 5.24 (for OUTPUT_CARRY) below, respectively.

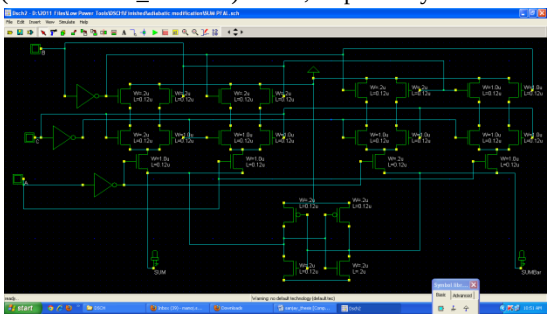


Figure4: PFAL Sum Circuit

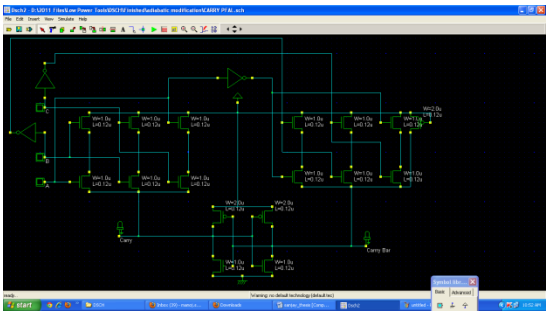


Figure5: PFAL Carry Circuit

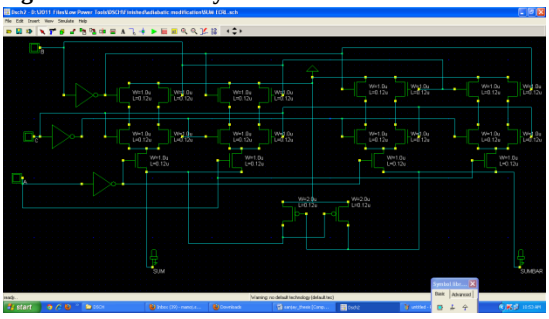


Figure6: ECRL SUM Circuit

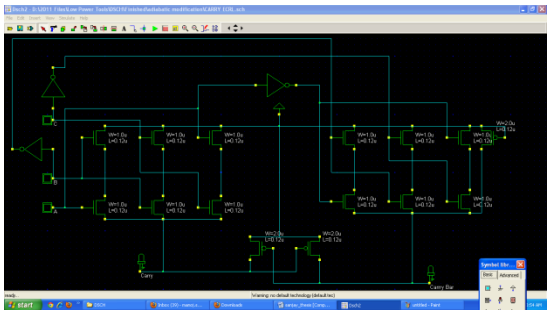


Figure7: ECRL Carry Circuit

VII. Conclusion

The thesis primarily was focused on the design of low power CMOS cell structures, which is the main contribution of this work. The design of low power CMOS cell structures uses fully complementary CMOS logic style and an adiabatic PFAL logic style. The basic principle behind implementing various design units in the two logic styles is to compare them with reference to the average power dissipated by all of them.

A family of full-custom conventional CMOS Logic and an Adiabatic Logic units were designed in Mentor Graphics IC Design Architect using standard TSMC 0.35 μm technology, layout them in Microwind & Digital Schematic and the analysis of the average dynamic power dissipation with respect to the frequency and the load capacitance was done. It was found that the adiabatic PFAL logic style is advantageous in applications where power reduction is of prime importance as in high performance battery-portable digital systems running on batteries such as note-book computers, cellular phones and personal digital assistants.

With the adiabatic switching approach, the circuit energies are conserved rather than dissipated as heat. Depending on the application and the system requirements, this approach can be used to reduce the power dissipation of the digital systems. With the help of adiabatic logic, the energy savings of upto 76 % to 90 % [15] can be reached.

Circuit simulations show that the adiabatic design units can save energy by a factor of 10 at 50 MHz and about 2 at 250 MHz, as compared to logically equivalent conventional CMOS implementation.

VIII. Future Work

(a) ADIAMEMS: To perform digital logic in CMOS in a truly adiabatic (asymptotically thermodynamically reversible) fashion requires that the logic transitions be driven by a quasi-trapezoidal (flat-topped) power-clock voltage waveform, which must be generated by a resonant element with very high *Q* (quality factor). Recently, MEMS resonators have attained very high frequencies and *Q* factors and are becoming widely used in communications system-on-chip (SOC) for RF signal filtering, amplification, etc.

(b) APPLICATION OF NANO-TECHNOLOGY: Carbon nano-tubes grown using Chemical Vapor Deposition (CVD) can be selected to conform to a spiraling shape. Thus, a good quality factor *Q* can be achieved. The work left to be done for this design would include a method for causing it to keep its form, since nano-tubes are typically not rigid. Also, putting the tube to use in a circuit would lower the effective *Q* due to the junction discontinuities.

(c) SPACECRAFT: The high cost-per-weight of launching computing-related power supplies, solar panels and cooling systems into orbit imposes a demand for adiabatic power reduction in spacecraft in which these components weigh a significant fraction of total spacecraft weight.

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