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Design and Analysis Of Cross Coupled Sense Amplifier Circuit For Srams

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***Abstract*— In present work, CMOS sense amplifier has been studied and their performance evolution in terms of sensing delay and power has been carried out. The circuits have been implemented in 0.35µm and 0.5µm CMOS technology using Mentor Graphics Tool. Comparison of existing CMOS sense amplifier and modified current sense amplifier has been reported. The comparison has been made in term of power dissipation and sensing delay of the circuits. The effect o various design parameters on the current sense amplifier has been discussed and reported.**

Keywords- CMOS, SRAM, Column Selector .

I. INTRODUCTION

Sense amplifiers are one of the most critical circuits in the periphery of CMOS memories. Their performance strongly affects both memory access time, and overall memory power dissipation. As with other ICs today, CMOS memories are required to increase speed, improve capacity and maintain low power dissipation [1]-[4]. These objectives are somewhat conflicting when it comes to memory sense-amp design. With increased memory capacity usually the increased bit-line parasitic capacitance. This increased bit-line capacitance in turn slows down voltage sensing and makes bit-line voltage swings energy expensive resulting in slower more energy hungry memories.

Sense amplifiers are mainly used to read the contents of RAM, DRAM and SRAM cells. They are very sensitive to noise and their design implies that they will provide adequate noise margins and provide good quality of data that represent the contents of a particular memory cell. There are two categories of sense amplifiers. The static sense amplifiers mainly used to detect logic in the static RAMs and SRAMs and the dynamic sense amplifiers mainly used to save energy when low power dissipation is required.

Fast sense amplifiers are important for achieving low latency in many circuits, the most common domain being bit-line reading in memories. With the advent of sub micrometer CMOS chips, interconnection is becoming a major source of on-chip delay, and fast sense amplifiers are also likely to be needed, e.g. as repeaters for high-speed signals which must traverse large chips.

Several operate in current-mode, i.e. they present a low impedance to the inputs and respond to the differential current rather than to the voltage between the inputs , this can reduce interconnect delay in long wires there by providing speed improvement[6], [7]. The current mode sense amplifier reduces the bit line swing during read operation as compared to voltage mode sensing technique. It proves that current sensing technique would be faster than voltage mode due to the low impedance termination of the current mode. It shows that current sensing is relatively insensitive to the bit line capacitance. This gives the motivation to use current mode sensing in the bit lines in SRAM.

II. CROSS COUPLED SENSE AMPLIFIER

Cross Coupled Sense Amplifier

The Current sensing scheme reported in [5], [8] is shown in Fig. 2. The current conveyor consisting of M20-M24 is used as the column selector as shown in Fig. 1. When a cell is accessed and the column select signal CS is low to turn on M23 and M24, the differential current signals will flow from bit lines to data lines.

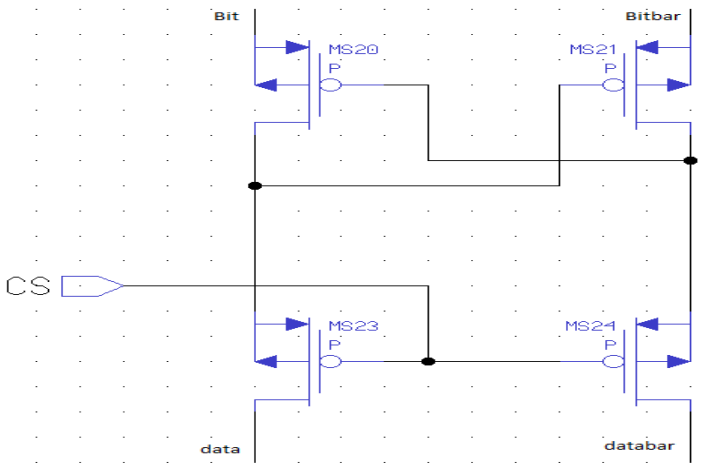

Fig. 1: Column Selector

From voltage-mode circuit viewpoint, M20, M23 and M21, M24 constitute two MOS amplifier and their gains are proportional to the equivalent resistance of M23 and M24. The two amplifiers are connected in positive feedback in the current conveyor circuit. At the end of read operation, column

select signal CS switches from low to high and results in the increase of equivalent resistance of M23 and M24 as well as the gains of the MOS amplifiers consisting of M20-M24. The voltage difference between nodes A and B will be enlarged by the high efficient amplifiers after read operation, instead of being eliminated automatically. Simulation with varied transistor sizes of M20-M24 shows that this unbalancing state is mostly locked by the cross-coupled transistors M20 and M21, even when the column select signal CS becoming low again. In the previous analysis, a voltage balance between nodes A and B is assumed before a read operation. This case may be true in the first read operation, but mostly is not true in the following operation. In order to eliminate the unbalancing state, an equalization device M22 is added to the current conveyor as shown in Fig. 3. M22 is off during the read operation. When the sensing operation is complete, M22 is on to equalize the voltage of nodes A and B.

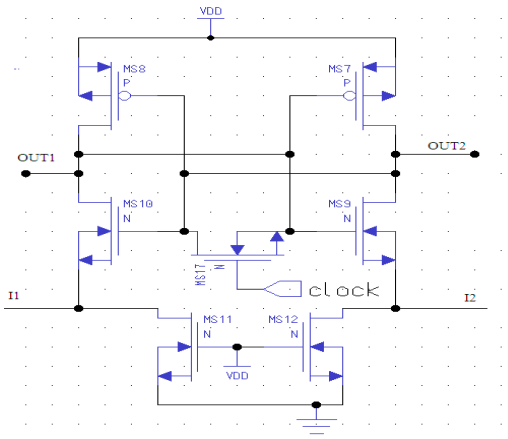

Fig. 2: Cross Couple Sense Amplifier

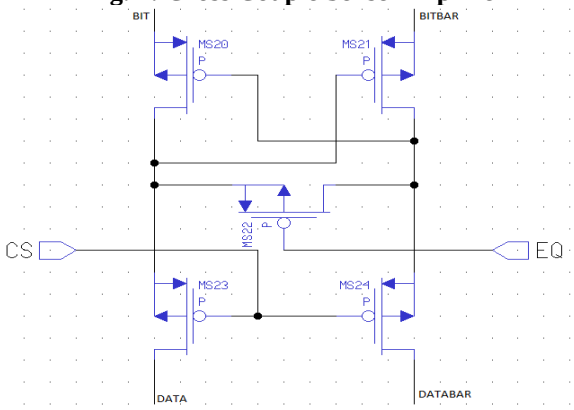

Fig. 3: Modified Column Selector

Modified Cross Coupled Sense Amplifier

The current sense amplifier used in the modified scheme has a higher sensing speed and lower power consumption. The new circuit also operates in two periods: sensing period and equalization period. In sensing period, large size transistors M26 and M25 turn on so that the amplifier has a high current

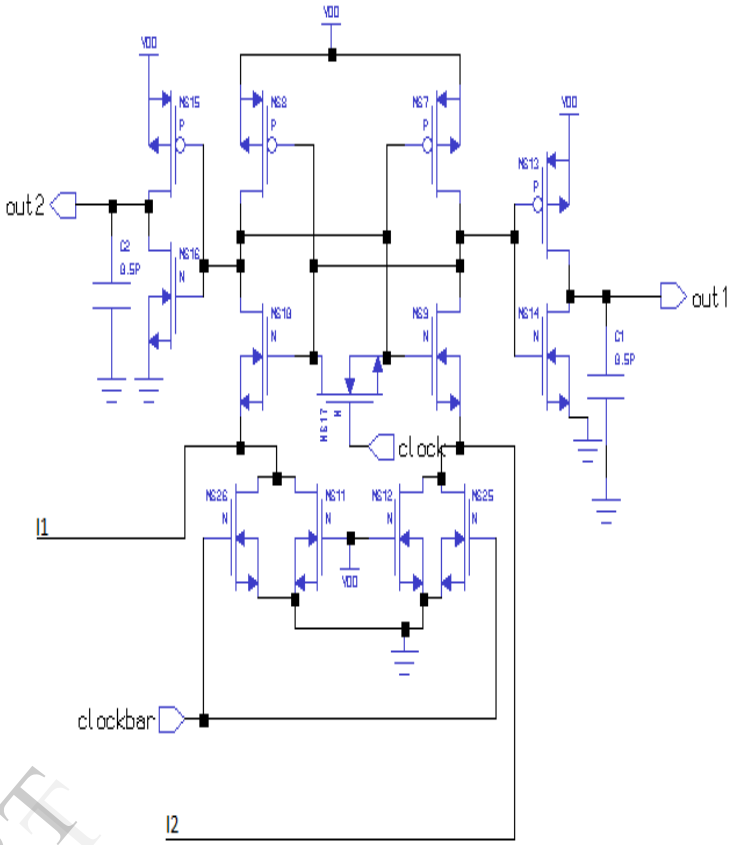

Fig. 4: Modified Cross Coupled Sense Amplified

small size transistors, the DC current flowing through the sense amplifier is reduced. Since the sense amplifier dissipates little power in its sensing period, the whole power consumption of sense amplifier decreases apparently with the equalization current reducing. In addition, the higher load resistance in equalization period conduces to constitute a bigger voltage difference between nodes C and D, which is caused by the differential current signals I1 and 12, at the beginning of sense operation. This is another speed enhancing factor for the proposed sense amplifier. With the same input current signals and same transistor sizes, except the size of load transistors, the modified designed sense amplifier is compared with the previous one in the aspects of power consumption and sensing delay by Mentor Graphics simulation. For the previous amplifier, the size of load device means the size of M11 and M12 in Fig. 2. For the modified, the size of load device is the sum of M11 and M26, or the sum of M12 and M25. In the simulation, the sizes of M11 and M12 are fixed and the sizes of M26 and M25 change from 2 to 16.

III. SIMULATION AND RESULTS

The simulation results of the CMOS Sense Amplifier are shown in Table 1 which shows the comparison of previous current sense amplifier circuit and modified current sense amplifier circuit with different load device sizes. The comparison is between the power dissipation and sensing delay at 0.35µm and 0.5µm technology.

Table 1: Comparison of Previous Current Sense Amplifier and Modified Current Sense Amplifier

Load Device Size	Previous Circuit				Modified Circuit			
	PowerDissip,mW		Sensing Delay, ns		PowerDissip,mW		Sensing Delay, ns	
	0.35µm	0.5µm	0.35µm	0.5µm	0.35µm	0.5µm	0.35µm	0.5µm
2	2.1065	0.2058	2.6128	27.633	1.7145	0.7312	2.0986	27.604
4	2.1155	0.7261	2.5107	6.2833	1.7198	0.1646	1.9867	3.2802
6	2.2605	0.7369	2.4936	6.5789	1.7271	0.1826	1.9768	3.1608
8	2.2895	0.7384	2.4806	6.4824	1.7286	0.2014	1.3368	3.0946
10	2.3818	0.7403	2.4732	6.3929	1.7308	0.2068	1.2986	3.0786
12	2.3882	0.7417	2.4608	6.2656	1.7323	0.2261	1.2768	3.0445
14	2.4971	0.7442	2.4585	6.036	1.7335	0.2861	1.2602	3.0256
16	2.5811	0.7532	2.4302	6.018	1.7344	0.2976	1.2511	3.0168

Fig. 5 shows comparison of power dissipation and sensing delay with different load device sizes. The Fig. a, b, c and d shows the effect of load device sizes on the total power dissipation and sensing delay for 0.35µm and 0.5µm technology.

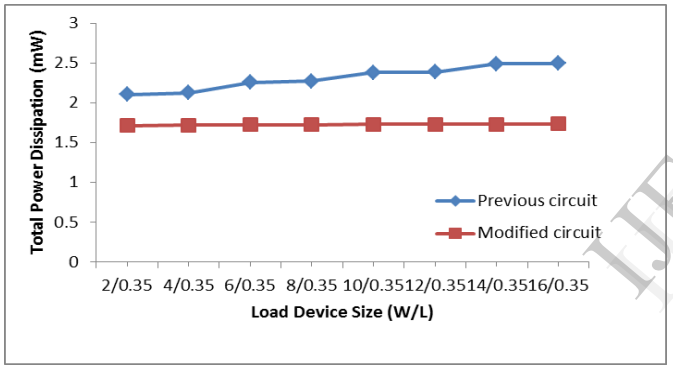

Fig.(a): Power Consumption vs. Load Device Size for 0.35µm Technology

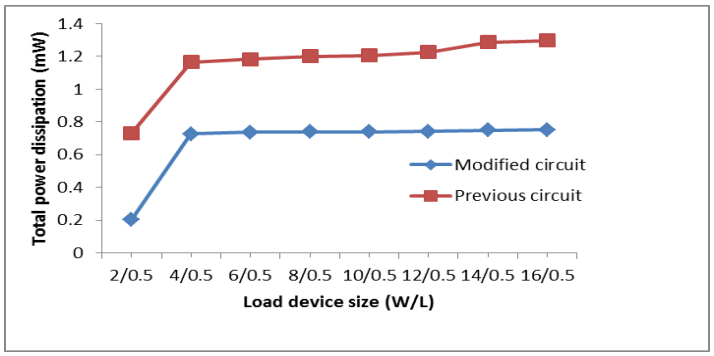

Fig.(b): Power Consumption vs. Load Device Size for 0.5µm Technology

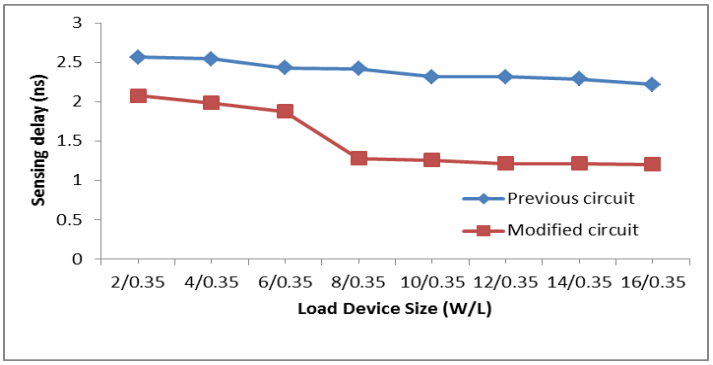

Fig.(c): Sensing Delay vs. Load Device Size for 0.35µm Technology

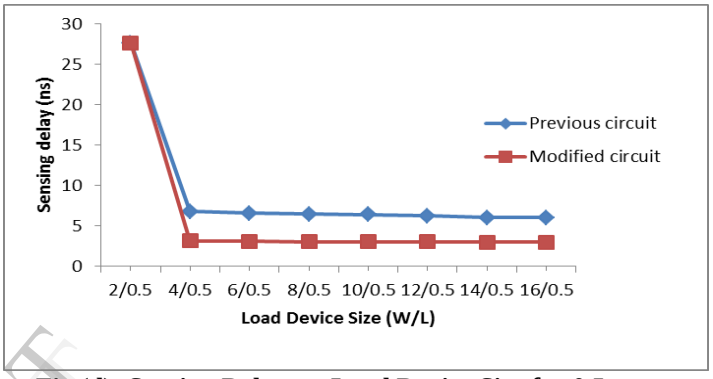

Fig.(d): Sensing Delay vs. Load Device Size for 0.5µm Technology

Fig. 5: Comparison of Power Dissipation and Sensing Delay with Different Load Device Sizes

IV. CONCLUSIONS

The performance of cross coupled sense amplifier was designed, optimized and has been studied for different load device size. The effect of varying the parameter of sense amplifier power dissipation and time delay was calculated and simulated using Mentor Graphics Tool. Comprehensive simulations, analysis and optimization demonstrate the complexity of the structures in terms of design fabrication process. The cross coupled sense amplifier power dissipation and time delay was calculated and concluded that modified cross coupled sense amplifier show excellent performance as compare with previous cross coupled sense amplifier.

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