# Design and Analysis of Current Mode Pipelined Analog to Digital Converter

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*Abstract*— **The analog signal is converted into digital signal by using a analog to digital converter. The converter must be efficient, low power consuming, less area occupying. The new trends in the CMOS technology scaling and the power requirements demand circuit which operate at lower supply voltages. In this paper the designing and analysis of current mode pipelined ADC are proposed which is useful in integration on digital CMOS technology. Scaling of the supply voltage is done in order to reduce the power consumption and to occupy lesser area. The difficulty level in scaling of the threshold voltage increases as the supply voltage is scaled down. . In this paper presents the design and simulation of a converter using current mirror of 10 bits with the supply voltage of 1v in CADENCE SPECTRE tool in GPDK 180nm CMOS process. The converter architecture consists of a low resolution, high speed comparators, a thermometer-weighted current mode DAC and a simple current subtractor and amplifier for generating the residual current. The speed of the complete circuit is increased due to the parallel working of the thermometer encoder and the current subtractor.**

*Keywords— CMOS, current mirror, cadence, low power, analog to digital converter, pipelining, gpdk 180nm.*

## I. INTRODUCTION

An Analog-to-Digital converter is a device, which translates an analog voltage signal into a corresponding digital number. Whenever we relate to the real world most of the signals are analog in nature. But some applications such as digital signal processing requires signals to be digital. In such situations it becomes necessary to get analog to digital conversion using an ADC. Analog-to-digital converter (ADC) is a fundamental block in mixed-signal VLSI circuits. For low-power applications, a pipelined ADC is often used. Resolution, speed, and power consumption are the three key parameters for an analog-to digital converter (ADC). These parameters cannot be changed once an ADC is designed. While one can use 6-bit precision from an 8-bit ADC, it is non-optimal resulting in slower speed and extra power consumption due to full 8-bit internal operation [1].

In this discussion, a new flash ADC design is proposed that is a true variable-power and variable-resolution ADC. It can operate at higher speed and will consume less power when operating at a lower resolution. Such features are highly desirable in many wireless and mobile applications. Optimally, the ADC resolution can be reduced upon the reception of strong signal and can be increased upon the reception of weak signal. Substantial reduction in power consumption at lower resolution will prolong the battery life.

Recently in many wireless mobile applications demand very high speed data converters with wide bandwidth, higher signal to noise ratio and variable (adaptive) resolution with optimized power and cost effectiveness. So there is a need for upgrading the performance of data converters to meet the demands of emerging technologies. So it is a challenging issue in the mixed signal design to have high speed, variable resolution data converters with less space and low power consumption.

## II. METHODOLOGY

The proposed work mainly depends on the analysis, design and implementation of the 10 bit current mode pipelined analog to digital converter. Here at the first, the most important component of the design that is the current mirror circuit is designed. And then the current comparator and the thermometer encoder is designed. Later all the designed components are integrated to obtain the accurate results.

### A. Current Mirror

The basic component used in building the current mode circuits is the current mirrors. The transistors with minimum feature size are often used for VLSI technologies. A circuit with a high output resistance and small channel length modulation is usually desirable. There are many different kinds of current mirrors available.

As far as traditional current mirror is concerned, for the design of analog circuits the output resistance as to be more. As current flows through M1, corresponding to $V_{GS1}$. But $V_{GS1}=V_{GS2}$ so the same current flows through the M2, when it saturate. But this technique has very low output impedance, which can be improve by using the regulated gate current mirror is implemented in this paper.

In regulated gate current mirror the output impedance is increased without the help of any compensation or any biasing circuit. The m1-m4 of nmos and m1-m4 of pmos are used as cascaded current mirrors. M7 and m8 of nmos are used to increase the output impedance of the circuit. The aspect ratio of the Mn5 and Mn7 are same and can be found out by $V_{GS5}=V_{GS7}$, and then $V_{DS6}=V_{DS8}$ which in turn make $V_{GS6}=V_{GS8}$. As $V_{GS6}=V_{GS2}=V_{DS2}$ and $V_{GS6}=V_{DS4}$, the $V_{DS2}=V_{DS4}$ and $I_{in}=I_{out}$.
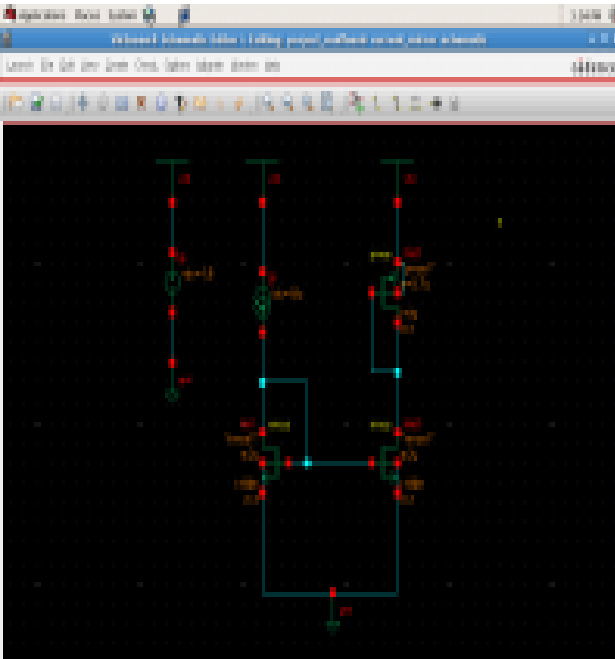
Fig 2.1: schematic of basic current mirror

### B. Comparators

The comparator is the most important component in the ADC architecture. Its role is to convert an input voltage ($V_{in}$) into logic '1' or '0' by comparing a reference voltage ($V_{ref}$) with the $V_{in}$. If $V_{in}$ is greater than $V_{ref}$, the output of the comparator is '1', otherwise '0'. Here $2^N-1$ differential amplifiers are used as comparators in 'N' bits flash-ADC architecture.

When the input signal voltage is less than the reference voltage, the comparator output is at logic '0'.when the input signal voltage is higher than the reference voltage, the comparator output is at logic '1'. The comparators give the $2^N-1$ levels of outputs in terms of reference voltage.
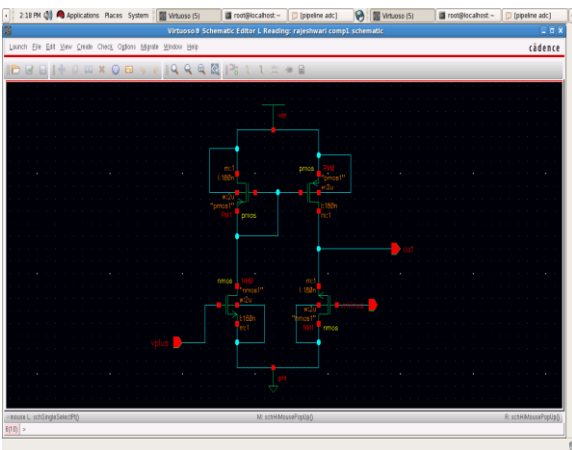


Fig 2.2: Schematic of comparator

### C. Current Amplifier and Subtractor

The current which is passed to current subtractor and amplifier has to be amplified and then subtracted before applying to the next stage. The input current is mirrored by the nmos circuit and the reference circuit is amplified by the pmos circuit block and the transistor msw acts like a switch. This

switch is switched on when $I_{ref}$ is to be subtracted from $I_{in}$. This subtracted current is amplified by doubling the pmos module which mirrors the input current when switch is off.
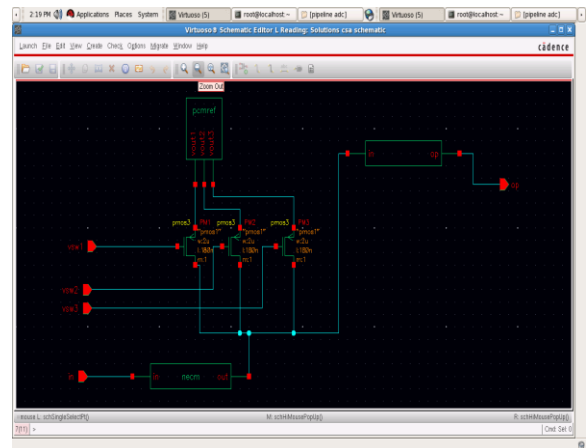


Fig 2.3: Schematic of CSA

### D. Thermometer Encoder

The thermometer encoder is the efficient encoder used in this paper which converts the output of the three comparators into two bit encoded form. The corresponding VLSI schematic design of the current mirror is s shown the following figure.
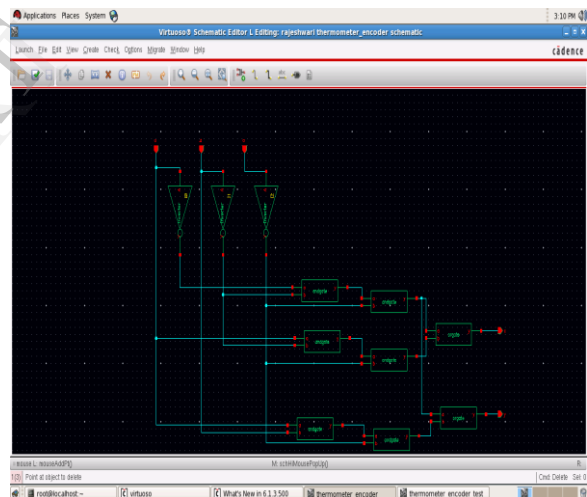


Fig 2.4: Schematic of thermometer encoder

### E. Current Mirred Pipelined ADC

In this proposed work the input is a current and the comparison is done on the currents but the output bits of ADC are logic values. The major concern about the architecture is the power.

Each and every ADC is having a two bit flash ADC, three level comparator and the thermometer encoder. As it is not possible to mirror the current with 0µA, the reference current is shifted to 10µA. Before sending it out the same current will be subtracted to increase the efficiency because the amplifier will not amplify 0µA current. The schematic of the current mirror pipelined ADC is as shown the figure 2.5.
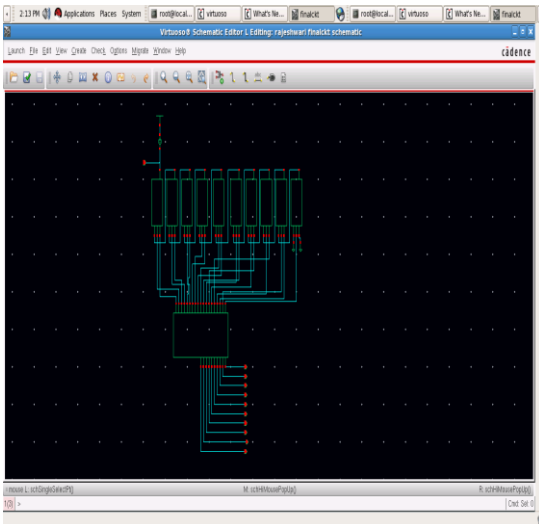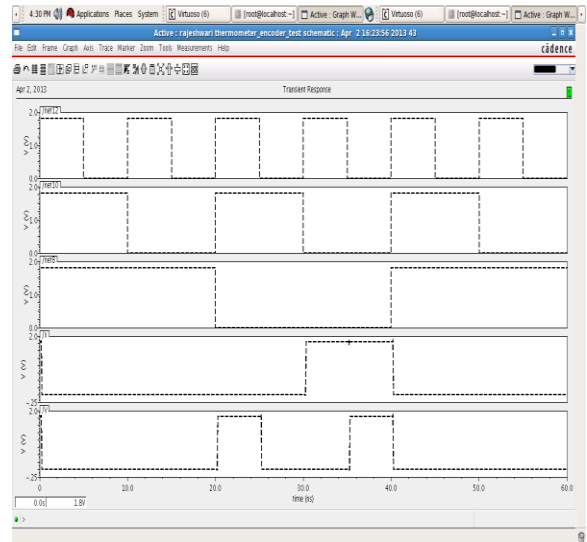
Fig 2.5 Current mode pipelined ADC

## III.    EXPERIMENTAL OUTCOMES

The proposed ADC is designed and implemented in standard gpdk180nm technology of version – IC 6.1 using Cadence virtuoso tool.

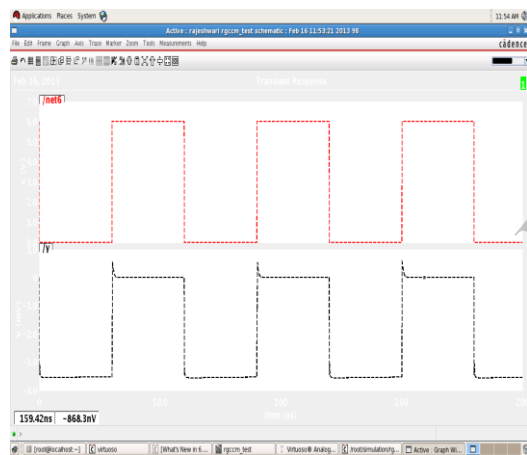The following results were accomplished.



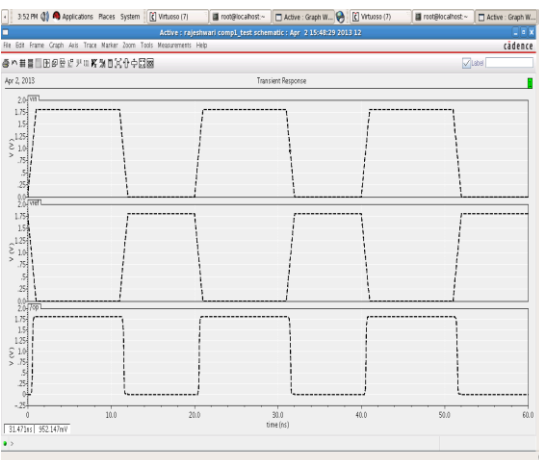Fig 3.1: Output waveform of basic current    mirror.



Fig 3.2: Output waveform of comparator.



Fig 3.3: Output waveform of thermometer encoder.

## IV.    CONCLUSION

The schematic of basic current mirror, comparator stage, current substractor cum amplifier stage, thermometer encoder stage and digital error correction stage are designed. The current mode pipelined ADC is operated at 10-bit precision with analog input voltage of 0 to 1.8V, supply voltage 4V, Resolution 10bits, The ADC is designed and implemented in standard gpdk180nm technology of version – IC 6.1 using Cadence virtuoso tool.

## V.    FUTURE WORK

The design in this paper can be upgraded to give better performance. Resolution can be increased up to 15bits in order to increase the accuracy. Using cadence tool we can write Verilog code in digital labs and can be implemented on hardware. Using different low power comparators and different encoding methods we can design a current mode pipelined ADC in order to decrease the power consumption.

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