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# Design and Analysis of DC-DC Converter Peripherals for Lithium-Ion Battery Charger Using 90nm CMOS Technology

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***Abstract*— This research is centered on developing and analyzing DC-DC converter peripherals tailored for charging Lithium-Ion batteries using 90 nm CMOS technology. Lithium-ion batteries are favored in many applications because of their superior energy density and durability over numerous charge cycles. Efficient charging is critical for maximizing battery lifespan and optimizing overall system performance. DC-DC converters serve a crucial role in this process by facilitating voltage conversion and regulation. The proposed DC-DC converter peripherals are custom-designed to meet the specific demands of Li-Ion battery charging. The primary objectives of the design include minimizing propagation delay, reducing power consumption, maximizing overall circuit efficiency, and achieving a compact form factor suitable for portable and energy-efficient devices. By tailoring the design to the unique characteristics of Lithium-Ion batteries and utilizing the capabilities of 90 nm CMOS technology, the research aims to enhances the operation and dependability of battery charging unit and contributes to the development of more sustainable and efficient electronic devices.**

***Keywords*—90nm technology, Lithium – Ion batteries, level shifter, gate driver, power device, CMOS technology, Lithium – ion battery charger.**

## I. I. INTRODUCTION

At the heart of modern portable electronics is the Lithium-Ion battery, a revolutionary energy stockpile solution known for its exceptional energy density, lightweight nature and rechargeable capability. This battery type has reshaped the technological landscape, finding applications in the huge spectra of devices ranging from telecommunication devices and notebooks to electric vehicles and green energy storage systems. Its superiority over other battery types lies in its ability to store a significant amount of energy in a relatively tiny and feather-weight package, coupled with the ability to be recharged multiple times without significant degradation in performance.

Compared to other battery chemistries, such as lead acid, nickel-cadmium (NiCd) and nickel metal hydride (NiMH), Lithium-Ion batteries offer several distinct advantages [2]. Lead-acid batteries, for example, are bulky, heavy, and have a lower energy density, making them less suitable for portable electronics. NiCd batteries suffer from the "memory effect" and contain toxic cadmium, posing environmental concerns. NiMH batteries offer better energy density than NiCd but still fall short of the performance offered by Lithium-Ion batteries. In contrast, Lithium-Ion batteries provide higher energy density, allowing them to store more energy per unit weight or volume [3]. This translates to longer runtime for portable devices or extended driving range for electric vehicles. Additionally, Lithium-Ion batteries exhibit a lower self-discharge rate compared to NiCd and NiMH batteries, meaning they can hold their charge for longer periods when not in use. Moreover, Lithium-Ion batteries do not suffer from the memory effect, allowing users to recharge them at any state of charge without impacting their overall capacity.

Given the prevalence of Lithium-Ion batteries in portable electronics, there is a growing demand for charging solutions that can maximize their efficiency and longevity. This drives the need for research and development in the design and analysis of charging peripherals, such as DC-DC converters [4], tailored specifically for Lithium-Ion battery chargers. By leveraging technologies like 90 nm CMOS, researchers aim to create charging infrastructures that are not only more efficient but also more compact and suitable for the evolving landscape of portable and energy-efficient devices.

## II. ARCHITECTURE

The architecture of the battery charger chip, as illustrated in Fig 1, includes several key components crucial for its efficient operation: a current and voltage control unit, a level -shifter, a gate-driver, a power MOSFET, and a 5V low dropout (LDO) regulator [5]. Each of these components plays a vital role in ensuring optimal performance during the battery charging process. The current and voltage control unit is responsible for regulating charging parameters, which helps to prevent overcharging and overheating by adjusting the current and voltage levels as needed. The level shifter facilitates internal communication by translating signals between different voltage levels, enhancing the overall efficiency of the system.

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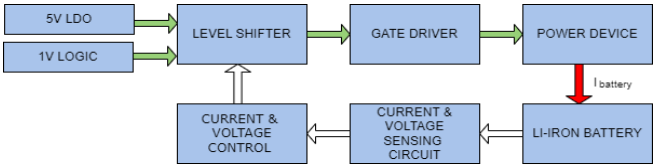


Fig. 1. Architecture of Battery Charger Chip

In this proposed design, novel level shifter and gate driver configurations leveraging 90 nm CMOS technology are introduced. The upgraded level shifter is designed to improve efficiency by quickly elevating voltage levels, thus reducing propagation delay and speeding up the charging process. Simultaneously, the gate driver provides precise control of the power MOSFET, ensuring efficient switching and minimizing power loss.

The power MOSFET, positioned at the core of the architecture, acts as the primary switching device, managing the current flow to the battery and aiming to reduce power loss and heat generation. The integration of current and voltage sensing circuitry further enhances the charger's ability to monitor and regulate the charging process effectively.

Additionally, the current and voltage control unit plays a critical role in maintaining the safety and longevity of the battery by dynamically adjusting the charging parameters. This ensures that the battery operates within safe limits, preventing potential damage from excessive current or overheating. The novel level shifter design in this architecture, utilizing 90 nm CMOS technology, allows for faster voltage translation, which significantly reduces propagation delays and speeds up the overall charging process. This quick response is crucial for maintaining high efficiency in power management.

Moreover, the gate driver, also enhanced by 90 nm CMOS technology, provides accurate control over the power MOSFET. This precision is vital for efficient switching, as it minimizes power losses during the transition states, thereby improving the overall power efficiency of the charger. The power MOSFET itself, being the central switching element, is designed to handle high current flows with minimal resistance, reducing heat generation and further improving efficiency.

The inclusion of a 5V low dropout (LDO) regulator ensures stable and reliable voltage supply to the different components of the charger, which is essential for consistent performance. The combination of these advanced components and the integration of current and voltage sensing circuitry enable the charger to effectively monitor and regulate the charging process, ensuring optimal performance.

Ultimately, the advancements made possible in this charger architecture are poised to deliver a highly efficient and compact solution for modern portable electronics. These innovations not only enhance the performance and reliability of the battery charging system but also facilitates to the development of more persistent and energy-effective electronic devices. By meeting the stringent demands of today's portable electronics, this design promises to extend device runtime and optimize battery usage, thereby addressing the growing needs of consumers for dependable and effective power management solutions.

## III. PROPOSED LEVEL SHIFTER AND GATE DRIVER

### A. PROPOSED LEVEL SHIFTER

In electronic circuits, level shifters are indispensable components, particularly in systems where signals must be transferred between different voltage domains. Their primary function is to convert input signals from one voltage level to another, enabling circuit components operating at different voltage levels to communicate and function together seamlessly.

In DC-DC converter peripherals for Lithium-Ion battery chargers, the role of a level shifter becomes even more critical. These converters are essential for managing the power flow from the charger to the battery [6], ensuring that the battery charges efficiently and safely. The level shifter acts as an intermediary, linking the low-voltage control signals produced by the control circuitry to the high-voltage power devices used in the power conversion stage, that includes MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistors) and IGBT (Insulated Gate Bipolar Transistors). Lithium-Ion batteries typically operate at higher voltages — around 3.7V per cell— whereas the control circuitry within the charger often operates at much lower voltages, such as 0.9V or 3.3V. This disparity necessitates the use of a level shifter to ensure effective communication between the control circuitry and the power devices [7]. The level shifter adjusts the voltage levels of the input signals, either amplifying or reducing them, to match the voltage requirements of the target domain. This voltage translation is vital for the accurate and efficient operation of the power devices, ensuring that they receive the correct control signals.

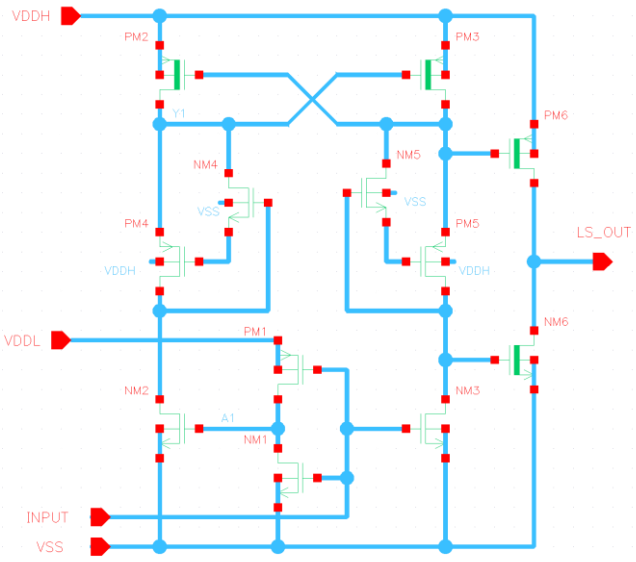


Fig. 2. Proposed Schematic of Level shifter

By facilitating this seamless voltage translation, the level shifter enables precise coordination and control of the power conversion process within the DC-DC converter. This ensures that the high-voltage power devices can be effectively managed by the low-voltage control signals, optimizing the performance and efficiency of the battery charger. Moreover, the level shifter contributes to the overall reliability and safety of the charging system, as it ensures that the various components operate within their specified voltage

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ranges, preventing potential damage due to voltage mismatches.

Fig 2 illustrates the proposed level-shifter schematic implemented using 90nm CMOS technology. This design comprises 12 transistors, including 6 PMOS and 6 NMOS transistors. The transistors NM1, NM2, NM3, and PM1 form the lower voltage circuit, which operates with an input voltage of 0.9V. This low-voltage signal is then transferred to the higher-voltage circuit. The higher voltage circuit incorporates a current-limiting circuit, which is constructed using the transistors PM2, PM3, PM4, PM5, NM4 and NM5. This part of the circuit is crucial for controlling the current flow and ensuring the safe and efficient operation of the level shifter. Finally, the transistors NM6 and PM6 are responsible for driving the stepped-up voltage, completing the voltage translation process. The strategic arrangement and interaction of these transistors enable the level shifter to perform its function effectively, ensuring efficient and reliable voltage level translation in the charging system.

## B. CONVENTIONAL AND PROPOSED LEVEL SHIFTER

A gate driver is a fundamental component in power electronics, particularly in systems utilizing high-power semiconductor devices like Metal-Oxide-Semiconductor Field-Effect Transistors or Insulated Gate Bipolar Transistors. Its primary function is to supply the necessary drive signals to these power devices, enabling them to switch on and off rapidly and efficiently.

In DC-DC converters for lithium-ion battery chargers, the gate driver plays a critical role in managing the operation of power-switching devices such as MOSFETs. These devices are essential for converting and regulating voltage during the charging process. The DC-DC converter must efficiently adjust the voltage from the input source (like a DC power supply or another battery) to the appropriate charging voltage for the battery. The gate driver ensures that MOSFETs or other power devices switch on and off with precise timing, accurately responding to control signals generated by the system. This precise control is crucial for maintaining high efficiency and minimizing power losses throughout the charging process.

Additionally, gate drivers often incorporate features like overcurrent protection, under voltage lockout, and temperature monitoring, which enhance the safety and reliability of the charging system. These protective characteristics are an add-ons in preventing the damage to the power devices and the overall system, ensuring safe and stable operation.

The role of the gate driver extends beyond just switching the MOSFETs or IGBTs on and off. It is also responsible for optimizing the performance of these power devices by ensuring they operate within their optimal parameters. For instance, a gate driver can control the switching speed of a MOSFET, which directly impacts the efficiency and thermal performance of the device. Faster switching can reduce energy losses during transitions, but if the switching is too fast, it can generate excessive electromagnetic interference (EMI) and potential ringing in the circuit. Therefore, gate drivers often include adjustable settings or built-in features to fine-tune the switching speed to balance efficiency and EMI concerns.

Gate drivers also handle the time management in circuits where two or more power devices are used in configurations like half-bridge or full-bridge topologies. Dead time is a short interval where both the high-side and low-side MOSFETs are off, preventing short circuits or shoot-through conditions, which can damage the power devices. Proper dead time management by the gate driver is crucial for the safe and efficient operation of the power converter.

Furthermore, gate drivers are designed to withstand the harsh electrical environments typically found in high-power applications. They need to manage high voltages and currents without degrading their performance or causing failures. Therefore, gate drivers often include features like galvanic isolation, which separates the high-power and low-power sections of the circuit to protect sensitive control electronics from high-voltage transients.

Temperature management is another critical aspect that gate drivers address. High-power devices generate significant heat, and excessive temperatures can lead to device failure. Modern gate drivers include temperature monitoring and protection features to ensure that the power devices operate within safe temperature ranges. If the temperature exceeds a predefined threshold, the gate driver can reduce the switching activity or shut down the device to prevent thermal damage.

Overall, the gate driver serves as the intermediary between the control circuitry and the power devices, converting low-power control signals into high-current drive signals required for the accurate switching behaviour of the power devices. By delivering robust and efficient drive signals, the gate driver ensures the optimal performance and reliability of the DC-DC converter. This, in turn, facilitates efficient and safe charging of Lithium-ion batteries, making it an indispensable component in modern power electronic systems. Through their advanced features and precise control capabilities, gate drivers are crucial in enabling the development of high-performance, energy-efficient, and safe power conversion solutions.

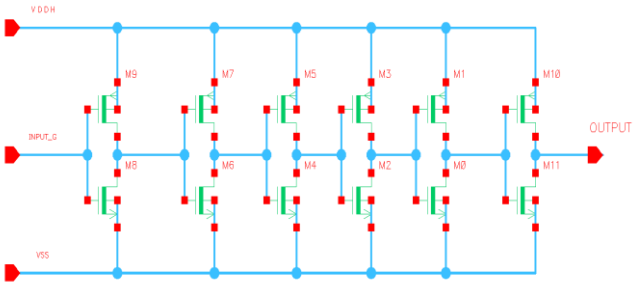


Fig. 3(a). Conventional Schematic of Gate Driver

Fig 3(a) provides a schematic representation of a conventional gate driver circuit and Fig 3(b) provides a schematic representation of the proposed gate driver circuit. These buffer circuits play a pivotal role in stabilizing the signals and ensuring the proper activation of the power MOSFET and how they are placed in these two models help us improve the power consumption without compromising the output efficiency.

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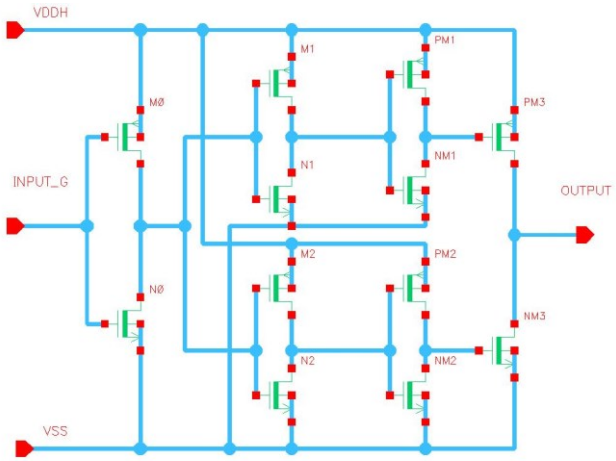


Fig. 3(b). Proposed Schematic of Gate Driver

## C. POWER MOSFET

A power MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) is a specialized type of transistor designed to manage and control significant power levels efficiently. Unlike standard MOSFETs, power MOSFETs are optimized for applications that require high current and voltage handling capabilities. These devices play a crucial role in modern electronics, particularly in systems that require efficient power switching and amplification, such as power supplies, motor controllers and DC-DC converters.

The structure of a power MOSFET includes three primary terminals: the gate, the drain, and the source. The gate terminal controls the flow of current between the drain and the source [5]. When a voltage is applied to the gate, an electric field is created, allowing current to flow from the drain to the source, effectively turning the MOSFET on. Conversely, when the gate voltage is removed, the current flow stops, turning the MOSFET off. This ability to switch on and off rapidly with minimal energy loss makes power MOSFETs highly efficient and suitable for high-speed switching applications.

Major features of power MOSFETs include its high efficacy. They are designed to switch rapidly with low energy loss, which is crucial for applications like switching power supplies and DC-DC converters. Additionally, power MOSFETs are characterized by their low on-resistance (RDS (on)), which is the resistance between the drain and source terminals when the device is turned on. Lower RDS (on) values result in lower conduction losses, thereby enhancing overall efficiency. Furthermore, power MOSFETs are engineered for effective thermal management, often featuring large metal tabs and other design elements to dissipate heat efficiently, ensuring reliable operation under high power conditions.

Power MOSFETs are widely used across various applications. In power supplies, especially switched-mode power supplies (SMPS), they are essential for efficient electrical power conversion. In motor control applications, power MOSFETs are employed in motor drivers and controllers for electric vehicles and industrial machinery due to its ability to handle high currents. It is also crucial for DC-DC converters, which regulate voltage levels in numerous electronic devices, including computers and mobile phones. Additionally, power MOSFETs find applications in audio amplifiers, where they help amplify signals with low distortion, contributing to high-fidelity audio performance.

The advantages of power MOSFETs are numerous. Their high efficiency and fast switching speeds reduce power loss and improve performance in various electronic systems. Their versatility allows them to handle a broad range of voltages and currents, resulting in diverse array of applications. Moreover, power MOSFETs are designed for reliability, capable of withstanding high temperatures and electrical stress, which ensures durability and long-term performance in demanding environments [15]. These features make power MOSFETs indispensable components in the realm of power electronics, enabling the development of more efficient, compact, and reliable electronic devices.

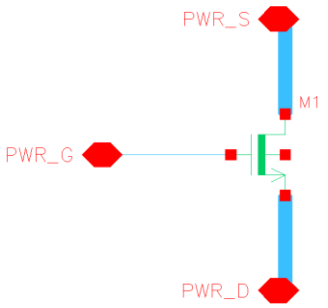


Fig. 4. Schematic of Power MOSFET

Fig 4 illustrates the schematic design of a power MOSFET using an NMOS configuration. This power MOSFET is designed to operate with a gate voltage of 5V, which is essential for turning the device on and enabling current to flow between the drain and source terminals. The schematic shows how the power MOSFET receives a stepped-up voltage from a gate driver, which is crucial for its operation. The gate driver amplifies the control signal to the necessary 5V, ensuring that the MOSFET switches on effectively. When this voltage is applied to the gate, it creates an electric field that forms a conductive channel, allowing the electrons to flow from the drain to the source. This process enables the MOSFET to manage the power flow efficiently within the circuit. The integration of the gate driver and the power MOSFET is critical for applications requiring rapid and reliable switching, such as in power supplies, motor controllers and voltage regulators. The design ensures that the MOSFET operates with high efficiency and minimal power loss, highlighting the importance of precise voltage control in power management systems.

## D. INTEGRATED DESIGN OF LEVEL SHIFTER, GATE DRIVER AND POWER MOSFET

Fig 4, depicts the final representation of the level-shifter, gate-driver and the power MOSFET connected. The input of 0.9 V is driven into the level shifter and the shifted voltage of 5V is produced as the output further the stepped-up voltage is passed into a gate driver which turns on the power device.

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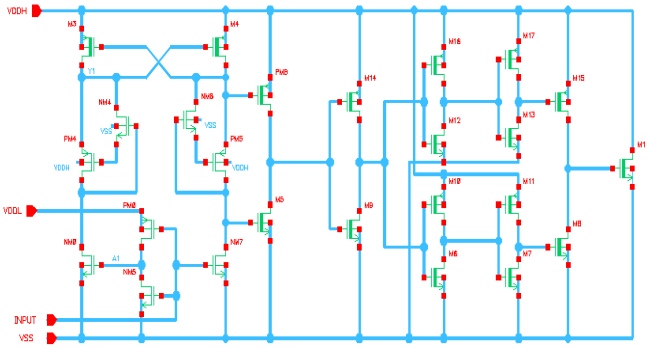


Fig. 4. Schematic of Proposed Gate Driver, Level Shifter and Power MOSFET together

## IV. SIMULATION RESULTS

### A. TRANSIENT ANALYSIS OF PROPOSED LEVEL SHIFTER

The transient analysis of the proposed level shifter is illustrated in Fig 6. During this analysis, an input voltage of 0.9V is successfully shifted to an output voltage of 5V. The resulting propagation delay, a critical parameter for assessing the performance of the level shifter, is precisely measured at 37.15 ps. The rise time and fall time of the proposed model is measured to be 25.42ps and 48.93ps, respectively. The obtained propagation delay is 37.15ps. Since there is minimal delay, the circuit is significantly efficient, ensuring fast and reliable operation, which is crucial for Lithium-Ion battery chargers.

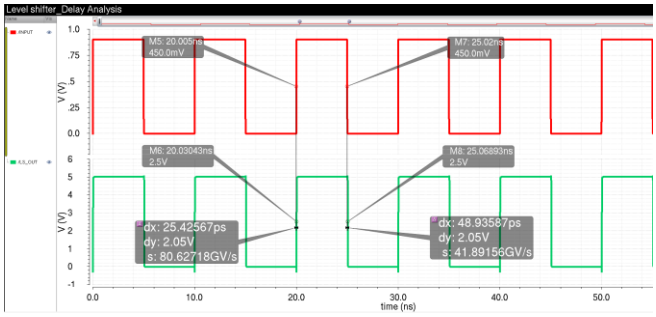


Fig. 6. Transient Analysis for propagation delay of proposed level shifter

To further validate the consistency and reliability of this propagation delay, a Monte Carlo analysis was conducted, involving 180 samples. This statistical analysis, depicted in Fig 7, provides a comprehensive understanding of the variation in propagation delay, highlighting the robustness and stability of the proposed design under different conditions. By analyzing the spread and mean of the delay times, the Monte Carlo analysis offers valuable insights into the performance and potential variability of the level shifter in practical applications.

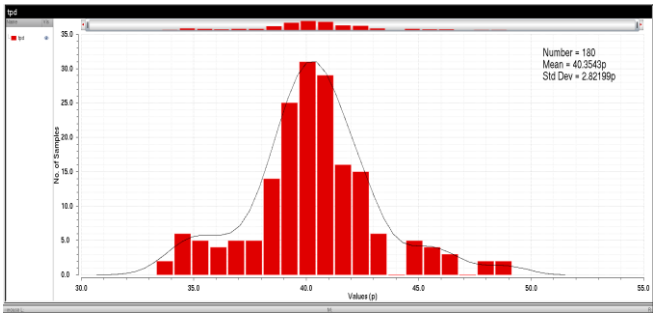


Fig. 7. Monte Carlo Simulation for Propagation Delay of Proposed level shifter with 180 Samples

### B. COMPARATIVE ANALYSIS OF VARIOUS LEVEL SHIFTER

TABLE 1 COMPARATIVE DELAY ANALYSIS OF PROPOSED LEVEL SHIFTER AND OTHER DESIGN

| Work/reference | Technology | VDDL (V) | VDDH (V) | Delay (ns) |
|---|---|---|---|---|
| This paper | 90nm CMOS | 0.9 | 5.0 | 0.037 |
| [8] | 180nm CMOS | 1.8 | 5.0 | 0.15 |
| [9] | 65nm CMOS | 1.2 | 5.0 | 0.61 |
| [10] | 180nm CMOS | 0.4 | 3.0 | 15.65 |
| [11] | 0.35 um HV | 3.3 | 6.7-10 | 3.00 |
| [12] | 45nm CMOS | 0.7 | 1.2 | 12.18 |
| [13] | 28nm FDSOI | 0.25 | 1.0 | 3.11 |

Table 1 presents a comparative analysis of different level shifter designs across various technologies, detailing their supply voltages and resulting delay times. The first entry describes the proposed work, a level shifter using 90nm CMOS technology with a low supply voltage (VDDL) of 0.9V and a high supply voltage (VDDH) of 5V, achieving a delay of 0.037 nanoseconds (ns). This table highlights how varying technologies and supply voltages impact the performance, specifically the delay, of level shifters.

### C. TRANSIENT ANALYSIS OF PROPOSED GATE DRIVER

The transient analysis of the conventional gate driver is illustrated in Fig 8, showing a propagation delay of 125.545 ns. In comparison, the proposed gate driver, as depicted in the Fig 9, achieves a significantly reduced propagation delay of 110.81 ns. This improvement highlights the enhanced performance of the proposed design over the conventional gate driver.

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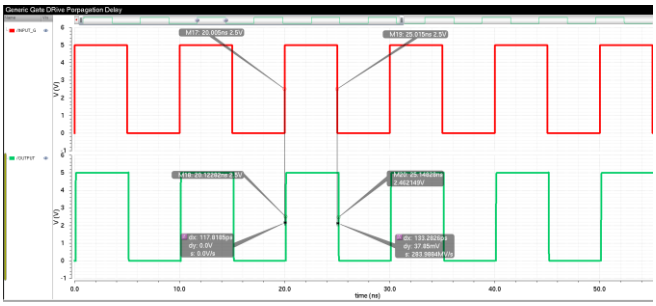

Fig. 8. Propagation Delay of Conventional Gate Driver

The reduced propagation delay of the proposed gate driver indicates a notable increase in efficiency, making it particularly advantageous for applications that require rapid and reliable signal processing. The enhancement in delay performance underscores the effectiveness of the proposed gate driver in optimizing system response times, thereby contributing to better overall performance in high-frequency switching scenarios.

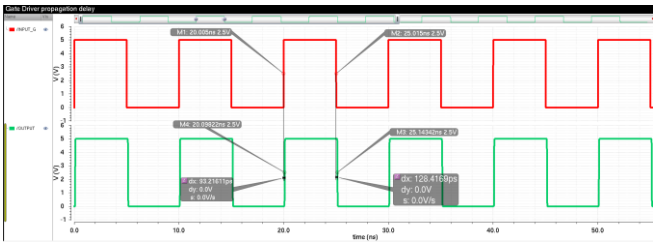

Fig. 9. Propagation Delay of Proposed Gate Driver

## D. ANALYSIS OF LEVEL SHIFTER AND GATE DRIVER

The level shifter is interfaced with the power device through a gate driver, which plays a crucial role in amplifying the signal from the level shifter. This amplified voltage is then used to activate the power MOSFET. This configuration highlights how the gate driver enhances the output of the level shifter before it is applied to control the power MOSFET, ensuring efficient signal transmission and reliable operation of the power device.

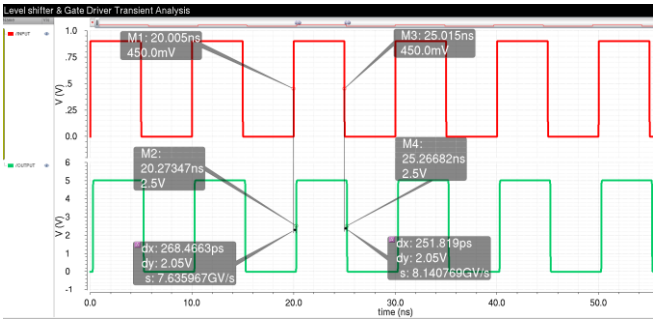


Fig. 10. Propagation Delay of Proposed Gate Driver and Level Shifter together

The transient analysis of the integrated level shifter and gate driver system is shown in Fig 10. The combined system exhibits a rise time of 268.4ps, a fall time of 251.8 ps, and an overall propagation delay of 260.1 ps. In this configuration, the level shifter first steps up the input voltage from 0.9V to 5V. This adjusted signal is then fed into the gate driver, which stabilizes the voltage before it is sent to the power MOSFET. The gate driver ensures that the signal is properly conditioned to effectively turn on the power device, demonstrating the seamless integration and efficient performance of the combined system.

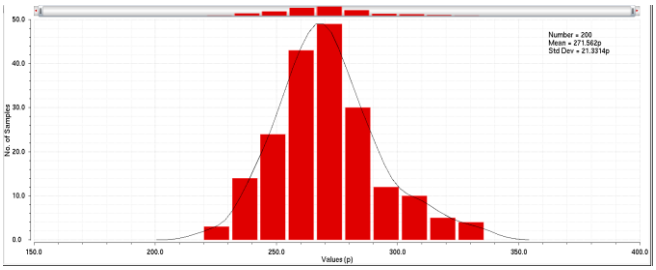

Fig. 11. Monte Carlo Simulation for Propagation Delay of Proposed Gate Driver and Level Shifter together

Monte Carlo analysis was conducted on the circuit shown in Fig 11, utilizing 200 samples to assess the propagation delay. This analysis, detailed in Fig 10, offers a thorough evaluation of the propagation delay variability across different conditions. By simulating a range of scenarios, the Monte Carlo analysis provides a comprehensive understanding of the circuit's performance consistency and robustness. The results illustrate the range and distribution of propagation delays, highlighting how the circuit maintains its performance under varying operational conditions. This detailed statistical evaluation underscores the reliability and stability of the circuit design, ensuring its effectiveness and predictability in practical applications.

## E. TRANSIENT ANALYSIS OF LEVEL SHIFTER, GATE DRIVER AND POWER MOSFET TOGETHER

Fig 12, provides an in-depth analysis of the complete circuit, which includes the level shifter, gate driver, and power device. The Figure details the input voltage of 0.9V, which is first processed by the level shifter and then fed into the proposed gate driver. The output from the gate driver is shown with a rise time of 611.73 ps and a fall time of 647.760ps, resulting in an overall propagation delay of 629.745ps.

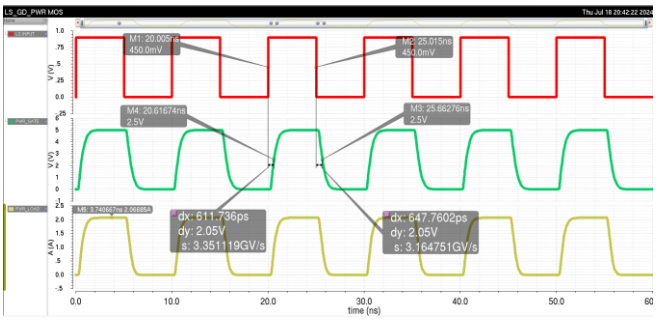


Fig. 12. Propagation Delay of Proposed Gate Driver and Level Shifter connected to output Power MOSFET

This output from the gate driver is subsequently used to drive the power device. The performance characteristics of the power device, including its output, are also depicted in Fig 12. This comprehensive analysis illustrates the signal's journey through the entire circuit, highlighting the timing and performance metrics at each stage. By examining these parameters, the figure provides a detailed understanding of

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how the integrated components work together to achieve efficient and reliable operation. This detailed view underscores the effectiveness of the design in managing signal transitions and delays, crucial for ensuring optimal performance in practical applications.

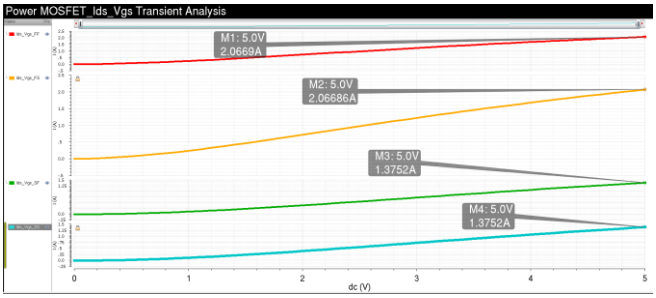


Fig. 13. Power MOSFET's $I_{ds}$ vs $V_{gs}$ graph for FF, FS, SF and SS models

For the different MOSFET models—FF, FS, SF, and SS—the $I_{ds}$ versus $V_{gs}$ characteristics were evaluated. The goal of the proposed design is to achieve a maximum current of 2A. As shown in Fig 13, both the FF and FS models successfully achieve this target. The graph illustrates how these models reach the desired current level, confirming their suitability for applications requiring high-current performance. This analysis highlights the effectiveness of the FF and FS models in meeting the design specifications and achieving the required performance.

## V. CONCLUSION

The research focuses on designing a level shifter and gate driver that meet the demanding requirements of Lithium-Ion battery chargers. The proposed level shifter efficiently converts a 0.9V input signal to a 5V output, enabling effective control of the power MOSFET, a key component in the charging circuit. The novel design using 90nm CMOS technology minimizes power propagation delay, thereby enhancing the charging efficiency and reducing power consumption.

The level shifter in the proposed design effectively increases the input voltage from 0.9V to 5V with an impressive propagation delay of just 0.037 ns. This performance is notably faster and more efficient compared to other level shifters available. After the voltage is shifted, the output is fed into a gate driver. The gate driver plays a critical role in stabilizing the output from the level shifter, ensuring that the signal remains strong and consistent. The gate driver achieves this with a propagation delay of 629.745 ps.This propagation delay is carefully maintained throughout the circuit, which is crucial for ensuring the overall efficiency and reliability of the design. The consistent delay performance across the circuit components underscores the robustness of the proposed system.

The power MOSFET, which is controlled by the stabilized output from the gate driver, operates with a current of 2A. This current level is achieved using the transistor in the FF (Fast-Fast) model, indicating the design's capability to handle high current efficiently. The integration of the level shifter and gate driver, along with the power MOSFET's performance, demonstrates the system's effectiveness in delivering high-speed and reliable voltage regulation and current control.

The entire design and simulation process was conducted using the Cadence Virtuoso platform, ensuring accurate and reliable results. The advancements presented in this paper supports to the development of high efficient and compact charging solutions for Lithium-Ion batteries, thereby supporting the evolving needs of modern portable electronics and promoting sustainable and efficient energy usage.

In conclusion, the research successfully demonstrates that leveraging 90nm CMOS technology in the design of DC-DC converter peripherals significantly enhances the efficiency and performance of Lithium-Ion battery chargers. This work lays the groundwork for further innovations in battery charging technology, promoting longer battery life and more reliable portable electronic devices.

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