Published by :
http://www.ijert.org

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 09, September-2020

Design and Analysis of Low Power Reversible Adder/Subtractor Circuits

Nitin Krishna V
B. E. Student, Dept of ECE, PSG College of Technology, Coimbatore, India

Uma A
Assistant Professor(Sl. Gr.), Dept of ECE, PSG College of Technology, Coimbatore, India

***Abstract*—In recent years, reversible logic has become a promising technology in the areas of low power VLSI design, nanotechnology, quantum computing and optical computing. The performance and reliability of digital systems which are now implemented using conventional logic gates can be enhanced by the usage of reversible logic gates, which pave for low power consumption and lesser quantum delays, thus increasing the speed of computation. Adder/subtractor circuits form the fundamental block in the arithmetic and logic unit of processors and other digital logic programmable devices. The performance of a digital system, its speed and throughput depend critically on the way these circuits are designed. Adder circuits are used in the Graphics Processing Unit(GPU) of computers for graphics applications to reduce complexity. Any way to enhance the performance and computational speed of these circuits will pave way for a better ALU. Incorporating the concepts of reversible computing in the design of adder/subtractor circuits can significantly enhance the performance and speed of operation of digital systems. In this paper, two existing adder/subtractor designs and a novel design are compared, analyzed for different bit lengths (1,8,16,32,64). Detailed analysis of reversible logic design parameters, power consumption parameters, and FPGA utilization parameters is carried out. These designs are analyzed and simulated using the Xilinx Vivado tool and implemented on Zedboard Zynq 7000 Evaluation and Development kit(xc7z020clg484-1). The proposed design outperforms the existing designs.**

Keywords—Reversible ALU design; Reversible logic; Reversible adder/subtractor; Low power VLSI design; High speed adder;

I. INTRODUCTION

Over the past few decades, phenomenal growth has been achieved in the design of computers and other digital logic processing devices like mobile phones, calculators, etc. Incorporating several millions of transistors into a single chip has enabled computations and operations to be efficient and fast. However, having very high transistor densities will lead to an increase in power dissipation. Existing technologies like CMOS will reach their boundaries soon as believed by today's researchers. Power dissipation and vulnerability to computing errors are the most important problems associated with the existing technologies. Reversible Logic is believed to be a prominent technology that could alleviate the drawbacks of the existing technologies. Reversible circuits are called lossless circuits, as there is neither energy loss nor information loss. These circuits are very attractive in applications where extremely low power consumption, is needed in areas ranging from communications, low power VLSI (Very Large-Scale Integration) technology, DNA computing to nanotechnology. Furthermore, reversible logic is very useful in quantum computing where the quantum evolution is inherently reversible. Arithmetic circuits such as adders, subtractors, multipliers, and dividers are the quintessential blocks in a data processing system. Dedicated Adder/Subtractor circuits are required in several Digital Signal Processing applications. Reducing the number of reversible gates required to realize a circuit, quantum costs incurred and garbage inputs/outputs are the focus of research in reversible logic circuit design.

In [1], it is depicted that the amount of energy (heat) dissipated for every bit operation that is not reversible is given by KT ln2, where K is the Boltzmann's constant (1.3807×10-23 JK-1) and T is the operating temperature of the system. For T equal to the room temperature (300 K), KT ln2 is approximately equals 2.8×10-21 J, which might seem is small but it is non-negligible. For example, assuming that all the 1.75 billion transistors in a processor (e.g., Intel i5 core) dissipate heat at a rate equal to the processor's operating frequency (2.5 GHz), then the processor would consume a power of approximately (2.5 x 10^9) x (KT ln2) x (1.75 x 10^9) = 12.258 mW (Assuming that the room temperature is 300K). The loss incurred is not tolerable in the design of ultra-low power consuming devices. Furthermore, Moore's law states that speed and capability of computers can be expected to double every two years, as a result of increases in the number of transistors a microchip can contain. The increase in transistors will lead to further power consumption and power dissipation due to information loss. If this goes on, there will be an intolerable amount of heat dissipation by computer systems. The advent of revolutionary technologies in computing is the need of the hour. One such technology is reversible computing. [2-3] In 1973, C. H. Bennett concluded that no energy would dissipate from a system as long as the system was able to return to its initial state from its final state regardless of what occurred in between. In [4], it is shown that the theory of reversible computing is based on invertible primitives and composition rules that preserve invertibility and the constraints to be met with deal with both functional and structural aspects of computing processes. The laws of physics won't have an impact on the reduction in the size and quantum behaviour of computers as depicted in [5]. Reversible logic can be defined as thermodynamics of information processing. Hence, it is used to reduce the power dissipation by preventing the loss on information[6]. It is shown in [7] that parallel adder/ subtractor can be extended to design low power Reversible ALUs, Multipliers and Dividers. In [8], four designs for reversible full-adder circuits and their implementation in CMOS logic and pass transistor logic were presented. A detailed

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 09, September-2020

description on reversible computing, quantum implementation of reversible gates, challenges and promising features of reversible logic in [9]. Furthermore, it delineates how reversible logic technology will pave way for achieving ultra-low power computing. [10] presents a detailed analysis of FPGA utilization parameters and power parameters of reversible logic designs. Two designs of adder/subtractor circuits using WG gate and DKG gate are proposed in [11]. A serial adder/subtractor circuit constructed using 4*4 DKG gate and an analysis on reversible logic parameters is carried out in [12]. A 8-bit adder-subtractor circuit using reversible approach for Xilinx Spartan 3E FPGA is proposed, simulated and synthesised in [13]. In [14], a novel design of ALU is compared with an existing design. In [15], three designs using TR, Peres and Feynman gates were proposed and compared them interms of quantum cost, garbage outputs and gate count. One of the designs is considered as Existing Design 1 in this paper. A 8 bit parallel adder/subtractor using DKG gate and Dual Key Pair Gate (DKPG) in Xilinx ISE Design Suite is implemented in [16].

Section II of the paper explains the terminologies associated with reversible logic, power consumption parameters like static power, dynamic power, etc and FPGA design and utilization parameters like LUTs, nets, etc. Section III of this paper presents some of the important basic reversible logic gates, their quantum costs, and quantum representations. In section IV, a brief overview of adder/subtractor circuits. Section IV presents the existing design 1[15], the existing design 2[11] and the proposed design. The circuit diagram, RTL Schematic, various logical and arithmetic operations of both designs are also provided under it. Section V of the paper consists of simulation results of the designs for different bit lengths, waveform results from Xilinx Vivado tool and also charts and tables of comparison of parameters like gate count, number of garbage outputs, power parameters, the delay incurred and FPGA utilization parameters. Section VI presents the conclusion of the paper.

II. TERMINOLOGIES

A. *Reversible Function*

A multiple output Boolean function F(x1; x2; ... ; xn) of n Boolean variables is said to be reversible, if it can satisfy the following conditions.

a. The number of outputs is equal to the number of inputs.

b. Any output pattern has a unique pre-image that is, there must be a one-to-one mapping between the inputs and outputs.

B. *Reversible Logic Gates*

A gate is said to be reversible, if it has a reversible function. Reversible gates can be used to “fan-out” the input signal. Since the output is a mere copy of the input, we can easily recover the input from the output.

C. *Constant Inputs / Ancilla Inputs.*

This refers to the number of inputs that are to be maintained constant at either logic 0 or logic 1 in order to synthesize the given logical function.

D. *Garbage Outputs.*

Garbage outputs refers to the number of outputs which are not used in the synthesis of a given function. In certain cases, these become mandatory to achieve reversibility. Garbage is the number of outputs added to make an n-input k-output function ((n; k) function) reversible. Equation (1) shows the relation between the number of inputs, ancilla inputs, outputs and garbage outputs.

$$\text{Inputs} + \text{Constant inputs} = \text{Outputs} + \text{Garbage} \quad (1)$$

E. *Quantum Cost*

Quantum cost refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit. The quantum cost of each reversible logic gate is an important optimization parameter. The quantum cost of a circuit is the minimum number of 2*2 unitary gates to represent the circuit keeping the output unchanged. The quantum cost of a 1*1 gate is 0 and that of any 2*2 gate is the same, which is 1.

F. *Hardware Complexity*

Hardware complexity refers to the total number of logical calculation (TC) in a circuit. The hardware complexity (HC) is determined by counting the number of EX-OR operations, number of AND operations number of NOT operations and number of OR operations.

To compute the hardware complexity of the reversible circuits; assuming.

α - no. of two input EX-OR gate operations

β - no. of two input AND gate operations

δ - no. of NOT gate operations

Ω - no. of OR operations

T - total logical operations.

The total logical calculation T be given as the sum of AND, OR, EX-OR and NOT calculations.

G. *Total On-Chip Power*

The power consumed internally within the FPGA, equal to the sum of device static power and dynamic power. It is also known as Thermal Power.

H. *Device Static Power*

The power from transistor leakage on all connected voltage rails and the circuits required for the FPGA to operate normally, post configuration. Device static power is a function of process, voltage and temperature. This represents the steady state, intrinsic leakage in the device.

I. *Dynamic Power*

The power consumed when all the inputs are active. It depends on voltage levels and logic and routing resources used.

J. *LUT*

A LUT (Look-Up Table) is a small asynchronous SRAM that is used to implement combinational logic. LUTs are usually read-only and their content can only be changed during FPGA configuration.

K. *Nets And Leaf Cells*

A net is a set of interconnected pins and wires. Leaf Cells could be standard cells from an ASIC library, or memories, macro cells, IP which would occupy space in the core area. These are the base cells that are used for further design/layout.

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 09, September-2020

III. REVERSIBLE LOGIC GATES

A. *NOT Gate*

This is a 1*1 reversible logic gate with one input and one output. The input A is mapped to the output P=A' as shown below in the Fig. 1.

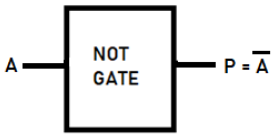

Fig. 1. NOT gate.

Fig. 2. Quantum representation of NOT gate.

B. *Feynman Gate*

This is a 2*2 reversible gate with two inputs and two outputs. The inputs (A, B) mapped to the outputs (P=A, Q=A^B) is shown in the Fig. 3.

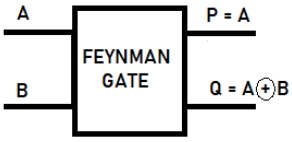

Fig.3. Feynman Gate.

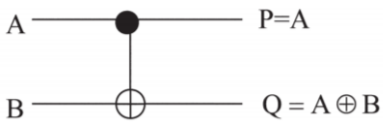

Fig. 4. Quantum representation of Feynman gate.

C. *Fredkin Gate*

This is a 3*3 Reversible gate with three inputs and three outputs. The inputs (A, B, C) mapped to the outputs (P=A, Q=A'B + A.C , R=A.B + A'.C) is shown in the Fig. 5.

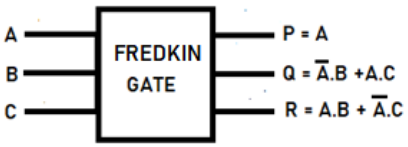

Fig. 5. Fredkin gate.

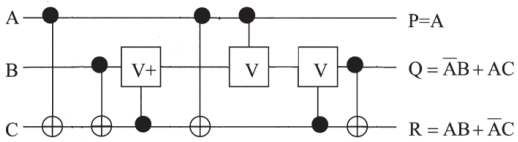

Fig. 6. Quantum representation of Fredkin gate.

D. *Toffoli Gate*

This is a 3*3 Reversible gate with three inputs and three outputs. The inputs (A, B, C) mapped to the outputs (P = A, Q = B, R = A · B ⊕ C) as shown in the Fig. 7.

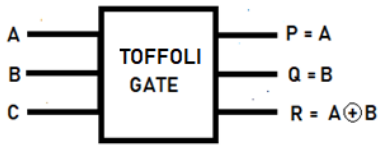

Fig. 7. Toffoli gate.

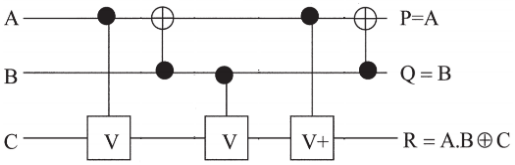

Fig. 8. Quantum representation of Toffoli gate.

E. *Peres Gate*

The Peres gate is a 3 inputs 3 outputs (3x3) reversible gate having the mapping (A, B, C) to (P=A, Q=A⊕B, R=(A.B)⊕C), where A, B, C are the inputs and P, Q, R are the outputs, respectively. It's also known as the New Toffoli Gate (NTG). It is constructed by one Toffoli and one Feynman gate. It has a quantum cost of 4.

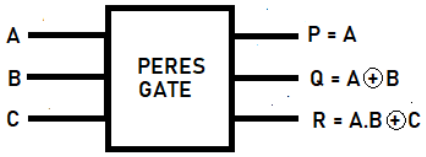

Fig. 9. Peres gate.

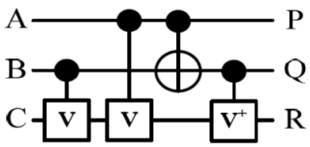

Fig. 10. Quantum representation of Peres gate.

F. *DKG Gate*

This is a 4*4 Reversible gate with four inputs and four outputs. The inputs (A, B, C, D) mapped to the outputs (P=B, Q=A'.C+ A.D' , R=A.^ B.C ^ D ^C.D, S=B^C*D) is shown in the Fig. 11.

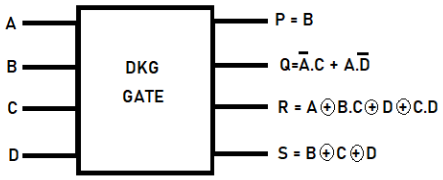

Fig. 11. DKG gate.

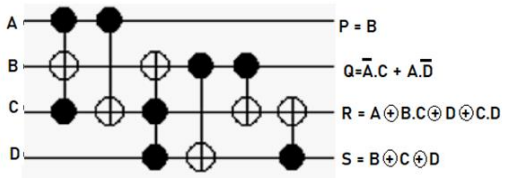

Fig. 12. Quantum representation of DKG gate.

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 09, September-2020

G. WG Gate

This is a 4*4 Reversible gate with four inputs and four outputs. The inputs (A, B, C, D) mapped to the outputs (P=A, Q=A + B + D, R=A. + B + C, S=(A⊕D ⊕ B) .(A ⊕ D ⊕ C) ⊕ (A ⊕D)) is shown in the Fig. 13.

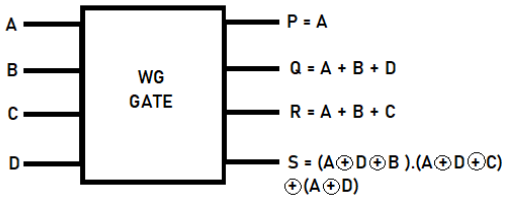

Fig. 13. WG gate.

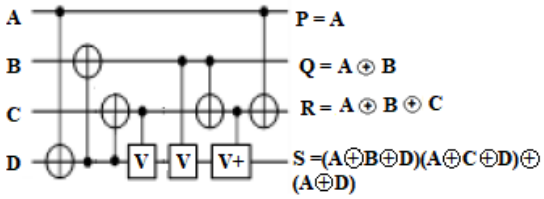

Fig. 14. Quantum representation of WG gate.

H. HNG Gate

This is a 4*4 Reversible gate with four inputs and four outputs. The inputs (A, B, C, D) mapped to the outputs (P=A, Q=B, R=A ⊕ (B ⊕ C), S=A ⊕ B .C ⊕A.B) is shown in the Fig. 15.

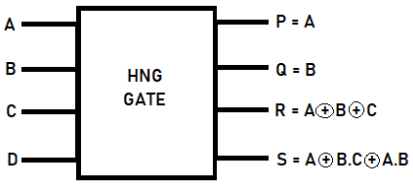

Fig. 15. HNG gate.

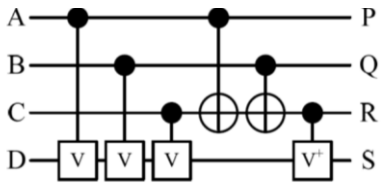

Fig. 16. Quantum representation of HNG gate.

I. TR Gate

This is a reversible gate that has 3 inputs and 3 outputs. The inputs (A, B, C) are mapped to the outputs (P=A, Q=A ⊕ B, R= (A.B') C).

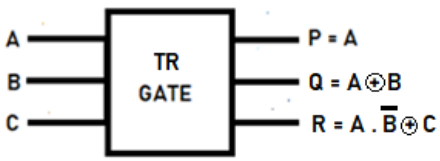

Fig 17. TR gate.

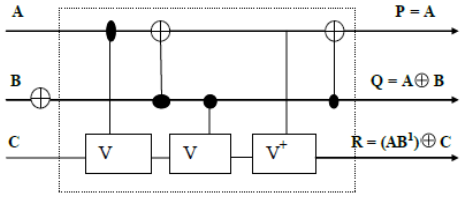

Fig. 18. Quantum representation of TR gate.

TABLE 1
Quantum cost and hardware complexity of reversible logic gates

GATE	Quantum cost	Hardware Complexity
NOT	1	δ
FEYMAN	1	α
FREDKIN	5	4β+2 δ +2 Ω
TOFFOLI	5	α+β
PERES	4	2α+β
DKG	6	5α+4 β+2 δ+ Ω
HNG	6	4 α+2β
TR	6	2α+β+ δ
WG	7	6 α +4 Ω

IV. DESIGN OF ADDER/SUBTRACTOR

A. Adder/Subtractor

An adder/subtractor is a circuit that can perform either addition or subtraction by varying a control input. By combining both adder and subtractor circuits to form a single circuit, considerable area can be saved on the silicon wafer. Adder/subtractor circuits form an integral part of the arithmetic unit of the ALU of the data processing system. The ALU uses this circuit to perform addition, addition with carry, increment, subtraction, decrement, etc. Dedicated Adder/Subtractor circuits are required in several Digital Signal Processing applications.

B. Existing Design 1

In this design, five Feynman gates, two Fredkin gates, and a TR gate are required to realize a full adder/subtractor circuit. By setting the control input Ctrl to logic 0, addition operation can be performed and by setting the control input to logic 1, subtraction operation can be performed. One bit full adder/subtractor is shown in Fig. 20 where the A, B, and Cin are the operands, Ctrl is the control input and outputs are S/D(sum/difference) and C/B (carry/borrow). This design incurs a quantum cost of 21. There are five garbage outputs (g1 to g5) and three ancilla inputs. By cascading one-bit full adder/subtractor circuits, ripple carries adder/ ripple borrow subtractor of different bit lengths can be obtained. The circuit diagram of existing design 1 is shown in Fig 19. RTL schematics of existing design 1 for bit lengths 1 and 8 is shown in Fig. 20 and Fig. 21.

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 09, September-2020

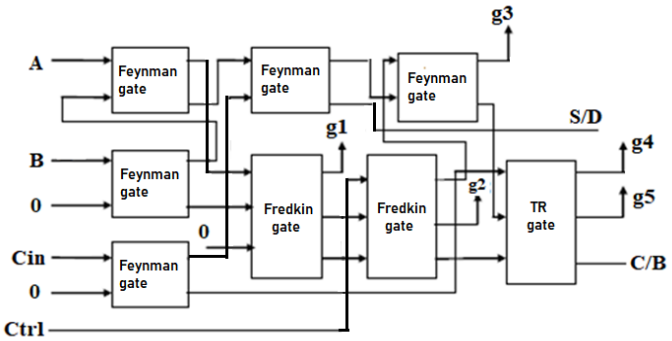

Fig. 19. Circuit diagram of full adder/subtractor circuit based on existing design 1.

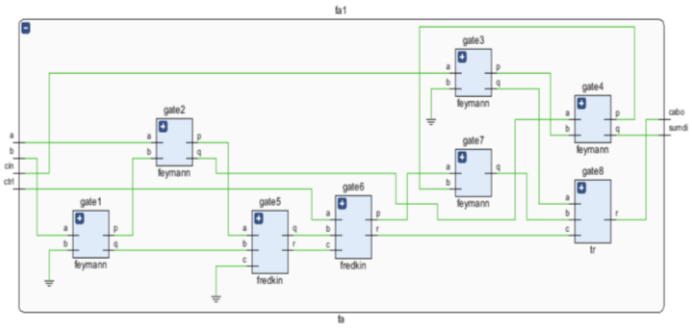

Fig. 20. RTL Schematic of existing design 1 based full adder/subtractor.

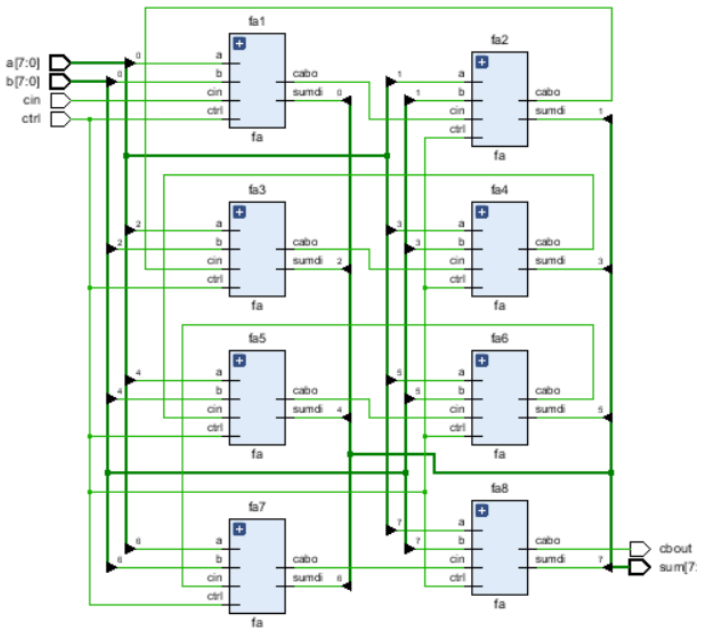

Fig. 21. RTL Schematic of existing design 1 based 8-bit ripple carry adder/ ripple borrow subtractor.

C. *Existing design 2*

A full adder/subtractor can be constructed by using a single WG gate. The mode of operation can be selected by configuring the D input pin as in the Fig. 13. When D=0, it acts as a full adder and when D=1, it acts a full subtractor. The outputs R and S produce sum/difference and carry/borrow, while the outputs P and Q are garbage outputs. This design incurs a quantum cost of 7. A n bit ripple carry adder/borrow subtractor requires n WG gates incurring a quantum cost of 7n. RTL Schematic of WG gate full adder/subtractor is shown in Fig. 22. The circuit diagram of existing design 2 is shown in Fig. 23. RTL schematic of 8 bit RCA/RBS based on existing design 2 is shown in Fig. 24.

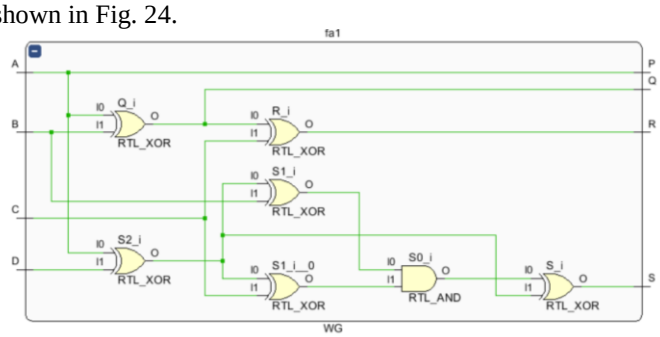

Fig. 22. RTL Schematic of WG gate full adder/subtractor.

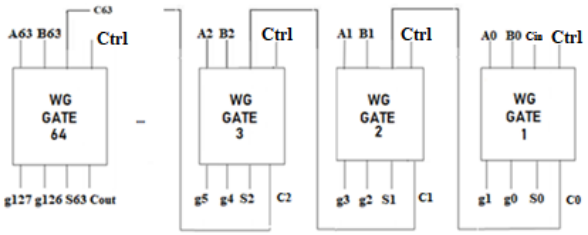

Fig. 23. Circuit diagram of existing design 2 based 64 bit ripple carry adder/ ripple borrow subtractor.

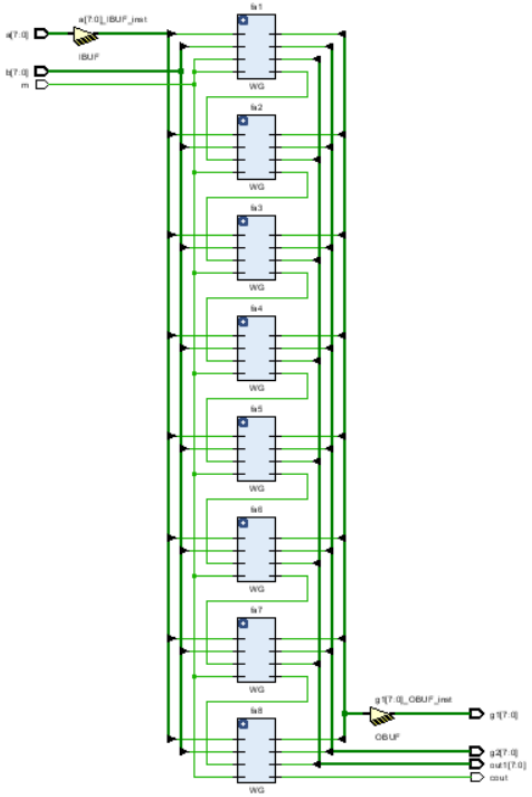

Fig. 24. RTL Schematic of existing design 2 based 8 bit ripple carry adder/ ripple borrow subtractor.

D. *Proposed design*

In this design, two Feynman and two Peres gates are used in constructing a full adder/subtractor. By setting the control input to logic 0, addition operation can be performed and by setting the control input to logic 1, subtraction operation can be

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 09, September-2020

performed. The proposed design incurs a quantum cost of 10. There are three garbage outputs and one constant input. By cascading one-bit adder/subtractor circuits, ripple carry adder/ ripple borrow subtractor of different bit lengths can be obtained. Fig. 25 shows the circuit diagram of the proposed design of the adder/subtractor circuit. The circuit diagram of the proposed design is shown in Fig. 25. RTL Schematic of the proposed design is shown in Fig. 26. RTL schematic of 8 bit RCA/RBS based on existing design 2 is shown in Fig. 27.

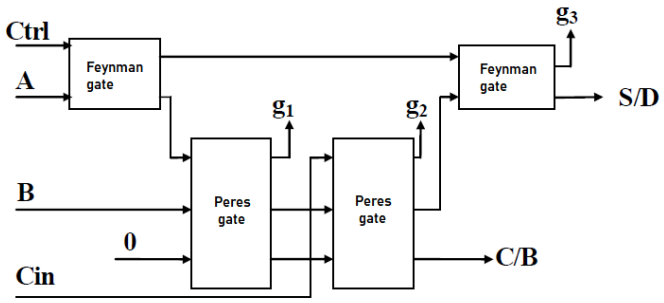

Fig. 25. Circuit diagram of proposed design adder/subtractor circuit.

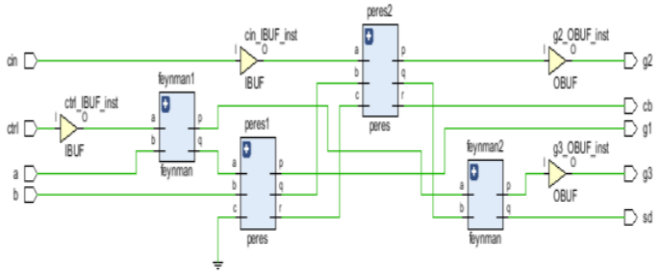

Fig. 26. RTL Schematic of proposed design adder/subtractor circuit.

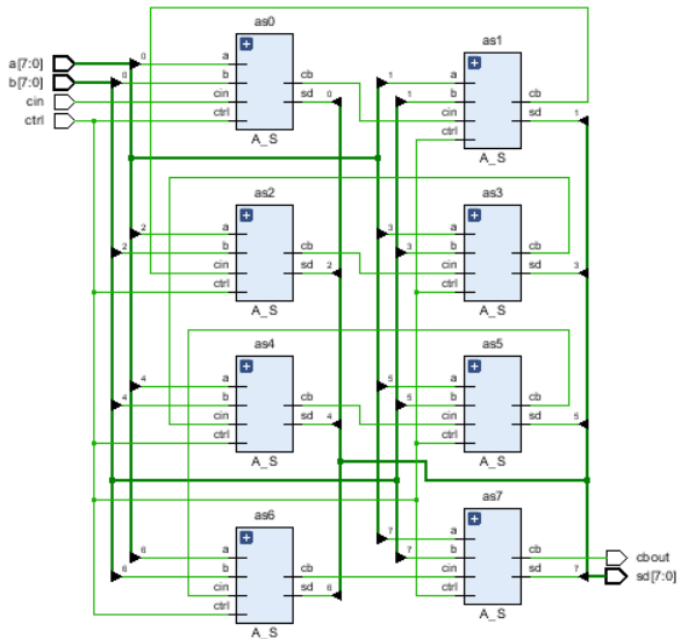

Fig. 27. RTL Schematic of proposed design 8 bit ripple carry adder/ ripple borrow subtractor.

V. SIMULATION AND RESULTS

A. *Existing design 1*

The simulation results of different bit lengths of existing design 1 from Xilinx Vivado tool are provided in table 2. The power report and FPGA utilization parameters report of existing design 1 is shown in Fig. 28 and Fig. 29. Waveforms of addition and subtraction of 64 bit inputs using existing design 1 is shown in Fig. 30 and Fig. 31.

TABLE 2
Simulation results of different bit lengths of existing design 1 from Xilinx Vivado tool

	1 bit	8 bit	16 bit	32 bit	64 bit
Gate Count	8	64	128	256	512
Garbage Output	5	40	80	160	320
Quantum Cost	21	165	336	672	1344
Total On chip Power (in W)	0.105	0.107	0.109	0.114	0.124
Static Power (in W)	0.104	0.104	0.104	0.104	0.105
Dynamic Power (in W)	<0.001	0.002	0.005	0.010	0.019
Logic Power (in W)	<0.001	<0.001	<0.001	<0.001	<0.001
Delay (in ns)	1.093	3.623	5.061	10.897	19.121
Nets	12	57	135	291	584
Leaf Cells	8	39	101	225	484
LUTs	1	12	40	94	195

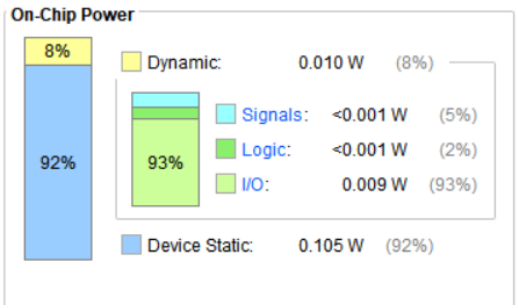

Fig. 28. Power report of existing design 1 based 32 bit RCA/ RBS.

Name	Slice LUTs (53200)	Bonded IOB (200)
addersub	94	99

Fig. 29. FPGA utilization parameters for existing design based 32 bit RCA/ RBS.

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 09, September-2020

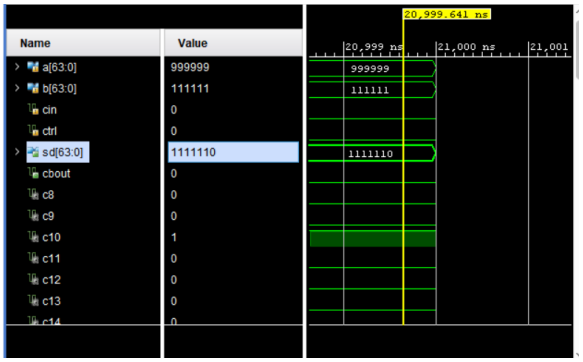

Fig.30 . Addition of 64 bit inputs A and B by existing design 1 RCA/ RBS.

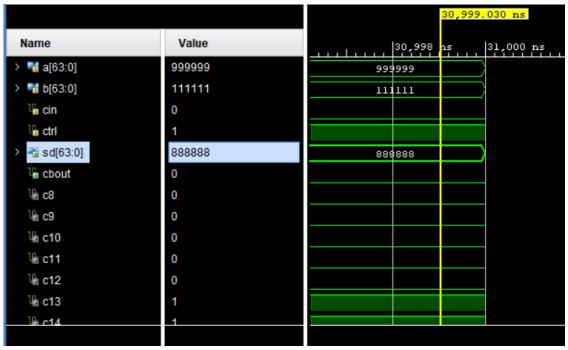

Fig. 31. Subtraction of 64 bit inputs A and B by existing design 1 RCA/ RBS.

B. *Existing design 2*

The simulation results of different bit lengths of existing design 2 from Xilinx Vivado tool are provided in table 3. The power report and FPGA utilization parameters report of existing design 2 is shown in Fig. 32 and Fig. 33. Waveforms of addition and subtraction of 64 bit inputs using existing design 2 is shown in Fig. 34 and Fig. 35.

TABLE 3

Simulation results of different bit lengths of existing design 2 from Xilinx Vivado tool

	1 bit	8 bit	16 bit	32 bit	64 bit
Gate Count	1	8	16	32	64
Garbage Output	2	16	32	64	128
Quantum Cost	7	56	112	224	448
Total On-chip Power (in W)	0.105	0.109	0.113	0.122	0.138
Static Power (in W)	0.104	0.104	0.104	0.105	0.105
Dynamic Power (in W)	0.001	0.004	0.009	0.017	0.034
Logic Power (in W)	<0.001	<0.001	<0.001	<0.001	<0.001
Delay (in ns)	1.174	3.726	6.438	11.790	22.494
Nets	13	79	155	307	611
Leaf Cells	10	62	122	242	482
LUTs	1	12	34	78	160

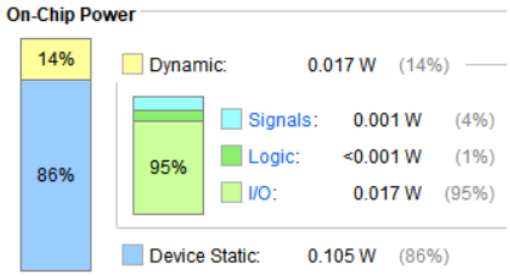

Fig. 32. Power report of existing design 1 based 32 bit RCA/ RBS.

Fig. 33. FPGA utilization parameters for existing design 2 based 32 bit RCA/ RBS.

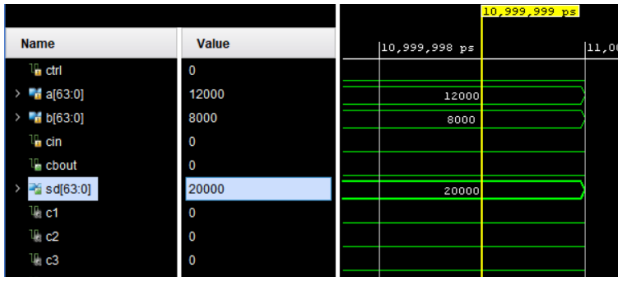

Fig. 34. Addition of 64 bit inputs A and B by existing design 2 RCA/ RBS.

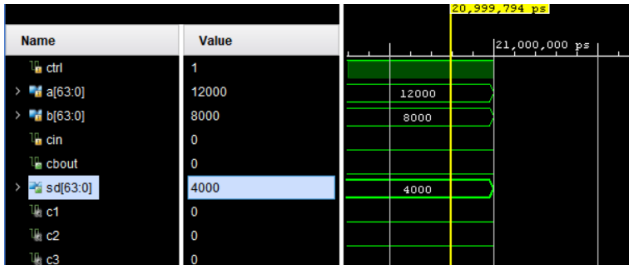

Fig. 35. Subtraction of 64 bit inputs A and B by existing design 2 RCA/ RBS.

C. *Proposed Design*

The simulation results of different bit lengths of the proposed design from Xilinx Vivado tool are provided in table 4. The power report and FPGA utilization parameters report of the proposed design is shown in Fig. 37 and Fig. 38. Waveforms of addition and subtraction of 64 bit inputs using the proposed design is shown in Fig. 39 and Fig. 40.

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 09, September-2020

TABLE 4

Simulation results of different bit lengths of the proposed design from Xilinx Vivado tool

	1 bit	8 bit	16 bit	32 bit	64 bit
Gate Count	4	32	64	128	256
Garbage Output	3	24	48	96	192
Quantum Cost	10	80	160	320	640
Total On chip Power (in W)	0.105	0.106	0108	0.113	0.121
Static Power (in W)	0.104	0.104	0.104	0.104	0.105
Dynamic Power (in W)	<0.001	0.002	0.004	0.008	0.016
Logic Power (in W)	<0.001	<0.001	<0.001	<0.001	<0.001
Delay (in ns)	1.060	3.286	4.989	9.637	18.476
Nets	10	57	127	267	533
Leaf Cells	7	39	93	201	493
LUTs	2	15	31	63	127

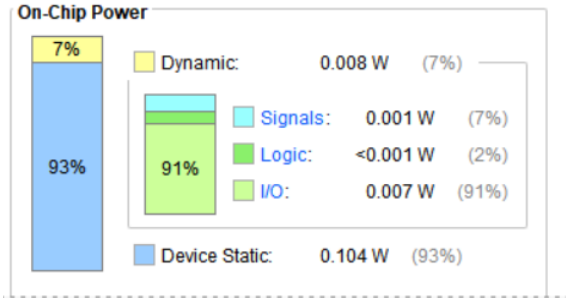

Fig. 37. Power report of proposed based 32 bit RCA/ RBS.

Fig. 38. FPGA utilization parameters for proposed design based 32 bit RCA/ RBS.

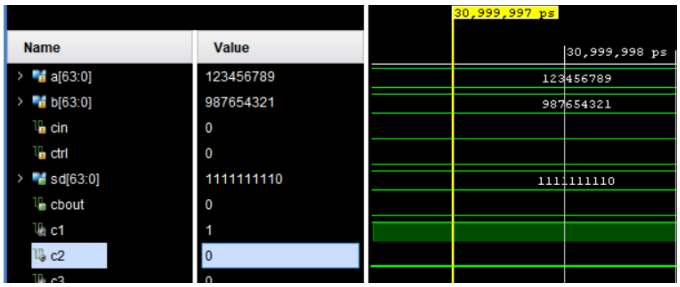

Fig. 39. Addition of 64 bit inputs A and B by proposed design RCA/ RBS.

Fig. 40. Subtraction of 64 bit inputs A and B by proposed design RCA/ RBS.

TABLE 5

Comparison of gate count, number of garbage outputs and quantum cost of the designs

	Gate Count	Garbage outputs	Quantum cost
Existing design 1	512	320	1344
Existing design 2	64	128	448
Proposed design	256	192	640

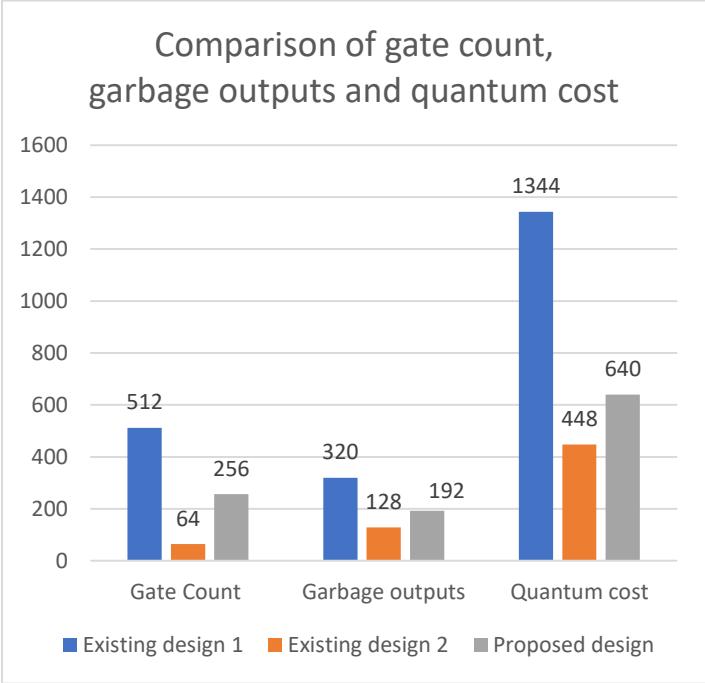

Fig. 41. Comparison chart of gate count, number of garbage outputs and quantum cost of existing and proposed designs.

Table 5 shows the comparison between the existing designs and the proposed design of the 64 bit reversible adder/subtractor designs. It can be depicted from the Fig. 41 and tables 2,3 and 4, that existing design 2 uses a fewer number of reversible logic gates, has fewer number of garbage outputs and incurs the least quantum cost in comparison with the other designs. Furthermore, it is understood that the difference between the proposed design and the existing design 2, in terms of quantum costs is not that significant and also it can be seen that the

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 09, September-2020

proposed design outperforms the existing design 1 by a good margin.

TABLE 6

Comparison of dynamic and total on-chip power of designs

	Dynamic power (mW)	Total on-chip power (mW)
Existing design 1	19	124
Existing design 2	34	138
Proposed design	16	121

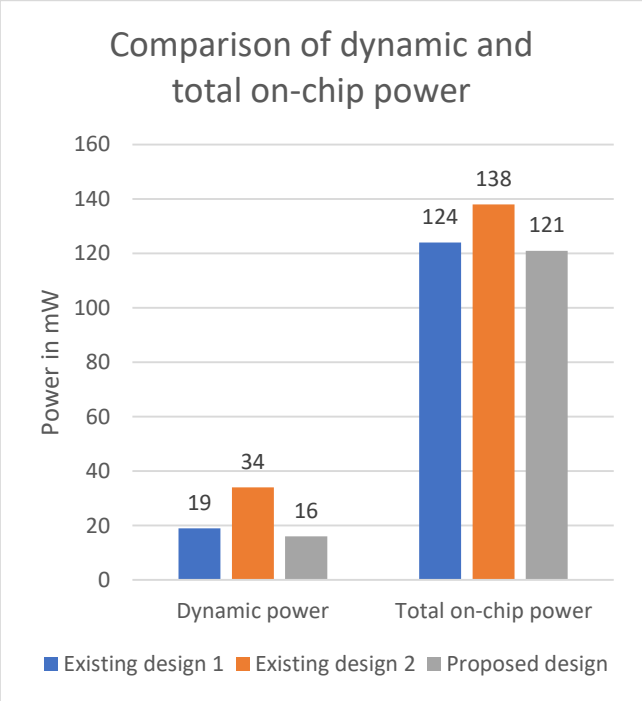

Fig. 42. Comparison of dynamic and total on-chip power of existing and proposed designs.

Table 6 shows the comparison between 64 bit reversible adder/subtractor circuits based on the designs in terms of dynamic and total on-chip power consumed. It can be seen from tables 2, 3, 4 and 6 that both static and logic power consumption of the designs remains fairly the same. It can be understood from the Fig. 42 that proposed design has the least dynamic power consumption in comparison with the existing designs. It can also be depicted that the total on-chip power of the proposed design is comparatively less than the existing designs.

TABLE 7

Comparison of numbers of LUTs, nets and leaf cells required by the designs

	Nets	Leaf cells	LUTs
Existing design 1	584	484	195
Existing design 2	611	482	160
Proposed design	533	493	127

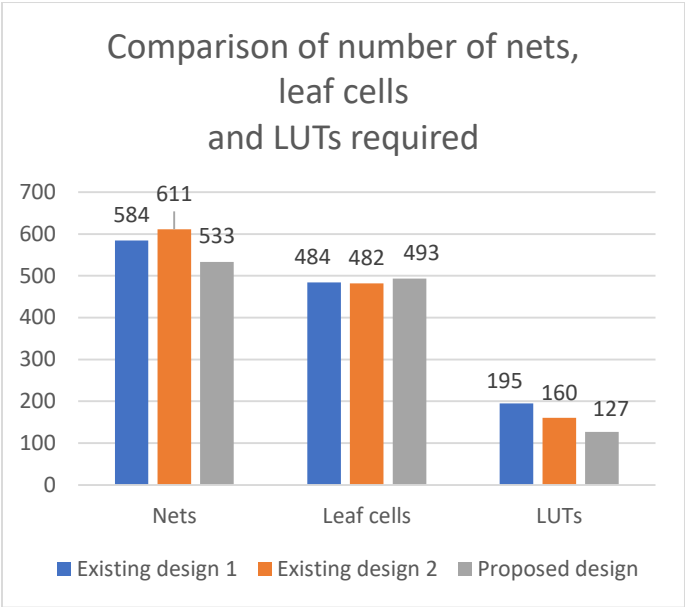

Fig. 43. Comparison chart of numbers of LUTs, nets and leaf cells required by existing designs and proposed design.

Table 7 shows the comparison between 64 bit reversible adder/subtractor circuits based on the designs in terms of the number of nets, leaf cells, and lookup tables required. It can be seen from Tables 2, 3, 4 and 7 that the proposed design outperforms both the existing designs.

TABLE 8

Comparison of delay incurred for 1,8,64 bit RCA/RBS for the designs

	1 bit (ns)	16 bit (ns)	64 bit (ns)
Existing design 1	1.093	5.061	19.121
Existing design 2	1.174	6.438	22.494
Proposed design	1.06	4.989	18.476

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 09, September-2020

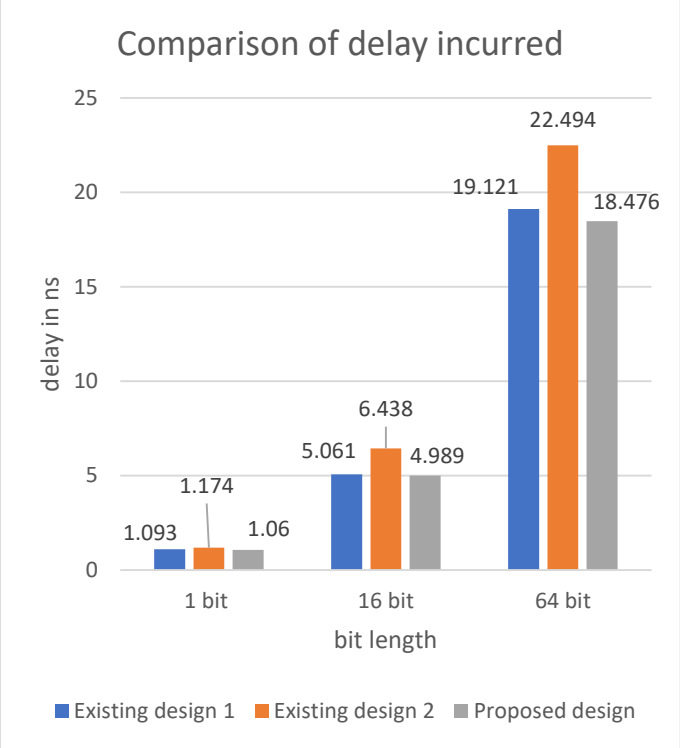

Fig. 44. Comparison chart of delay incurred for 1,8,64 bit RCA/RBS of the three designs

Based on Table 8, the comparison of delay between three designs of reversible adder/subtractor circuits is made. Based on the result as shown in Fig. 44 and in tables 2, 3, 4 and 8, it can be concluded that the proposed design shows higher reductions in propagation delay as compared to the existing designs.

VI. CONCLUSION

In this paper, a novel adder/subtractor design has been proposed. The proposed design is compared with two existing designs. These designs can be used to construct n-bit adder/subtractor circuits by cascading n 1-bit circuits. The designs have been simulated, analysed, and verified using Xilinx Vivado tool. They are implemented on Zedboard Zynq 7000 Evaluation and Development kit(xc7z020clg484-1). The performance and power consumption of the designs are compared with one another for different bit lengths(1,8,16,32,64). The quantum cost, number of garbage outputs, LUTs, nets and leaf cells are also evaluated. The simulation results illustrate that the proposed design outperforms the existing designs in terms of FPGA utilization parameters, power consumption and incurring delay. A complete reversible computer architecture can be designed with the help of the proposed design shortly. Reversible adder/subtractor circuits can soon find their application in calculators, mobile phones, and other ultra-low power-consuming devices. Furthermore, the proposed adder/subtractor design can serve as a basis for the design of sequential reversible circuits.

REFERENCES

[1] R. Landauer, “Irreversibility and heat generation in the computation process”, IBM journal of research and development, pp 183-191.

[2] C. H. Bennett, “Logically reversibility of computation”, IBM journal of research and development pp 525-532, NOV 1973.

[3] C. H. Bennett, “Notes on the history of reversible computation”, IBM Journal of Research and Development, 32 (1988), pp.16-23.

[4] T. Toffoli, “Reversible Computing”, Tech memo MIT/LCS/TM-151, MIT Lab for Computer Science 1980.

[5] R. Feynman, “Quantum mechanical computers”, Optics, News, 11, pp. 11-20, 1985.

[6] M. K. Bhagyalakshmi and M. K. Venkatesha, “An Improved Design of a Multiplier using Reversible Logic Gates”, International Journal of Engineering Science and Technology, vol. 2, pp. 3838-845, 2010.

[7] H. V. Ravish Aradhya, K. N. Muralidhara and B. V. Praveen Kumar, “Design of low power arithmetic unit based on reversible logic”, International Journal of VLSI and Signal Processing Applications, Vol. 1, Issue 1(30- 38), ISSN 2231-3133.

[8] Yvan Van Rentergen and Alexis De Vos, “Optimal design of a reversible full adder”, International Journal of unconventional computing, Vol. 1, pp. 339–355.

[9] W. David Pan and Mahesh Nalasani, “Reversible logic”, IEEE Potentials 24 (2005). 38-41.

[10] Himanshu Thapliyal and M. B. Srinivas, “Novel Design and Reversible Logic Synthesis of Multiplexer Based Full Adder and Multipliers”, 2008 Forty Eight Midwest Symposium on Circuits and Systems, vol. 2, pp. 1593 – 1596.

[11] Wadhawan and Prinkle, “Design of 8-Bit and 16-Bit Adder-Subtractor with Optimized Power and Quantum Cost”, International Journal for Research in Applied Science and Engineering Technology, Volume 5 Issue VIII, August 2017.

[12] Krishnaveni, Dhulipala and M. A. Priya, “Novel Design Of Reversible Serial And Parallel Adder/Subtractor”, International Journal of Engineering Science and Technology, Vol. 3 No. 3 March 2011.

[13] V. Shukla, O. P. Singh, G. R. Mishra and R. K. Tiwari, “Performance parameters optimization and implementation of adder/subtractor circuit using reversible logic approach”, 2016 11th International Conference on Industrial and Information Systems (ICIIS), Roorkee, 2016, pp. 323-328.

[14] V. Nitin Krishna, “Design and analysis of Arithmetic and Logic Unit using Reversible Logic”, International Journal for Research in Applied Science and Engineering Technology (IJRASET), Volume 8, Issue III, Page No. 878-893, ISSN . 2321-9653, www.ijraset.com

[15] H. G. Rangaraju, U. Venugopal, N. Muralidhara and K. B. Raja, “Low Power Reversible Parallel Binary Adder/Subtractor”, International Journal of VLSI Design & Communication Systems. 1. 10.5121/vlsic.2010.1303.

[16] Riya and Amandeep Singh Bhandari, “Design and Implementation of 8-Bit Low Power Parallel Adder/Subtractor Circuit Using Reversible Computing”, International Journal of Engineering Development and Research, Volume 6, Issue 3, ISSN. 2321-9939.