Design and Analysis of Topologically Compressed Flip Flop With Maximum Power Saving

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***Abstract*— This work proposes the Topologically Compressed Flip-Flop (TCFF), an extremely low-power flip-flop. The decreases power dissipation compared to traditional flip flops. Among the flip-flops that have been previously reported, this one has the largest power decrease ratio. The decrease is obtained by using the topological compression technique, which involves combination of transistors that are conceptually equivalent to an unusual latch structure. Only three, very few transistors were used, and they were all linked. The strength of the clock signal is considerably reduced, and the transistor count ensures that the overall cell area is comparable to that of conventional flip-flops.**

Keywords—Flip-Flop, Power saving, Topology, Delay, VLSI

I. INTRODUCTION

The electronic market is constantly growing. In recent years, the development of many types of electronic gadgets or healthcare-related instruments has flourished, in addition to the traditional smartphones, tablets, personal computers and digital cameras. Power reduction is a major concern in these battery-operated devices, and LSI power reduction is becoming more and more popular. Various types of circuit techniques have previously been presented using this backdrop. In very large-scale integration (VLSI), random logic often consumes greater than 50% of the power, with flip-flops accounting for half of this consumption. So many flip-flops consuming less power have been hurriedly developed within the last ten years.

However, because of its well-proportioned area of cell, power, and the performance, the conventional flip-flop is still the one that is most frequently utilised in real chip design. In order to accomplish all the objectives, including power decrease without sacrificing area of the cell or performance in terms of timing parameters, this study will provide a solution.

II. BACKGROUND

A. Adaptive Coupling flip flop (ACFF)

The 6-transistor memory cell serves as the foundation for the adaptive-coupling type FF (ACFF) [1]. With regard to decrease the number of transistors related to clock in this circuit, the single-channel transmission gate including an extra dynamic circuit is used in this circuit instead of the double channel transmission gate, which is more typical. However, because this circuit uses many single channel transmission gates of various kinds linked to the same clock signal on the identical data line, variations in the input clock skew are easily able to alter the delay. Furthermore, changes in the process have a significant impact on the properties of dynamic circuits and single-channel transmission-gate circuits. As a result, it can be challenging to optimise them, and performance degradation at different process corners is a problem.

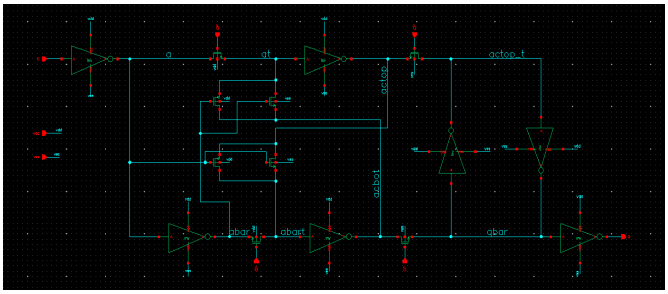

Fig. 1. Adaptive-coupling flip-flop (ACFF).

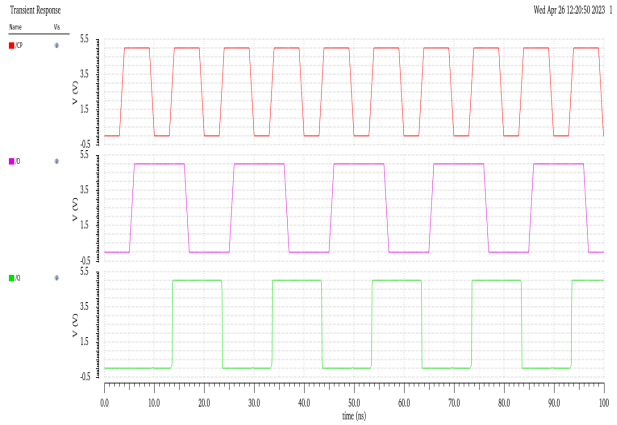

Fig. 2. Waveform on VIRTUOSO simulation.

B. Transmission Gate Flip Flop(TGFF)

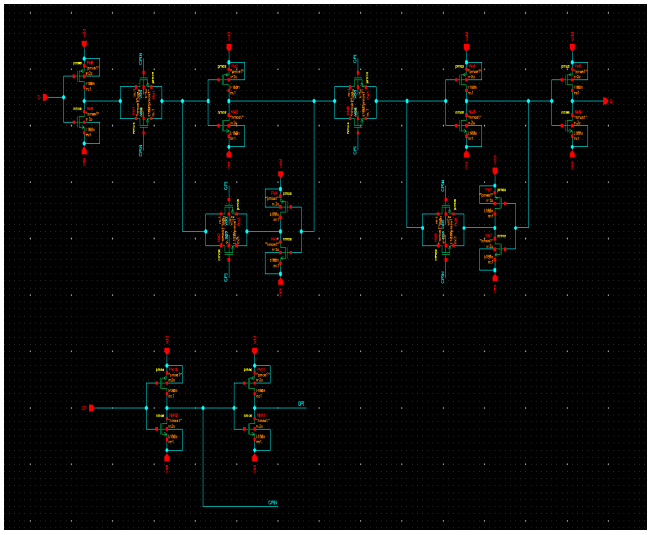

Fig. 3. Conventional transmission-gate flip-flop (TGFF).

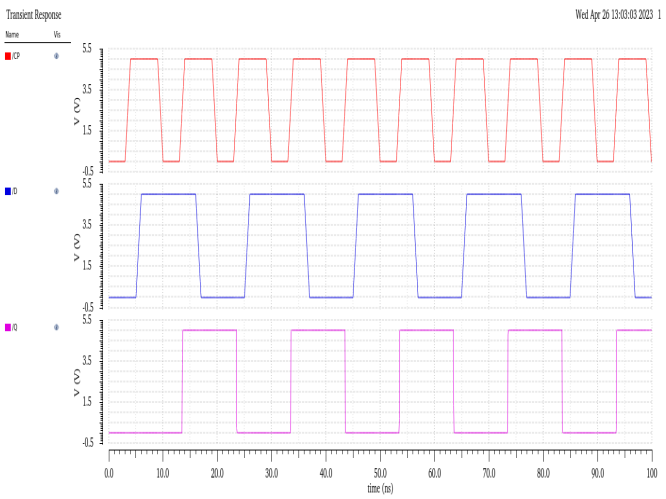

Fig. 4. Waveform on VIRTUOSO simulation

The fig 3. given demonstrates conventional transmission gate flipflop (TGFF) [2]. There are 12 clock related transistors in this conventional flipflop design. This transmission gate flipflop[2] is most commonly used as the conventional flipflop circuit in most of the chip manufacturing industries.

III. DESIGN APPROACH

Even when there is little data activity, flip flops continue to use energy every clock cycle to charge and discharge the transistors' gate capacitances, which are coupled to the clock signal CP. Our design idea for improving low power is to lower the number of transistors using a clock by topologically compressing them. A technique called topological compression (TC) [3] is used to combine several transistors with the same logical action.

An attempt has been done to minimise the number of transistors, particularly those using clock signals, without introducing any pre-charge or dynamic circuit with regard to lower the power of the flip-flop while maintaining a similar cell area and comparable performance. The majority of the flip-flop's power is lost during the operation of transistors related to the clock, therefore reducing the number of transistors is a good way to prevent cell area growth and lower internal node load capacitance.

In the existing flip-flop shown in Fig. 3, number of transistors used in clocks 12. It is rather challenging to directly reduce the number of transistors used in clock from this circuit. One of the reasons is that the clock driver cannot be removed because transmission-gates require a dual phase clock signal. Another justification is to prevent the worsening of data transfer characteristics brought on by the use of single-channel MOS by building transmission-gates using both PMOS and NMOS.

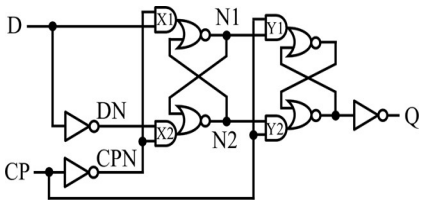

Fig. 5.Example of combinational type FF.

Consequently, we start with a circuit of combinational type as illustrated in Fig. 6 in place of a transmission-gate type circuit. We take into consideration a process that consists of the two phases below to decrease the number of transistors based on logical equivalence. As a first stage, we intend to create a circuit with two or more AND or OR logic components which are logically comparable that share the same set of input signals, particularly a clock signal. The next stage is to combine those components at the transistor level.

IV. PROPOSED TOPOLOGICALLY-COMPRESSED FLIP-FLOP

A. Compression at Transistor Level in Proposed flip-flop

We developed an unusually arranged flip-flop [4], which is shown in the following Fig. 7. The master and slave sections of this FF each have a different sort of latch. Reset-Set (RS) is a form of latch used in the slave, whereas single data input is used in the master. Two sets of functionally equivalent input AND logic, designated by the letters X1 and Y1 and X2 and Y2, respectively, are included in this circuit, which distinguishes itself by running on a single-phase clock.

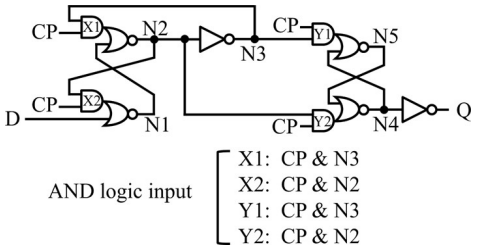

Fig. 6. Gate level schematic of proposed FF

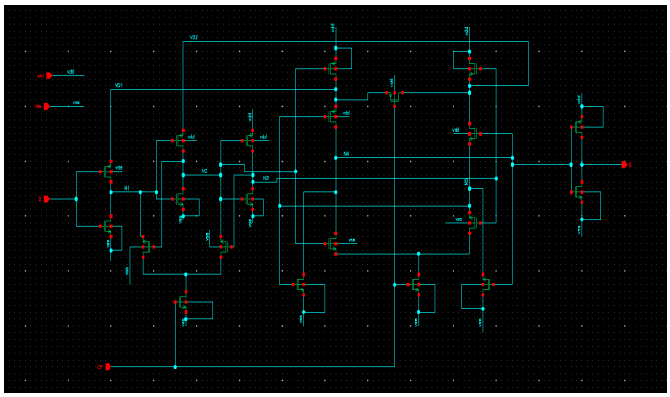

Fig. 7.Transistor level schematic of Fig. 6.

The schematic of Fig. 6 at the level of transistors is shown in Fig. 7. This design is used to combine transistors that are conceptually comparable. In the M1 and S1 blocks of Fig. 7's PMOS side, two transistor pairs may be shared as seen in Fig. 8. When anyone of the N3 or CP is Low, the shared common node changes to voltage level VDD, and PMOS transistors gated at nodes N1 and N4 control the nodes N2 and N5, respectively [2]. When both N3 and CP are high, NMOS transistors are used to draw down the N2 and N5 nodes and gate them to the VSS.

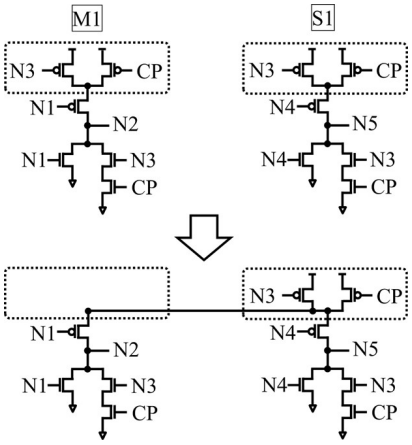

Fig. 8. Merging of transistors in PMOS side.

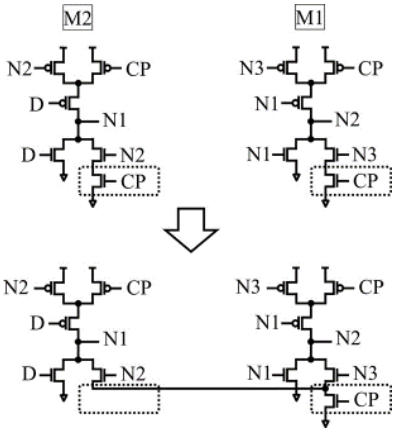

Fig. 9. Merging of transistors in NMOS side.

The two pairs of PMOS transistors of blocks M2 and S2 are common to blocks M1 and S1. Transistors with conceptually comparable operations on the NMOS side can also be shared. In blocks M1 and M2 of Fig. 9, two transistors can be shared. Also, the transistors of node S1 and node S2 are common.

Since the nodes N2 and N3 are logically opposite to each other, the input transistors CP shown in Fig. 10 can be connected in S1 and S2 further along the PMOS side. Both nodes are at the high voltage level VDD and anyone of the N2 or N3 is active when the CP is low [2]. Both nodes have an independent voltage level when CP is high as shown in fig 11. The transistors tied to the CP input are common and connected as shown in Fig. 10 to explain this behavior. To connect S1 and S2, the transistor associated with the CP input acts as a switch.

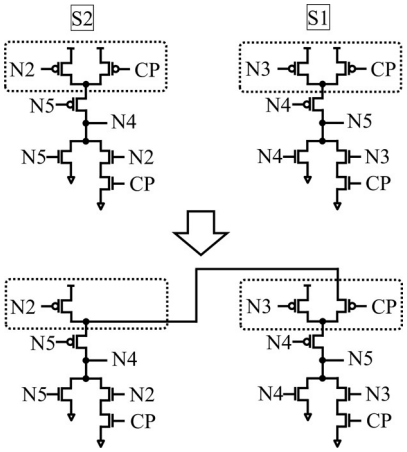

Fig. 10.Further merging of transistors in PMOS side.

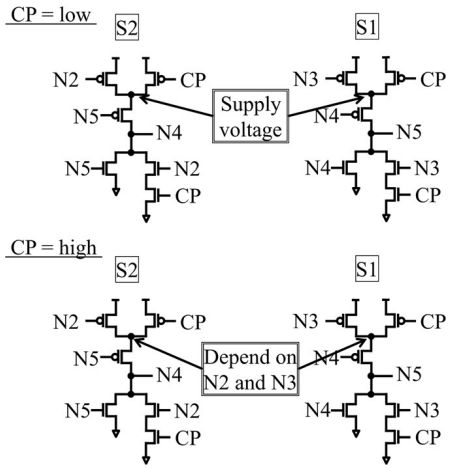

Fig. 11. The state of internal nodes.

The process described above results in the circuit illustrated in Figure 12. The original circuit in Fig. 7 had seven more transistors than this design does. There are only three transistors associated with the clock. Notably, neither dynamic circuit or pre-charge circuit exists; as a result, no additional power dissipation occurs. The Topological Compression (TC) methodology is the name of this compression method. When the TC-Method [6] is applied, the flip-flop is known as a topologically-compressed flip-flop (TCFF).

B. Cell Operation

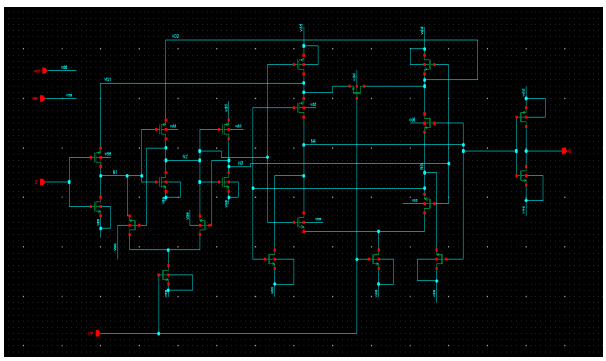

Fig. 12. Transistor level schematic of topologically-compressed flip-flop (TCFF).

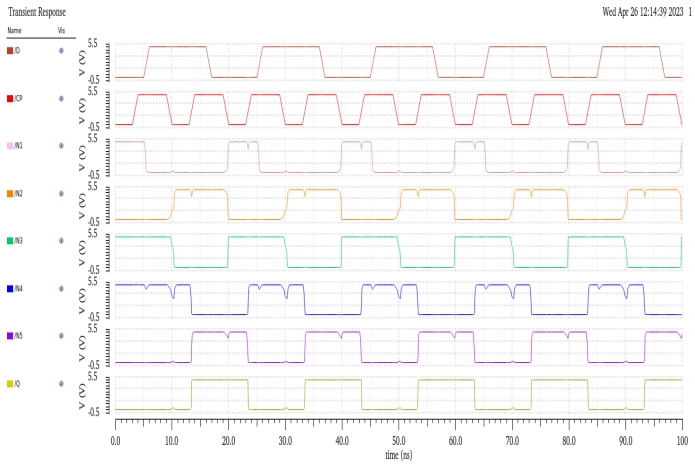

Fig. 13. Waveform on VIRTUOSO simulation.

The circuit depicted in Fig. 12 has simulated waveforms given in Fig. 13 [5]. In Fig. 12, the master latch switches to the data input mode when the CP signal is low, turning on the PMOS transistor connected to CP. VD1 and VD2 are both pushed up to power supply level, and the master latch stores the input data from D. When CP is set high, the NMOS transistor attached to it turns on and the NMOS transistor that is connected to PMOS transistor turns off, causing the slave latch to switch to the data output mode. The data present in the master latch is output to Q in this situation after being transferred to the slave latch.

Each node is in full static and swing during this procedure [7]. The master latch and the slave latch alternately become active, preventing the current from the power source from flowing into both latches simultaneously. As a result, even when several transistors are shared without a corresponding increase in transistor size, timing degradation has a little impact on cell performance.

It can be observed that the proposed topologically compressed flip flop on VIRTUOSO simulation is giving the same output waveforms as that of the adaptive coupling flip flop and the transmission gate flip flop. Also, the number of transistors used in the proposed flip flop after topological compression is less than the number of transistors in the conventional flip flop designs. Hence, the proposed flip flop can be used in place of the conventional transmission gate flip flop and the adaptive coupling flip flop.

V. SIMULATION

In VIRTUOSO simulation using 180 nm CMOS technology, the performance of TCFF is shown. Each transistor in all the three flip-flop topologies, including TCFF (Topologically Compressed flip-flop), is used with the same transistor size for comparison with other flip-flops in an effort to recreate identical conditions. For the purposes of comparison, some standard values for transistor sizes have been taken into consideration: 2000nm for width and

180nm for length in NMOS, and 2000nm for width and 180nm for length in PMOS.

A. Table

The normalised power dissipation in comparison to different FFs is shown in Fig. 14. In practically all categories of data activity, TCFF uses the least amount of electricity. Due to its essentially fully-static function, TCFF can function at 0.6V supply voltage. Even though TCFF uses a single phase clock signal to operate. It does not require a clock buffer. A clock pin directly drives the circuit.

The power and delay measure for the topologically compressed flip flop has been done using the calculator tool available in the virtuoso simulation window

TABLE I

PERFORMANCE COMPARISON OF TCFF AND OTHER FFS

Flip-flop topologies	*Parameters*		
	No. of transistors	***Delay in sec***	***Avg. power in watts***
ACFF	22	20.0×10^{-9}	2.319
TGFF	24	19.96×10^{-9}	2.323
TCFF	**21**	**19.85×10^{-9}**	**2.344**

Fig. 14 Power comparison of FFs

The above TABLE I represents the number of transistors, delay and average power comparisons between the ACFF, TGFF and TCFF. In the table we can observe that the proposed TCFF is having 21 transistors, the conventional TGFF has 24 transistors and the ACFF has 22 transistors. The average output power of the TCFF is 2.344watts which is more than the average output power measure of conventional flip flop designs ACFF and TGFF that are analyzed in the paper. Even the clock to Q delay is also less in the TCFF when compared to ACFF and TGFF. We can conclude that the proposed TCFF having 21 transistors with delay of 19.85ns and average power of 2.344watts, represents that the proposed TCFF is better than the conventional ACFF and TGFF with less delay and more output power.

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CONCLUSION

Topologies of adaptive coupling flipflop, transmission gate flip-flop and topologically compressed flip-flop are thoroughly analyzed. The delay and power comparison of the designs can be done across all technology nodes and all process conditions.

With topological compression design technique, a very low-power FF called the TCFF is suggested. Comparatively speaking, the least power dissipation is seen in TCFF throughout practically the whole data activity spectrum. TCFF uses less power than TGFF when there is zero data activity without an increase area overhead. Without sacrificing speed, it is simple to adapt the TCFF architecture to different FF types.

Hence, it can be concluded that the proposed topologically compressed flip flop can replace the conventional flip flop designs that are widely used in chip manufacturing industries.

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