Design and Control of Interline Unified Power Quality Conditioner for Power Quality Disturbances

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Abstract

Proliferation of electronic equipment in commercial and industrial processes has resulted in increasingly sensitive electrical loads to be fed from power distribution system which introduce contamination to voltage and current waveforms at the point of common coupling (PCC) of industrial loads.This paper proposes a new connection for a UPQC to improve the Power Quality (PQ) of two feeders in a distribution system. Interline Unified Power Quality Conditioner (IUPQC), specifically aims at the integration of series VSC and Shunt VSC to provide high quality power supply by means of voltage sag compensation, harmonic elimination and power factor correction in a power distribution network, so that improved PQ can be made available at the point of common coupling . The structure, control and capability of the IUPQC are discussed in this paper. The efficiency of the proposed configuration has been verified through simulation using MATLAB/SIMULINK.

I. Introduction

PQ problems have received a great attention nowadays because of their ill effects. Nowadays most of the domestic and industrial equipment are corrupting the quality of the delivered power. The most common PQ problem is due to the utilization of modern semiconductor switching devices more and more in a wide range of applications in distribution networks , particularly in domestic and industrial loads These semiconductor devices present nonlinear operational characteristics, which introduce contamination to voltage and current waveforms at PCC of industrial loads. Nowadays VSC based custom power devices are increasingly being used in custom power applications for improving the PQ of power distribution systems. Devices such as Distribution Static Compensator (DSTATCOM) and Dynamic Voltage Restorer (DVR) have already been in use. A DSTATCOM can compensate for distortion and unbalance in a load. A DVR an compensate for voltage sag/swell and distortion in the supply side voltage such that the voltage across a sensitive/critical load terminal is perfectly regulated. A UPQC can perform the functions of both DSTATCOM and DVR. The UPQC consists of two VSCs that are connected to a common DC bus. One of the VSCs is connected in series with a distribution feeder, while the other one is connected in shunt with the same feeder. The DC links of both VSCs are supplied through a common DC capacitor.

This paper presents the new connection for UPQC i.e., IUPQC which is the most sophisticated mitigating device for the PQ problems. It was firstly introduced to mitigate the current harmonics and voltage disturbances. The main aim of the IUPQC is to hold the voltages V_{t1} and V_{l2} constant against voltage sag/sell/any power disturbances in either of the feeders. Many contributions were introduced to modify the configurations and the control algorithms to enhance its performance. Most of the existing control algorithms which are employed to control IUPQC have some drawbacks. These drawbacks have significant influence on the performance of IUPQC.

II. IUPQC Connection

The single-line diagram of an IUPQC connected distribution system is shown in Fig. 1.

Two feeders, Feeder-1 and Feeder-2, which are connected to two different substations, supply the system loads L-1 and L-2. The supply voltages are denoted by V_{s1} and V_{s2}. It is assumed that the IUPQC is connected to two buses B-1 and B-2, the voltages of which are denoted by V_{t1} and V_{t2}, respectively. Further two feeder currents are denoted by i_{s1} and i_{s2} while the load currents are denoted by i_{l1} and i_{l2}. The load L-2 voltage is denoted by V_{l2}. The purpose of the IUPQC is to hold the voltages V_{t1} and V_{l2} constant against voltage sag/swell, temporary interruption and momentary interruption etc. in either of

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the two feeders. It has been demonstrated that the IUPQC can absorb power from one feeder (say Feeder-1) to hold V_{l2} constant in case of a sag in the voltage V_{s1}. This can be accomplished as the two VSCs are supplied by a common dc capacitor. The dc capacitor voltage control has been discussed here along with voltage reference generation strategy. Also, the limits of achievable performance have been computed. The performance of the IUPQC has been evaluated through simulation studies using MATLAB/SIMULINK.

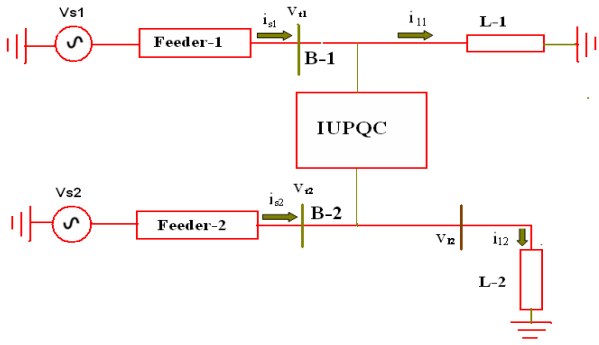

Fig. 1. Single-line diagram of an IUPQC distribution system

But basically IUPQC is nothing but the device UPQC kept in between two individual feeders, (called feeder-1 and feeder-2). UPQC consists of two back to back connected IGBT based voltage source bi-directional converters or VSCs (called VSC-1 and VSC-2) with a common DC bus. VSC-1 is connected in shunt with feeder-1 while VSC-2 is placed in series with the feeder-2. All the inverters are supplied from a common single DC capacitor and each inverter has a transformer connected at its output. The AC filter capacitors are also connected in each phase (Fig.1) to prevent the flow of the harmonic currents generated due to switching. The six inverters of the IUPQC are controlled independent.

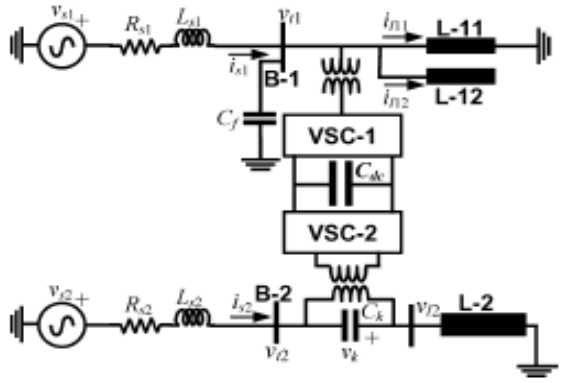

Fig. 2. Typical IUPQC connected in a distribution system.

An IUPQC connected to a distribution system is shown in Fig. 2, the feeder impedances are denoted by the pairs ($R_{s1,}$ L_{s1}) and ($R_{s2,}$ L_{s2}). It can be seen that the two feeders supply the loads L-1 and L-2. The load L-1 is assumed to have two separate components an unbalanced part (L-11) and a non-linear part (L-12). The currents drawn by these two loads are denoted by i_{l11} and i_{l12}, respectively. We further assume that the load L-2 is a sensitive load that requires uninterrupted and regulated voltage. The system parameters are mentioned in Table1.

Table 1: System parameters

System quantities	Values
System fundamental frequency	50Hz
Voltage source V_{s1}	11kv(L-L,rms), phase angle 0^0
Voltage source V_{s2}	11kv(L-L,rms), phase angle 0^0
Feeder-1 (R_{s1} + j2∏fL_{s1})	Impedance:3.05+j0.036Ω
Feeder-2 (R_{s1} + j2∏fL_{s2})	Impedance:3.05+j30.73Ω
Load L-11 Unbalanced RL component	Phase a: 24.2+j62.54 Ω Phase b: 36.1+j81.86 Ω Phase b: 48.2+j97.90 Ω
Load L-12 Non-linear component	A three-phase diode rectifier That Supplies a load of 250+j31.41Ω
Balanced load L-2 Impedance	95+j85.86 Ω

III. Design Considerations

The design considerations of IUPQC can be evaluated by using the following filtering systems

A. Active Filtering System

The active filtering system is based on a philosophy that addresses the load current distortion from a time domain rather than a frequency domain approach. The most effective way to import the distortive power factor in a non-sinusoidal situation is to use a nonlinear active device that directly compensates for the load current distortion. The performance of these active filters is based on three basic design criteria. They are:

1.The design of the power inverter (semiconductor switches, inductances, capacitors, dc voltage).

2.The PWM control method (hysterisis, triangular carrier, periodical sampling)

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3.Method used to obtain the current reference or the control strategy used to generate the reference template.

B. Design of Power Inverters

Inverter*:* Both series voltage control and shunt current control involve use of voltage source converters. Both these inverters each consisting of six IGBTs with a parallel diode connected in reverse with each IGBT are operated in current control mode employing PWM control technique

Capacitor*:* Capacitor is used as an interface between the two back to back connected inverters and the voltage across it acts as the dc voltage source driving the inverters. The IUPQC parameters are shown in Table2.

Table 2: IUPQC Parameters

System Quantity	Parameters
System fundamental frequency	50Hz
VSC-1 Single phase transforme	1MVA,3/11kv 10% leakage reactance
VSC-2 Single phase transforme	1MVA,3/11kv 10% leakage reactance
Filter capacitor (C_f)	490µf
Filter capacitor (C_k)	99µf
DC capacitor (C_{dc})	3000 µf

4. Control Strategy for IUPQC

A. Shunt Control Strategy

Shunt control strategy shown in Fig. 3 involves not only generating reference current to compensate the harmonic currents but also charging the capacitor to the required value to drive the inverters.

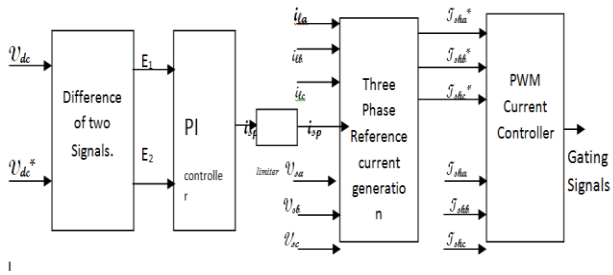

Fig. 3. Block diagram for generation of gating signals

PI Control

With a view to have a self regulated dc bus, the voltage across the capacitor is sensed at regular intervals and controlled by employing a suitable closed loop control. The DC link voltage, V_{dc} is sensed at a regular interval and is compared with its reference counterpart V_{dc} *. The error signal is processed in a PI controller. The output of the PI controller is denoted as $i_{sp(n)}$. A limit is put on the output of controller this ensures that the source supplies active power of the load and dc bus of the UPQC. Later part of active power supplied by source is used to provide a self supported DC link of the UPQC. Thus, the DC bus voltage of the UPQC is maintained to have a proper current control. Three phase reference supply currents (i_{sa}^*, i_{sb}^*, i_{sc}^*). Subtraction of load currents (i_{la}, i_{lb} and i_{lc}) from the reference supply currents (i_{la}^*, i_{lb}^*, i_{lc}^*) results in three phase reference currents (i_{sha}^*, i_{shb}^*, i_{shc}^*) for the shunt inverter.

These reference currents I_{ref} (i_{sha}^*, i_{shb}^*, i_{shc}^*) are compared with actual shunt compensating currents I_{act} (i_{sha}, i_{shb}, i_{shc}) and the error signals are then converted into (or processed to give) switching pulses using PWM technique which are further used to drive shunt inverter. In response to the PWM gating signals the shunt inverter supplies harmonic currents required by load. (In addition to this it also supplies the reactive power demand of the load). In effect, the shunt bi-directional converter that is connected through an inductor in parallel with the load terminals accomplishes three functions simultaneously. It injects reactive current to compensate current harmonics of the load. It provides reactive power for the load and thereby improve power factor of the system. It also draws the fundamental current to compensate the power loss of the system and make the voltage of DC capacitor constant. The subsystems of shunt controller and pwm signal generation subsystems are shown in Fig. 4 and Fig. 5.

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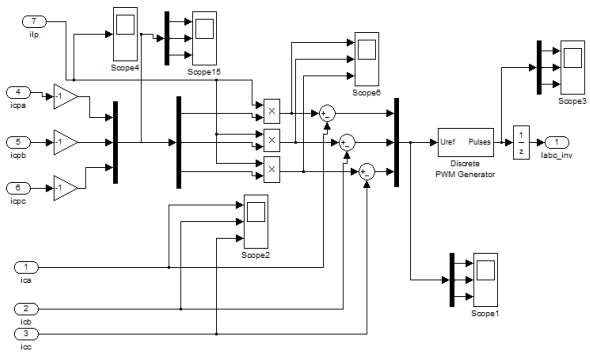

Fig. 4. PWM Shunt controller (Subsystem)

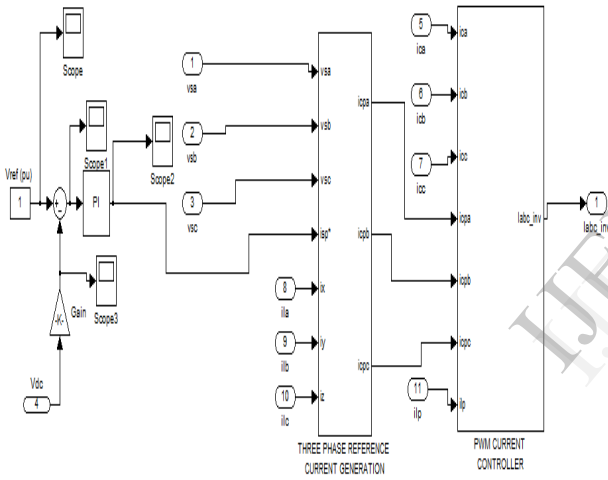

Fig. 5. Direct Shunt controller (Subsystem)

B. Series control strategy

The series controller could be a variable impedance, such as capacitor, reactor etc. Power electronics based variable source of main frequency, sub synchronous and harmonic frequencies to serve the desired need. In principle, all series controllers inject voltage in series with the line. Even variable impedance multiplied by a current flow through it, represents an injected series voltage in the line. The block diagram is shown in Fig. 6.

Fig. 6. Block diagram for generation of gating signals

The series inverter, which is also operated in current control mode, isolates the load from the supply by introducing a voltage source in between. This voltage source compensates supply voltage deviations such as sag and swell. In closed loop control scheme of the series inverter, the three phase load voltage (V_{la}, V_{lb}, V_{lc}) are subtracted from the three phase supply voltage (V_{sa}, V_{sb}, V_{sc}), and are also compared with reference supply voltage which results in three phase reference voltages (V_{la}^*, V_{lb}^*, V_{lc}^*). These reference voltages are to be injected in series with the load. By taking recourse to a suitable transformation, the three phase reference currents (i_{sea}^*, i_{seb}^*, i_{sec}^*) of the series inverter are obtained from the three phase reference voltages (V_{la}^*, V_{lb}^*, V_{lc}^*). The PWM generation subsystem of series controller shown in Fig. 7.

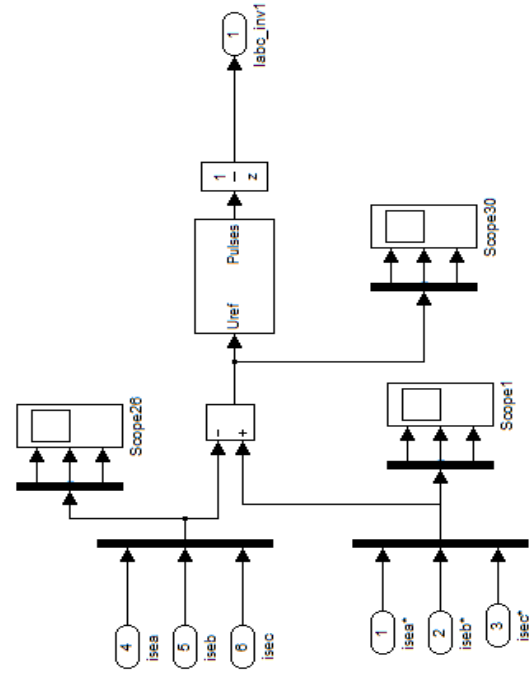

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Fig. 7. PWM Series controller (Subsystem)

These reference currents (i_{sea}^*, i_{seb}^*, i_{sec}^*) are fed to a PWM current controller along with their sensed counterparts (i_{sea}, i_{seb}, i_{sec}). The gating signals obtained from PWM current controller ensure that the series inverter meets the demand of voltage sag and swell, thereby providing sinusoidal voltage to load. Thus series inverter plays an important role to increase the reliability of quality of supply voltage at the load, by injecting suitable voltage with the supply, whenever the supply voltage undergoes sag. The series inverter acts as a load to the common DC link between the two inverters. When sag occurs series inverter exhausts the energy of the dc link. Thus, UPQC, unlike Dynamic Voltage Restorer, does not need any external storage device or additional converter (diode bridge rectifier) to supply the DC link voltage.

The direct series controller subsystem as shown in Fig.8

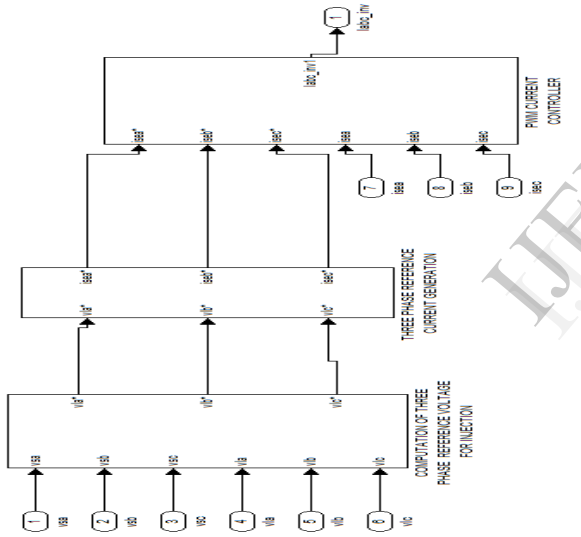

Fig. 8. Direct Series controller (Subsystem)

V. Model Equations of the IUPQC

A. Computation of Control Quantities of Shunt Inverter

The amplitude of the supply voltage is computed from the three phase sensed values as:

$v_{sm} = [\ 2/3(v_{sa}2 + v_{sb}2 + v_{sc}2)]^{1/2}$ (1)

The three phase unit current vectors are computed as:

$u_{sa} = v_{sa}/v_{sm}$; $u_{sb} = v_{sb}/v_{sm}$; $u_{sc} = v_{sc}/v_{sm}$; (2)

Multiplication of three phase unit current vectors (u_{sa}, u_{sb} and u_{sc}) with the amplitude of the supply current (i_{sp}) results in the three-phase reference supply currents as:

$i_{sa}^* = i_{sp}.u_{sa}$; $i_{sb}^* = i_{sp}.u_{sb}$; $i_{sc}^* = i_{sp}.u_{sc}$; (3)

To obtain reference currents, three phase load currents are subtracted from three phase reference supply currents:

$i_{sha}^* = i_{sa}^* - i_{la}$; $i_{shb}^* = i_{sb}^* - i_{lb}$; (4)

$i_{shc}^* = i_{sc}^* - i_{lc}$; (5)

These are the iref for Direct current control technique of shunt inverter. The iref are compared with iact in PWM current controller to obtain the switching signals for the devices used in the shunt inverter.

B. Computation of Control Quantities of Series Inverter

The supply voltage and load voltage are sensed and there from, the desired injected voltage is computed as follows:

$v_{inj}=v_s-v_l$ (6)

The magnitude of the injected voltage is expressed as:

$v_{inj}= |v_{inj}|$ (7)

Whereas, the phase of injected voltage is given as:

$\delta_{inj}= \tan(Re[v_{pq}]/Im[v_{pq}])$ (8)

for the purpose of compensation of harmonics in load voltage, the following inequalities are followed:

$v_{inj}<v_{injmax}$magnitude control; (9)

$0<\delta_{inj}<360^0$hase control; (10)

Three phase reference values of the injected voltages are expressed as:

$$V_{la}^*=\sqrt{2}v_{inj}\sin\ (wt+\delta_{inj}) \quad (11)$$

$$V_{lb}^*=\sqrt{2}v_{inj}\sin\ (wt+{}^{2\pi}/_{3}+\delta_{inj}) \quad (12)$$

$$V_{lc}^*=\sqrt{2}v_{inj}\sin\ (wt+{}^{2\pi}/_{3}+\delta_{inj}) \quad (13)$$

The three phase reference currents (iref) of the series inverter are computed as follows:

$i_{sea}^*= v_{la}^*/z_{se}$; $i_{seb}^* = v_{lb}^*/z_{se}$; $i_{sec}^* = v_{lc}^*/z_{se}$; (14)

The impedance zse includes the impedance of insertion transformer. The currents (i_{sea}^*, i_{seb}^*, i_{sec}^*) are ideal current to be maintained through the secondary winding of insertion transformer in order to inject voltages (V_{la}, V_{lb}, V_{lc}) thereby accomplishing the desired task of compensation of the voltage sag. The currents iref (i_{sea}^*, i_{seb}^*, i_{sec}^*) are compared with I_{act} (i_{sha}, i_{shb}, i_{shc}) in PWM current controller, as a result six switching signals are obtained for the IGBTs of the series inverter

VI. Operation Of IUPQC for Different Power Distrubances

Now, the performance of IUPQC has been evaluated considering various disturbance conditions.

Table. 3: IEEE Standard Power Quality Disturbances

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	Type of Interrup tion	Duration	P.U Value
1. Impulsive	Sag	0.5 30 cycles	0.1 0.9 p.u
	Swell	0.5-30 cycles	1.1-1.8 p.u
2. Momentary	Sag	20-30cycles	0.1-0.9 p.u
	Swell	20-30cycles	0.1-0.9 p.u
3. Temporary	Sag	30 40 cycles	<0.1 p.u
	Swell	30-40 cycles	1.1-1.2 p.u

The table shows that various IEEE Standard Power Quality disturbances, which are being applied to IUPQC and analyzing the performance.

IUPQC with series and shunt PI Controller:

A 3-phase supply voltage of 11kv line to line, 50Hz with different disturbances at source end, non-linear and unbalanced load at load end is considered. Non-linear load (whether Diode Rectifier feeding an RL load or thyristor feeding an RL load) injects current harmonics into the system. IUPQC is able to reduce the harmonics from entering into the system using shunt control.

Case 1: Impulsive

A. Iupqc-Mitigating The Effect Of Impulsive Sag

A 3-phase supply voltage (11kv, 50Hz) with impulsive sag of 0.3 pu magnitude and the duration about 0.5 to 30 cycles is taken. With the system operating in the steady state, a 30 cycle impulsive voltage sag of 0.3 pu magnitude is occurring at 0.2 msec for which the peak of the supply voltage reduces from its nominal value of 11kv to 8kv.

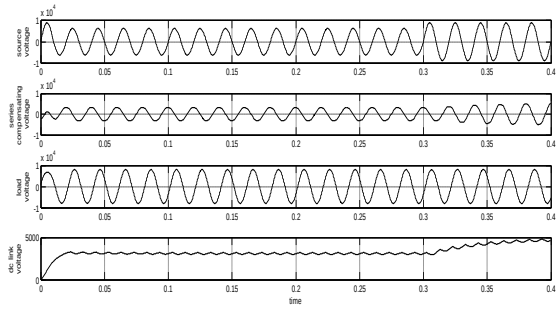

Fig. 1: Simulation results – mitigating the effect of impulsive sag of 0.3 pu with duration 0.5 to 30 cycles using series voltage controller.
(a) Supply voltage in phase-A (b) Series injected voltage in phase-A
(c) Load voltage in phase –A (d) The DC capacitor voltage

The Total Harmonic Distortion (THD) at load side is found to be 1.02%. The source voltage THD is effectively found to be 0.045%.

Compensating Load Current Harmonics Using Direct Current Control Technique

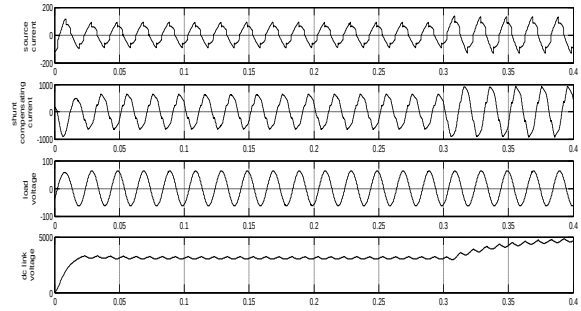

Fig. 2: Simulation results-mitigating the effect of impulsive sag of 0.3 pu with duration 0.5 to 30 cycles using direct current control technique with PI controller
(a) Load current in phase –A (b)shunt compensating current in phase –A
(c)Supply current in phase-A (d) DC capacitor voltage

The Total Harmonic Distortion (THD) at load side is found to be 0.294%. The source current THD was effectively found to be 14.30%.

B. Iupqc-Mitigating The Effect Of Impulsive Swell

A 3-phase supply voltage (11kv, 50Hz) with impulsive swell of 0.3 pu magnitude and the duration about 0.5 to 30 cycles is taken. With the system operating in the steady state, a 0.5 to 30 cycle impulsive voltage swell of 0.3 pu magnitude is occurring at 0.2 msec for which the peak of the supply voltage raises from its nominal value of 11kv to 14kv.

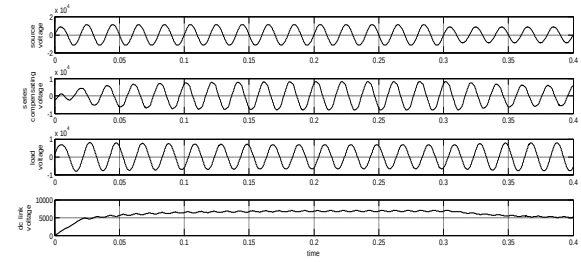

Fig. 3: Simulation results – mitigating the effect of impulsive swell of 0.3 pu with duration 0.5 to 30 cycles using series voltage controller.
(a) Supply voltage in phase-A (b) Series injected voltage in phase-A

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(c) Load voltage in phase –A (d) The DC capacitor voltage

The Total Harmonic Distortion (THD) at load side is found to be 1.71%. The source voltage THD is effectively found to be 0.045%.

Compensating Load Current Harmonics Using Direct Current Control Technique

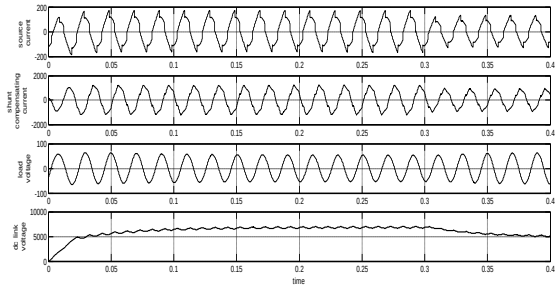

Fig. 4: Simulation results- mitigating the effect of impulsive swell of 0.3 pu with duration 0.5 to 30 cycles using direct current control technique with PI controller.
(a) Load current in phase –A (b) shunt compensating current in phase –A
(c)Supply current in phase-A (d) DC capacitor voltage

The Total Harmonic Distortion (THD) at load side is found to be 0.584%. The source current THD was effectively found to be 14.61%.

Case 2: Momentary

A. Iupqc-Mitigating The Effect Of Momentary Sag

A 3-phase supply voltage (11kv, 50Hz) with momentary sag of 0.2 pu magnitude with the duration about 20 to 30 cycles is taken. With the system operating in the steady state, a 20-30 cycle momentary sag of 0.2 pu magnitude is occurring at 8 msec for which the peak of the supply reduces from its nominal value of 11kv to 9kv.

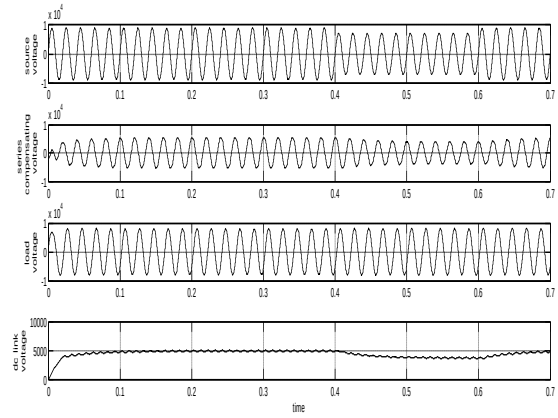

Fig. 5: Simulation results –mitigating the effect of momentary sag of 0.2 pu with duration 20 to 30 cycles using series voltage controller.
(a) Supply voltage in phase-A (b) Series injected voltage in phase-A
(c) Load voltage in phase –A (d) The DC capacitor voltage

Fig. 5(a) shows the series injected voltage, injecting the required compensating voltage. Fig. 5(b) shows the compensated feeder-2 load voltage. As can be seen from the Fig. 5(c) there is perfect compensation for momentary sag. Fig. 5(d) shows the DC link voltage. In order to supply the balanced power required to the load, the DC capacitor voltage drops as soon as the sag occurs. As the sag is removed the capacitor voltage returns to the steady state.

The Total Harmonic Distortion (THD) at load side is found to be 1.65%. The source voltage THD is effectively found to be 0.045%.

Compensating Load Current Harmonics Using Direct Current Control Technique

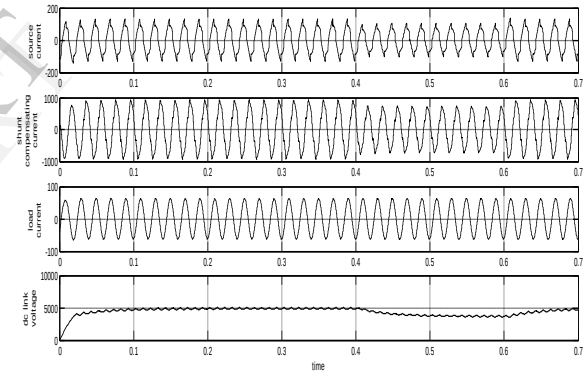

Fig. 6: Simulation results- mitigating the effect of momentary sag of 0.2 pu with duration 20 to 30 cycles using direct current control technique with PI controller.
(a) Load current in phase –A (b) shunt compensating current in phase –A
(c)Supply current in phase-A (d) DC capacitor voltage

The Total Harmonic Distortion (THD) at load side is found to be 0.496%. The source current THD was effectively found to be 14.44%.

B. Iupqc-Mitigating The Effect Of Momentary Swell

A 3-phase supply voltage (11kv, 50Hz) with momentary swell of 0.3 pu magnitude with the duration about 20 to 30 cycles is taken. With the system operating in the steady state, a 20-30 cycle momentary swell of 0.3 pu magnitude is occurring at 8 msec for which the peak of the supply raises from its nominal value of 11kv to 8kv.

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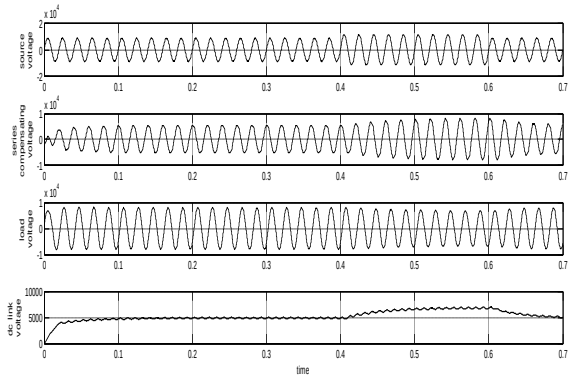

Fig. 7: Simulation results –mitigating the effect of momentary swell of 0.3 pu with duration 20 to 30 cycles using series voltage controller.
(a) Supply voltage in phase-A (b) Series injected voltage in phase-A
(c) Load voltage in phase –A (d) The DC capacitor voltage
Fig. 7(a) shows the series injected voltage, injecting the required compensating voltage. Fig. 7(b) shows the compensated feeder-2 load voltage. As can be seen from the Fig. 7(c) there is perfect compensation for momentary swell. Fig. 7(d) shows the DC link voltage. In order to supply the balanced power required to the load, the DC capacitor voltage raises as soon as the sag occurs. As the swell is removed the capacitor voltage returns to the steady state.

The Total Harmonic Distortion (THD) at load side is found to be 1.71%. The source voltage THD is effectively found to be 0.045%.

Compensating Load Current Harmonics Using Direct Current Control Technique

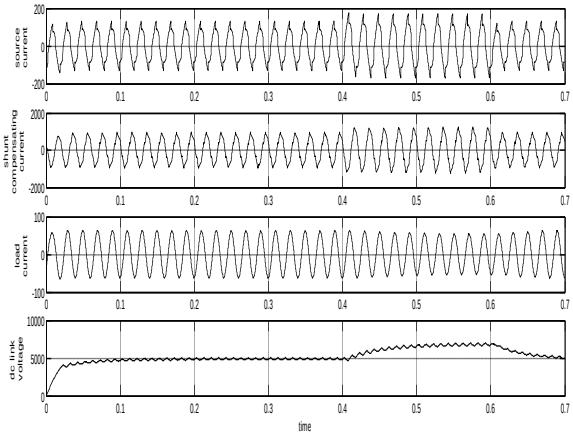

Fig. 8: Simulation results- mitigating the effect of momentary swell of 0.3 pu with duration 20 to 30 cycles using direct current control technique with PI controller.
(a) Load current in phase –A (b) shunt compensating current in phase –A
(c)Supply current in phase-A (d) DC capacitor voltage

The Total Harmonic Distortion (THD) at load side is found to be 0.567%. The source current THD was effectively found to be 14.60%.

CASE 3: TEMPORARY

A. Iupqc-Mitigating The Effect Of Temporary Sag

A 3-phase supply voltage (11kv, 50Hz) with temporary sag of 0.07 pu magnitude with the duration about 30 to 40 cycles is taken. With the system operating in the steady state, a 30-40 cycle momentary sag of 0.07 pu magnitude is occurring at 12 msec for which the peak of thesupply reduces from its nominal value of 11kv to 9kv.

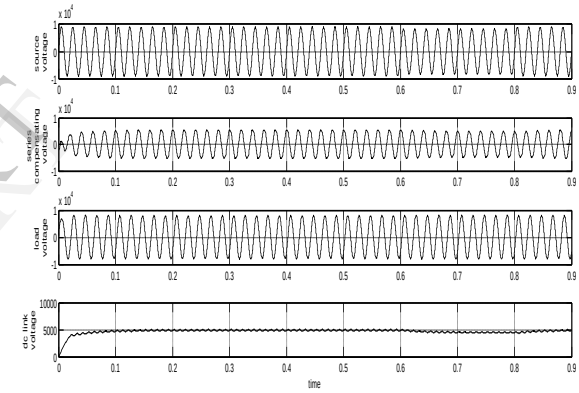

Fig. 9: Simulation results – mitigating the effect of temporary sag of 0.07 pu with duration 30 to 40 cycles using series voltage controller.
(a) Supply voltage in phase-A (b) Series injected voltage in phase-A
(c) Load voltage in phase –A (d) The DC capacitor voltage
Fig. 9(a) shows the series injected voltage, injecting the required compensating voltage. Fig. 9(b) shows the compensated feeder-2 load voltage. As can be seen from the Fig. 9(c) there is perfect compensation for temporary sag. Fig. 9(d) shows the DC link voltage. In order to supply the balanced power required to the load, the DC capacitor voltage drops as soon as the sag occurs. As the sag is removed the capacitor voltage returns to the steady state.

The Total Harmonic Distortion (THD) at load side is found to be 1.63%. The source voltage THD is effectively found to be 0.045%.

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Compensating Load Current Harmonics Using Direct Current Control Technique

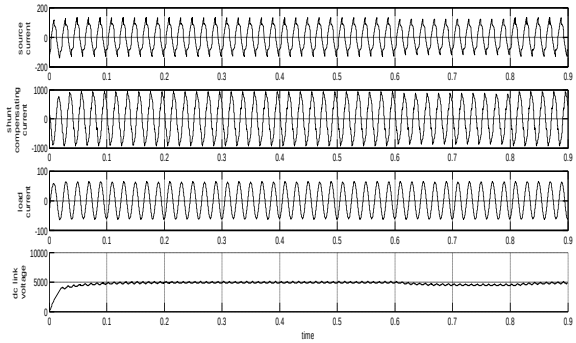

Fig. 10: Simulation results- mitigating the effect of temporary sag of 0.07 pu with duration 30 to 40 cycles using direct current control technique with PI controller.
(a) Load current in phase –A (b) shunt compensating current in phase –A
(c)Supply current in phase-A (d) DC capacitor voltage

The Total Harmonic Distortion (THD) at load side is found to be 0.479%. The source current THD was effectively found to be 14.49%.

B. Iupqc-Mitigating The Effect Of Temporary Swell

A 3-phase supply voltage (11kv, 50Hz) with temporary swell of .15 pu magnitude with the duration about 30 to 40 cycles is taken. With the system operating in the steady state, a 30-40 cycle temporary swell of 0.15 pu magnitude is occurring at 12 msec for which the peak of the supply reduces from its nominal value of 11kv to 12.5kv.

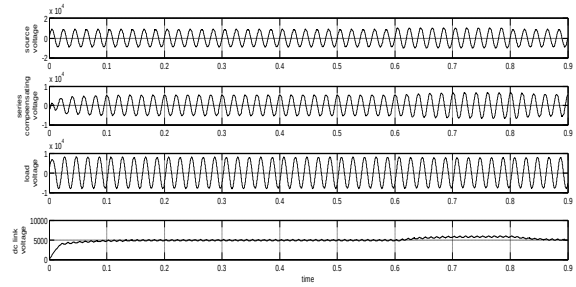

Fig. 11: Simulation results – with mitigating the effect of temporary swell of 0.15 pu with duration 30 to 40 cycles using series voltage controller.
(a) Supply voltage in phase-A (b) Series injected voltage in phase-A
(c) Load voltage in phase –A (d) The DC capacitor voltage

The Total Harmonic Distortion (THD) at load side is found to be 1.65%. The source voltage THD is effectively found to be 0.045%.

Compensating Load Current Harmonics Using Direct Current Control Technique

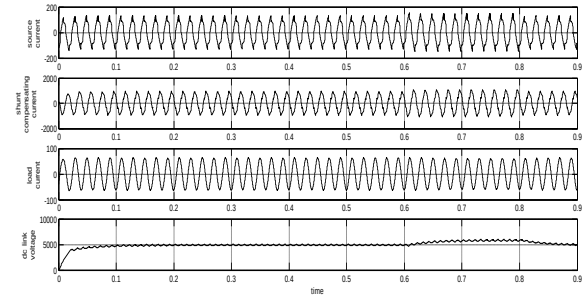

Fig. 12: Simulation results- with mitigating the effect of temporary swell of 0.15 pu with duration 30 to 40 cycles using direct current control technique with PI controller.
(a) Load current in phase –A (b) shunt compensating current in phase –A
(c)Supply current in phase-A (d) DC capacitor voltage

The Total Harmonic Distortion (THD) at load side is found to be 0.502%. The source current THD was effectively found to be 14.56%.

Table 4: Comparison of the THD Content after Compensation in Three Different Cases of Interruptions Used For IUPQC

S .no	Cases	Type of interruption	TOTAL HARMONIC DISTORTION (THD) In %			
			VS	IS	VL	IL
1	Case:1 Impulsive	a. sag, 0.5-30 cycles 0.1-0.9 p.u	0.045	14.30	1.02	0.29
		b. swell, 0.5-30 cycles 1-1.8 p.u	0.045	14.61	1.71	0.58
2	Case:2 Momentary	a. sag, 20-30 cycles 0.1-0.9 p.u	0.045	14.44	1.65	0.49
		b. swell,20-30 cycles 1.1-1.4 p.u	0.045	14.60	1.70	0.56
3	Case:3 Temporary	a.sag 30-40 cycles <0.1 p.u	0.045	14.49	1.63	0.47
		b. swell,30-40 cycles 1.1-1.2 p.u	0.045	14.56	1.65	0.50

VII. Conclusions

The closed loop control schemes of Direct current control, series voltage converter for the proposed IUPQC have been described. A suitable mathematical model of the IUPQC has been developed with shunt (PI) controller and series voltage controller the simulated results have been described.

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The simulated results shows that PI controller of the shunt filter (current control mode), series filter (voltage control mode) compensates of all types of interruptions in the load current and source voltage, so as to maintain sinusoidal voltage and current at load side. The series filter was tested with different types of interruptions. The simulated results show that in all the stages of circuit operation, the feeder-2 load voltages and load currents are restored close to ideal supply.

For all the types of disturbances (interruptions) the Total Harmonic Distortion (THD) after compensation is to be less than 5% which is as per IEEE standards.By observing below factors we conclude that performance of IUPQC for different interruptions

1. The THD content will not change for small term interruptions like impulsive nano, impulsive micro, impulsive milli, momentary interruption, temporary interruption etc.
2. The THD content with sag and swell is slightly changing from 3 to 5% only.

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