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Design and Development of OFDM Baseband Transceiver using VIRTEX-6 FPGA Family

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***Abstract* - Broadband Wireless Access (BWA) is a successful technology which offers high speed voice, internet connection and video. One of the leading candidates for Broadband Wireless Access is Wi-MAX; it is a technology that compiles with the IEEE 802.16 family of standards. This paper mainly focused towards the hardware Implementation of Wireless MAN-OFDM Physical Layer of IEEE Std 802.16d Baseband Transceiver on FPGA. The RTL coding of VHDL was used, which provides a high level design-flow for developing and validating the communication system protocols and it provides flexibility of changes in future in order to meet real world performance evaluation. The proposed design is very much supportive to adaptive modulation schemes which was described in IEEE Std. 802.16d and equipped with the soft interfaces for MAC layer and also RF-front end so that in future more work will be done in order to deploy complete Wi-MAX CPE IP core.**

Key Words: Wi-MAX, PHY Layer, IEEE Std 802.16d ,Orthogonal Frequency Division Multiplexing (OFDM), Field Programmable Gate Array (FPGA), Hardware Description Language (HDL), Fast Fourier Transform (FFT),Inverse Fast Fourier Transform (IFFT), Cyclic Prefix (CP).

I.INTRODUCTION

In the United States, the Federal Communication Commission has set aside 15 frequency bands for use in commercial fixed wireless service, at frequencies of 2 GHz to 40GHz. In other countries, similar frequency bands have been allocated. These frequencies are considerably higher than those used for cellular systems. At these frequencies, often referred to as millimeter wave frequencies, propagation characteristics are quite different from those in the MHz ranges. Then we introduce a technique that is used in a number of WLL systems, known as orthogonal FDM (OFDM).The telecommunications industry faces problem to provide telephone services to the rural areas like where the customer base is very small at these areas to install a wired phone network cost is very high. We have to reduce this problem and one method of reducing the cost of high infrastructure of a wired system is by using fixed wireless radio network. For rural and urban areas, large cell sizes are required to obtain sufficient coverage in but it leads problems Like large signal path loss and long delay times in multipath signal propagation. OFDM/COFDM also called multicarrier modulation, uses multiple carrier signals at different frequencies. It sends some of the bits on each channel. This is similar to FDM. However in case of OFDM, all of the sub channels are dedicate to a single data source. OFDM allows many users to transmit in an allocated band spectrum by dividing available bandwidth into many narrow bandwidth carriers. The transmission is occurs in such a way that the carriers used are orthogonal to each other to allows them to be packed together much closer than standard frequency division multiplexing this leads to OFDM/COFDM providing a high spectral efficiency. OFDM was recognized as an outstanding method for high-speed cellular data communication where its implementation relies on very high-speed digital signal processing.

In this paper the design and development of OFDM system will be illustrated as well as a detailed simulation of the OFDM system with 64-QAM to study the effect of various design parameters on the system performance. OFDM transceiver will be implemented by using FPGA Vertex6 (ML605 KIT-Xilinx). All modules are designed by using VHDL programming language.

OFDM Description

An OFDM symbol is made up from carriers; the amount of carriers determines the FFT size used.

There are several carrier types listed below:

- Data carriers – It is for data transmission
- Pilot carriers – It is for different estimation purposes
- Null carriers – Means no transmission at all, for guard bands and DC carrier.

All these OFDM carriers Frequency descriptions are shown in fig.1. In OFDM mode each OFDM symbol is generated by a single station and they convey a single logical stream. Then the data is transmitted by different stations serially in time. This mode is used with Fast Fourier Transform, sizes from 64 up to 512.

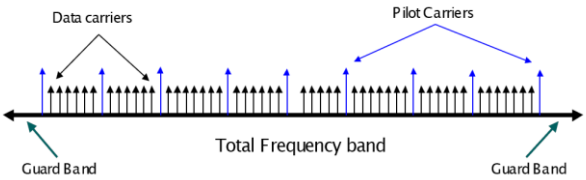


Fig. 1 OFDM Frequency descriptions

II. OFDM OVERVIEW

2.1. Orthogonality

The frequencies of the subcarriers are selected so that at each carrier frequency, all other subcarriers do not contribute any interference to the overall waveform. Maintaining orthogonality of the carriers is the key to OFDM. The integral of the product of two signals is zero over a time period then they are said to be orthogonal to each other. Two sinusoids with frequencies that are integer multiples of a common frequency can satisfy this criterion. Therefore, orthogonality is defined by:

$$\int_0^T \cos(2\pi nft)\cos(2\pi mft)\,dt = 0 \qquad n \neq m \quad (1)$$

Where n and m are two unequal integers; f is the fundamental frequency; T is the period over which the integration is taken. For OFDM, T is one symbol period and f set to $1 \div T$ for optimal effectiveness. Fig.2. below Shows the nature of orthogonality of the OFDM and it gives the orthogonal subcarriers-spectral view. By observing the figure.1.a. we can identify there is no interference between the carriers. The sub carriers are made orthogonal to each other so that each one has the integer number of cycles over a symbol period. So the spectrum of each sub carrier has a null at the centre frequency of each other sub carrier resulting in no interference between the sub carriers, allowing them to be closely spaced as theoretically possible as shown in the next slide.It means that each carrier is positioned such that it occurs at the zero energy frequency point of all other carriers.

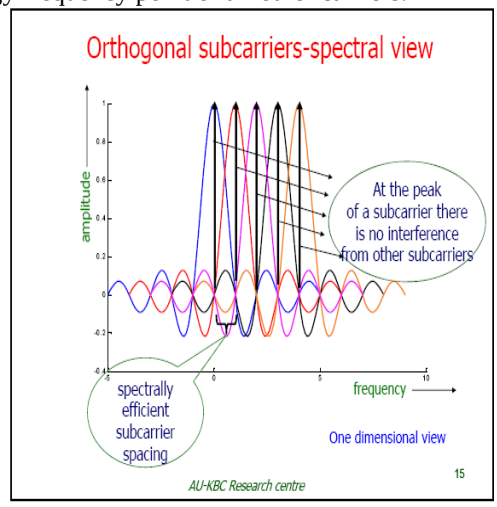


Fig.2 Illustration of Orthogonality of OFDM

OFDM is an attractive modulation technique is used in Broadband wireless systems that decreases large delay spread. OFDM avoids temporal equalization using a cyclic prefix technique with a small penalty in channel capacity. Where Line-of-Sight (LOS) cannot be achieved, there is likely to be significant multipath dispersion, which limits the maximum data rate. The technologies like OFDM are best placed to overcome these and allowing nearly arbitrary data rates on dispersive channels. [11]. each subcarrier is modulated independently as shown in Fig. 1. The subcarrier signals are mutually orthogonal as shown in Fig.3. [11].

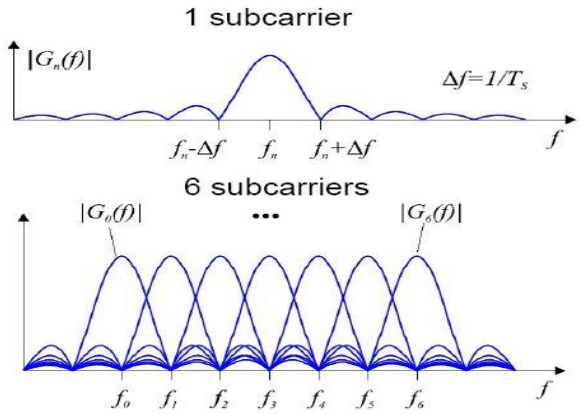


Fig. 3 OFDM Subcarriers in Frequency Domain

2.2 OFDM Advantages

(i) It uses the spectrum Efficiently
(ii) It is very much resistant to the frequency selective fading
(iii) Eliminates the ICI (Inter-Carrier Interference) and ISI (Inter-Symbol Interference)
(iv) It can recover lost symbols due to the frequency selectivity of channels.
(v) Channel equalization and computationally efficient.

2.3 OFDM Disadvantages

(i) High synchronism accuracy.
(ii) Multipath propagation must be avoided
(iii) It has large peak-to-mean power ratio due to the superposition of all subcarrier signals, this can become a distortion problem (Crest Factor).

III Why FPGAs

A Field Programmable Gate Array (FPGA) is kind of like a CPLD turned inside out. FPGA is a semiconductor device contains programmable logic components called 'logic blocks' and programmable interconnections. These Logic blocks are arranged in a 2D array and the interconnection wires are organized as horizontal and vertical routing channels between columns and rows of logic blocks. The routing channels contain programmable Switches and wires that allow the logic blocks to be interconnected in many ways. Logic circuits of more than a few hundred thousand equivalent gates in size can be implemented by using FPGA. A hierarchy of programmable interconnects allows logic blocks to be interconnected as needed by the system designer. Logic blocks and interconnections can be programmed by the customer or designer after the FPGA is

manufactured to implement any logical function. Hence the name is "Field-programmable".

Related work

4. OFDM TRANSCEIVER

The basic components of OFDM Transceiver will be discussed in the next few subsections.

4.1. OFDM Transmitter

The block diagram of OFDM transmitter is shown in Fig.4 [9].

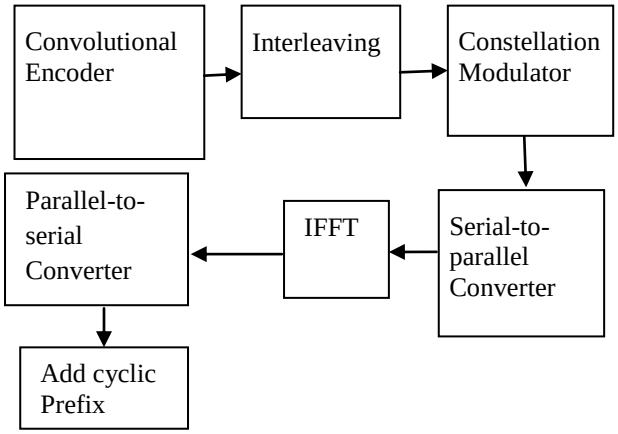


Fig. 4 Block Diagram of OFDM Transmitter

The Randomizer is used for generating random bit. The first three blocks in the transmitter section are used for data coding and interleaving. Then the coded bits are to be mapped by the constellation modulator by using Gray codification, in this way an + jbn values are obtained in the constellation modulator. The serial to parallel converter is used convert the data bits from the serial form to the parallel form. The output from the serial to parallel converter is then applied to Inverse Fast Fourier Transform (IFFT) transforms, it transforms the signals from the frequency domain to the time domain; IFFT converts a large number of complex data points of length that is power of 2, into the same number of points but in the time domain. The number of sub-bands in the available spectrum is split into [11, 12] is determined by the number of subcarriers. The Cyclic Prefix (CP) is a replica of the last N samples from the Inverse Fast Fourier Transform, which are placed at the beginning of the OFDM frame. It overcomes ISI problem. It is important to choose the minimum necessary CP to maximize the efficiency of the system [16].

4.2 OFDM Receiver

The block diagram of OFDM receiver is observed in Fig.5.

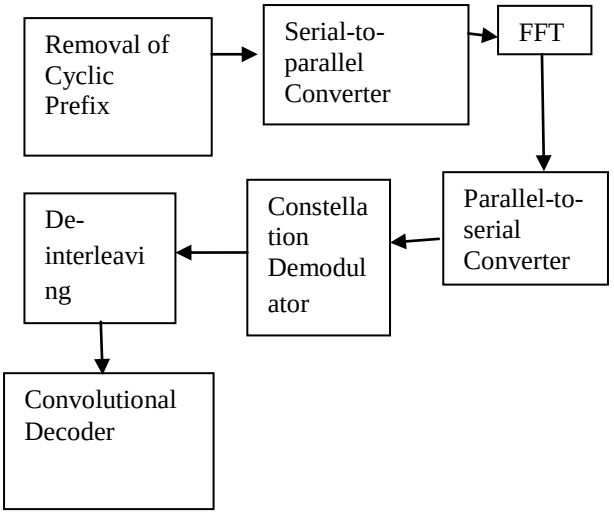


Fig. 5 Block Diagram of OFDM Receiver

The received signal is applied to the cyclic prefix removal block then the output from cyclic prefix removal block is fed to a serial-to-parallel converter [11]. After that, the signals are passed through an N-point fast Fourier transform. N-point fast Fourier transform converts the signal to frequency domain. The output of the FFT is formed by first M- samples of the output. The demodulation can be made by Discrete Fourier Transform, or better, by Fast Fourier transform that is it is very efficient implementation that can be used to reducing the time of processing and the used hardware [14]. FFT calculates DFT with a great reduction in the amount of operations, leaving several existent redundancies in the direct calculation of DFT [13-15].

The detailed discussion about each block of OFDM transceiver is given below

A. Convolution Encoder/Decoder

This coder adds redundant bits. In this type of coding technique each m bit symbol is transformed into an n bit symbol; this m/n is known as code rate. The transformation of m bit symbol into n bit symbol depends upon the last k data a symbol, therefore k is known as the constraint length of the Convolution code.Viterbi algorithm is used to decode convolutionaly encoded bits at the receiver section. Viterbi decoding algorithm is one of the most suitable for Convolution codes with k_10.

B. Interleaver/De-Interleaver

Interleaving is done to protect the data from burst errors during transmission. The in-coming bit stream is re-arranged such that adjacent bits are no more adjacent to one another. The data is broken into blocks and then the bits within a block are rearranged. The bits within an OFDM symbol are rearranged so that adjacent bits are placed on

non-adjacent sub-carriers. At the receiver section De-Interleaving again rearranges the bits into original form at reception.

C. Constellation Modulator/Demodulator

The Constellation Modulator at transmitter section modulates the incoming i.e. interleaved bits onto different sub-carriers. For different sub-carriers different modulation techniques can be employed such as, BPSK, QAM, QPSK etc.. The De-Modulator at receiver section simply extracts bits from the modulated symbols.

D. Serial-to-parallel Converter and Parallel to Serial converter

Serial to Parallel Conversion

This block is used in OFDM Transmitter; it converts serial input to parallel output. The output from this block is given to the input to IFFT. The input serial data stream is formatted into the word size required for transmission, e.g. word/ 2 bits for QPSK, and then shifted into a parallel format. Then the data is transmitted in parallel by assigning each data word to one carrier in the transmission.

Parallel to Serial conversion

This block is used in OFDM Receiver; it converts parallel input to serial output and then the output from this block is given to the Symbol de-mapper.

E. Inverse Fast Fourier Transform/ Fast Fourier Transform

This is the one of most important block in the OFDM system. IFFT basically gives OFDM orthogonality. The IFFT transform a spectrum (amplitude and phase response of each component) into a time domain signal. It converts complex data points into the same number of points in time domain. Similarly, FFT at the receiver side converts from time domain back to frequency domain i.e. it performs the reverse task.

F. Addition/Removal of Cyclic Prefix

The cyclic extension is used to overcome the inter symbol interference and inter carrier interference (ICI) issues while passing signal through a time-dispersive channel. A cyclic prefix is a copy of the last part of the OFDM symbol that is prepended to the transmitted symbol and removed at the receiver before the demodulation as shown in fig.6. The cyclic prefix11 should be at least as long as the significant part of the impulse response experienced by the transmitted signal. It avoids ISI because it acts as a guard space between successive symbols and it converts the linear convolution with the channel impulse response into a cyclic convolution. A cyclic convolution is the time domain translates into a scalar multiplication in frequency domain, the subcarriers remain orthogonal and there is no ICI. [7].

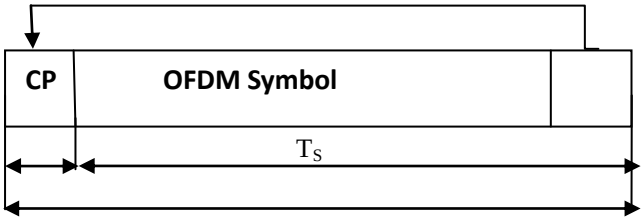


Fig.6 Cyclic prefix in OFDM principle

V. IMPLEMENTATION AND SIMULATION RESULTS

5.1 MATLAB Implementation of OFDM Transceiver

Figure.7. shows the configuration for a basic OFDM transmitter and receiver. The signal generated is at base-band and so to generate an RF signal the signal must be filtered and mixed to the desired transmission frequency.

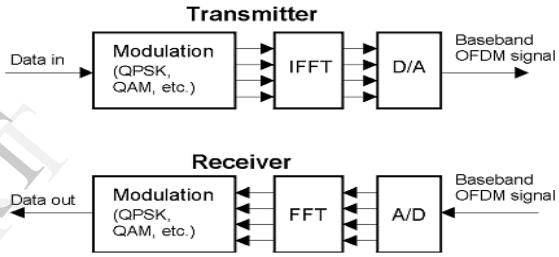


Figure.7 Basic FFT, OFDM transmitter and receiver

5.1.1 MATLAB implementation and verification

Section A: QAM

The following are the graphs from MATLAB showing the MATLAB implementation of OFDM transceiver module

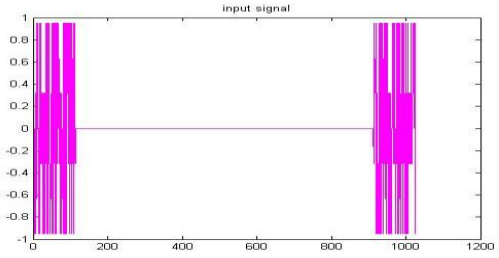


Fig .8.1 Graph of input signal to IFFT Block

The above graph shows the input signal which is to be modulated. It has 8 levels in total. This graph is a plot of the signal whose inputs are mapped using a random binary sequence. We can observe that there are 113 signals at the start and at the end with around 800 zeroes in between. This is done to get a uniform 1024 symbol iffy and taking FFT to which gives 26 samples from which the input signal can be re extracted.

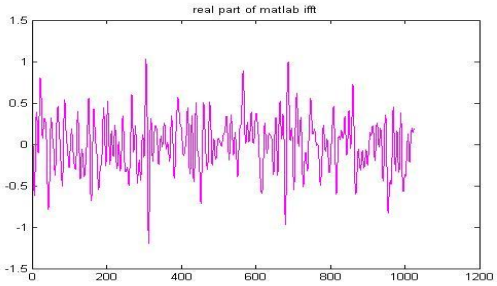


Fig .8.2 Graph of real part of MATLAB IFFT

The above graph shows the result of IFFT upon the input signal. The previous figure depicting the input is passed through an IFFFT block to get this signal. Since we are taking a 1024 point IFFT we get a signal with all 1024 samples in it. This graph shows only the real part of the result of the IFFT.

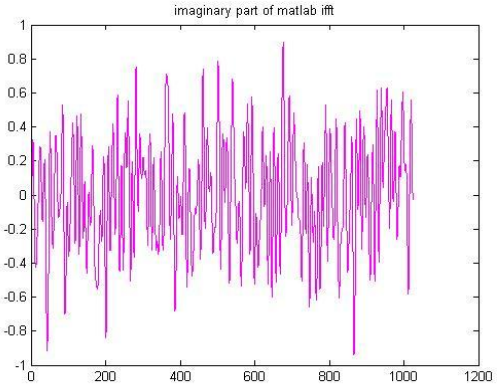


Fig.8.3 Graph of imaginary part of MATLAB IFFT

The above graph shows the imaginary part of the IFFT of the input signal. It also has 1024 points spread along the signal.

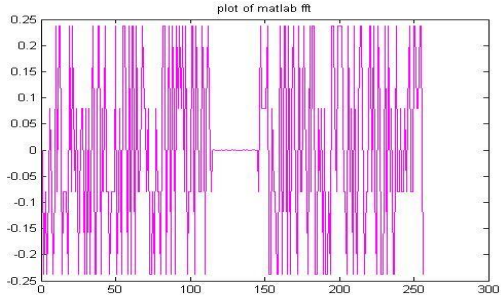
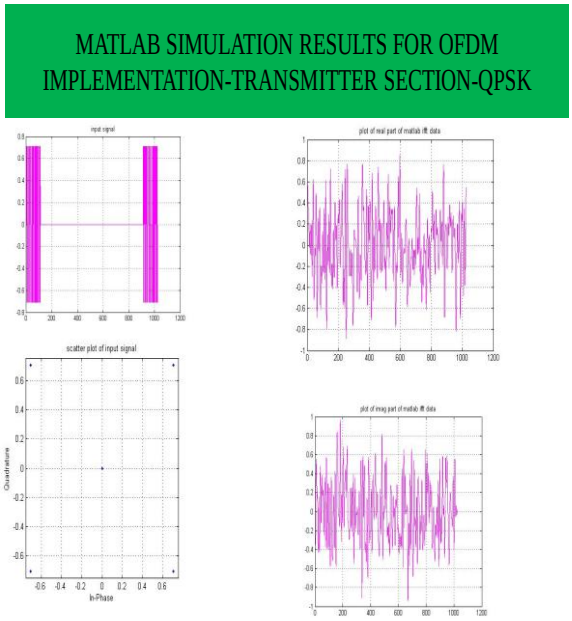


Fig.8.4 Graph of plot of MATLAB FFT

The above graph shows the signal recovered by taking FFT over the IFFT signal. This gets back the original signal without the nulls in between. Ideally all the amplitudes of this signal should equal those amplitudes of the input signal. We compare this signal with input signal to get the bit error rate.

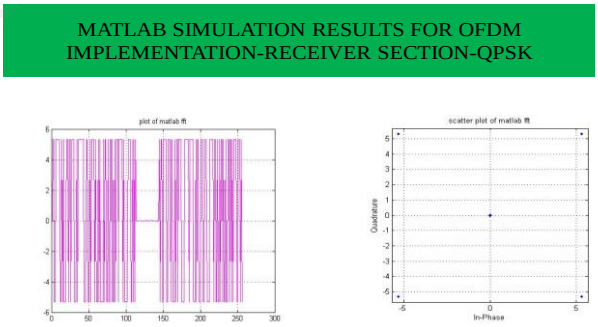
Section-B:-QPSK

With same consideration the OFDM chain is implemented in MATLAB for QPSK the following are the figures



Input Signals and I & Q representation of IFFT

Fig.8.5 Implementation-Transmitter Section-QPSK



Output signal from FFT Block and Scatter plot of out signal

Fig.8.6 Implementation-Receiver Section-QPSK

The above figures show the graphs of the input signal for QPSK, its IFFT plots and the FFT result after taking FFT over the IFFFT signal. These plots are same as those for the QAM with all the steps being the same except that there are only four levels in QPSK where there used to be eight in case of QAM.

5.2 VHDL implementation

Fig.9 shows Block Diagram of the process flow of implementation and verification of IFFT/FFT

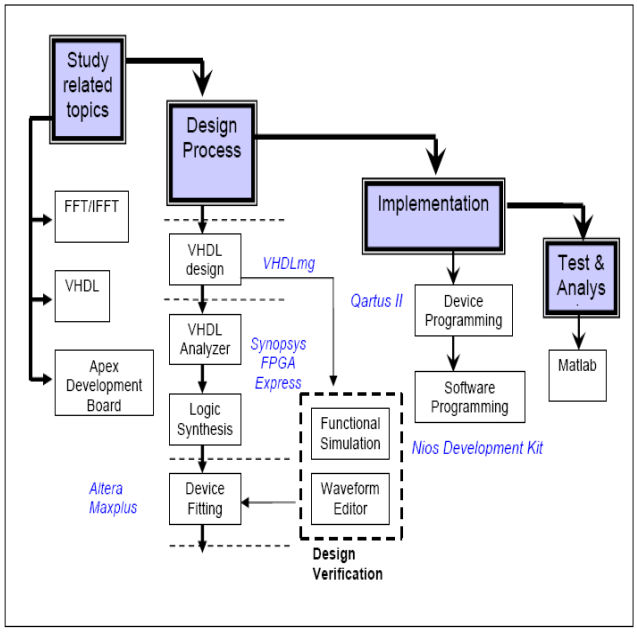


Fig.9 Block Diagram of the process flow of implementation and verification of IFFT/FFT

The proposed method uses Virtex-6 FPGA family to implement OFDM. Virtex has families have built-in PowerPC's which hard-core also micro blaze is can be programmed in Virtex FPGA's. The Virtex-6 FPGA families are the high-performance silicon foundation for Targeted Design Platforms. Consuming 50% lower power and delivering 20% lower cost than the previous generation, the new family is built with the integrated blocks for DSP ,programmability, connectivity support - including high-speed transceiver capabilities - to satisfy the insatiable demand for higher bandwidth, memory and higher performance.Virtex-6 FPGA Family Benefits Meet our performance targets easily Stay within our power budget without sacrificing performance, power, cost and Optimize I/O bandwidth with easy-to-use high-speed connectivity technologies. So our proposed method uses Virtex-6 FPGA family to design and develop OFDM. In this part the OFDM elements are developed and implanted for XILINXs Vertex6 (ML605 KIT) FPGA hardware board. All modules are designed using VHDL programming language and implement using Xilinx ISE software and tested with Xilinx Spartan 6 kit.

5.3 The following are simulation tools used for the synthesis

Software requirement

a. MATLAB Simulation for OFDM.
b. Xilinx ISE VHDL coding and synthesis.
c. Model Sim/Xilinx Isim for Simulation.
d. MATLAB for stimulus generation and verification.

Hardware requirement

a. Hardware for the verification and validation.
b. Xilinx VERTEX-6 kits from Xilinx

I. Simulation in Xilinx ISE Simulator:

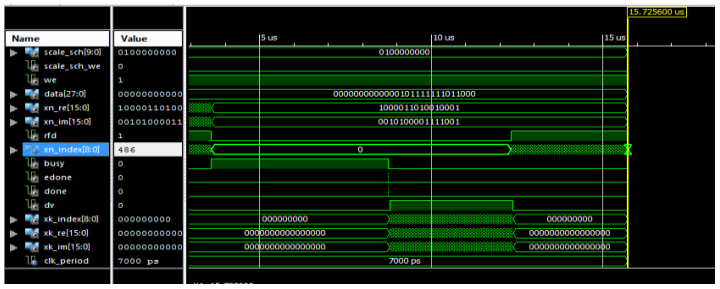


Fig.9.1 Scereen Showing the simulation FFT/IFFT Core where one cycle is completed.

In this section, the Xilinx IDE the simulation of entire code is done with help of test bench program in which reading the input data from file location and writing the output data in to a file in the project directory location as shown in fig.9.1.

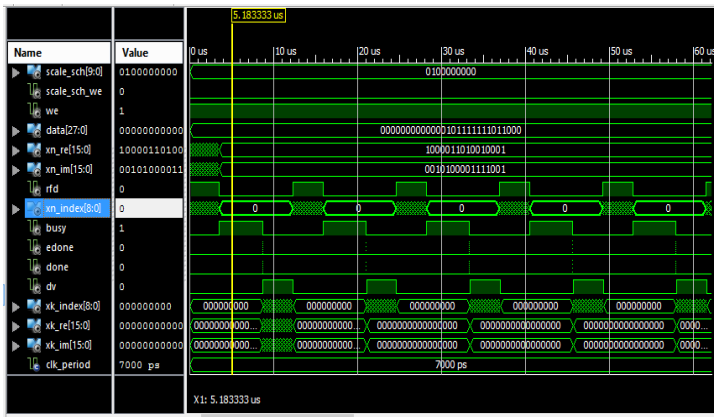


Fig .9.2 Scereen showing the multiple cycles completed

In this simulation section,the FPGA implementation of IFFT/FFT multiple cycles completed in Xilinxs hardware board as shown in fig.9.2 which we can see the output signal and busy signal.

5.3.1 Result Verification And Validation

In this section once again the matlab is used to
1.Genarate the input signal for givng the data.
2.Verification of FFT output.

5.3.2 Genarate the input signal for givng the data

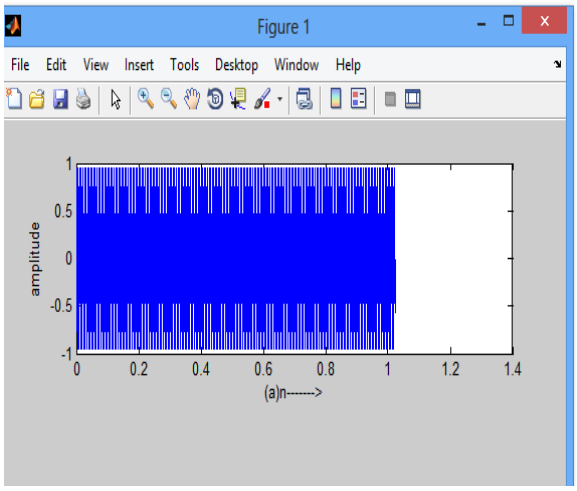


Fig.9.3 screen showing the input signal BPSK generation in matlab

The above figure which is out put file of matlab file shows the input signal genearion for 1024 point of bpsk signal in ifft verification.

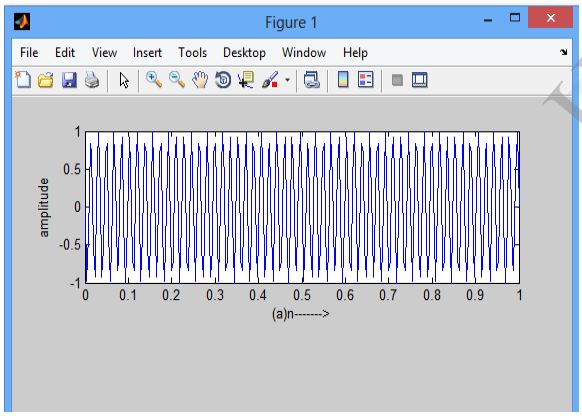


Fig.9.4 Screen showing the 256 point I/P signal generation

The above figure which is output plot from the MATLAB file used to generate the input data for IFFT block. This is generated for 256 point FFT verification.

5.3.3 Verification of FFT output

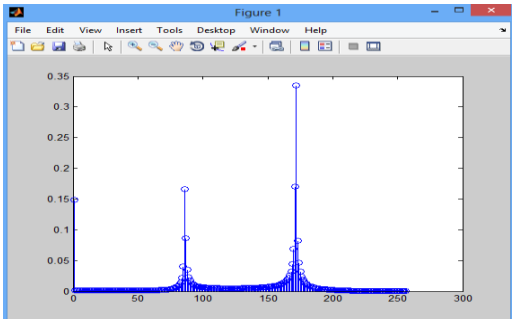


Fig.9.5 Screen showing the FFT output giving the clean spectrum in the MATLAB

The above figure is the MATLAB plot which is the output plot for verification file in MATLAB. This is used to verify the IFFT/FFT output gives the correct spectrum for the selected points and frequency.

II. HARDWARE FOR THE VERIFICATION AND VALIDATION

i. Xilinx Vertex6 (ML605 KIT-Xilinx)

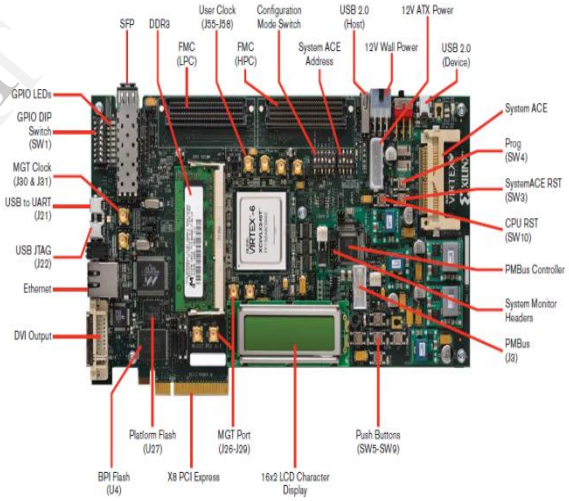


Fig.10 Photo Graph of Xilinx ML605 vertex -6 FPGA – kit

Fig.10 shows the Photo Graph of Xilinx ML605 vertex -6

FPGA – kit and Fig.11 shows its Testing with vertex 6 (ML605 kit) 1024-points IFFT/FFT with SNR=60 dB

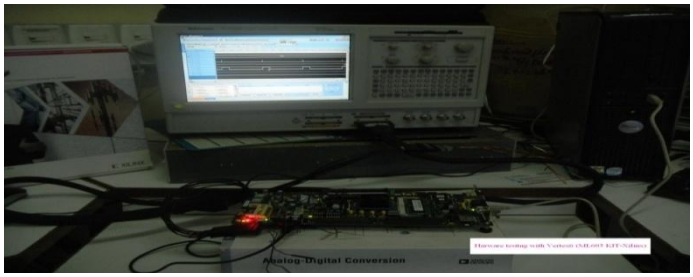


Fig.11 Testing with vertex 6 (ML605 kit) 1024-points IFFT/FFT with SNR=60 dB

VI. CONCLUSIONS

The complete design, validation and implementation of an OFDM transceiver compliant with DVB-T standard were successfully implemented on FPGA board. This work was performed using VHDL Hardware Descriptive Language and IFFT/FFT modules were implemented using Xilinx Virtex 6 FPGA kit. The result showed that the OFDM transceiver can be implemented and simulation at transmitter and receiver section we used in two categories of QPSK and QAM standards or processes. The modulated signal is generated in a computer (MATALB is used to generate the stimulus) passed to the hardware through the computer through USB port. Process of base band processing of transmitter takes place in the hardware board. After processing, the results are implementation and verified in MATLAB. As mentioned in the objectives, a base band OFDM transmitter was successfully developed using Xilinx virtex-6 FPGA MLC605 development board. The output from each module was tested using appropriate software to ensure the correctness of the output result.

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