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Design and Development of Zero Voltage Switched Full Bridge 5 kW DC Power Supply

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Abstract: **Design and implementation of a high power, high voltage, constant frequency, full bridge phase shift pulse width modulation converter in which zero voltage switching of all the active switches over the entire load range is maintained by using auxiliary circuit components is presented. The auxiliary circuit components used are, two capacitors that are connected in series across the DC power rail and two inductors that are connected in series with the transformer of the converter. The two capacitors act as a voltage divider providing midpoint voltage source and the two inductors supply additional current reinforcing the primary current during the transition intervals and increasing the energy available to achieve the zero voltage switching (ZVS). A prototype converter based on this topology is developed that delivers 450V at 5 kW output from 560V dc input, with efficiency greater than 94%. Experimental & simulation results for the converter are presented.**

Keywords— Full bridge converter, phase shift pulse width modulation (PSPWM) soft switching, zero voltage switching (ZVS), phase shift (PS), passive auxiliary circuit, ZVS range

I. INTRODUCTION

In medium to high power DC-DC converter applications, full bridge phase shift pulse width modulation (FB-PSPWM) converters are widely used because of its fixed switching frequency ZVS operation, high efficiency, low EMI, relatively small circulating energy, utilization of output parasitic capacitance of the switches and utilization of leakage inductance of the transformer [1-3]. However, conventional FB-PSPWM converter has main drawback of limited range of operation over which the ZVS can be achieved. ZVS of the left leg switches in the conventional FB-PSPWM converter mainly depend on the energy stored in the leakage inductance of the transformer. At light load, energy stored in the leakage inductance of the transformer is not sufficient to charge/discharge the switch capacitances and this leads to loss of ZVS condition. The loss of ZVS at light loads leads to 1) High switching losses 2) Higher EMI due to high di/dt of the snubber discharging circuit. Therefore, it is desirable to maintain ZVS of the switches over the entire range of operation.

Several techniques have been presented in literature to increase the ZVS range of conventional FB-PSPWM. Use of higher inductance in series with the transformer is reported to increase ZVS range but it leads to higher duty cycle loss as well as ringing across the secondary side rectifier diodes [4]. In this design higher turns ratio of transformer is required to get the desired output voltage, this results in higher primary reflected current and higher conduction loss in switches. In second technique a saturable reactor is used in series with the primary winding or with the secondary side diodes [5]. The advantage of the FB-PSPWM DC-DC converter incorporating saturable resonant inductor is that wider range of operation under ZVS is maintained without significant increase in conduction loss of the switches. However, to implement the saturable inductor large size core is required. The third technique reported to increase the ZVS for wider load range is by incorporating a commutating inductor and a clamp diode for the bridge switches [6]. However in this topology there is requirement of snubber to overcome the prevailing commutation loss. The fourth technique to increase the ZVS range in FB-PSPWM DC-DC converter is to use a two winding commutating inductor clamped to the output and overcome the problem in the technique mentioned in [6] by enabling recovery of the excess of energy directly to the load [7]. Nevertheless, this solution implies a larger, heavier and more complicated converter with inherent cost increase.

Another method for wider ZVS range is use of auxiliary LCC circuit with conventional FB-PSPWM DC-DC converter [8, 9, 10]. The auxiliary circuit consists of a voltage divider and an inductor connected between the middle point of voltage capacitor divider and the middle point of the left leg of conventional FB-PSPWM converter. It is observed that the right leg switches leaves ZVS at lighter load compare to the left leg switches. It is desired to get ZVS for both the legs to minimize the turn-on losses including the no load condition. It is indicated that the ZVS for the both legs of FB-PSPWM DC-DC converter, can be achieved if one more inductor is used in addition to LCC circuitry described in [8,9]. This auxiliary circuit is an add-on to the conventional FB-PSPWM converter, which does not alter the power circuit.

This paper reports the design of high power (5 kW), high voltage (450 V) FB-PSPWM converter based on LLCC auxiliary circuitry to extend the ZVS for entire load range for all the switches of full bridge without increase in the duty cycle loss. This topology is desired in applications where the output voltage is required to be adjustable and the load power is variable over a wide range. Most of the published work on

analysis & design of FB-PSPWM converter is confined to low power (up to 3 kW) converters or to low output voltage (up to 380 V) converters. The FB-PSPWM converter reported here is rated for high voltage and high power output (450 V, 5 kW) with widely variable output voltage (1 to 100%). Description of power circuit of the FB-PSPWM converter with auxiliary circuit is presented in Section II. Modes of operation of the converter are described in Section III. Specific design considerations are covered in section IV. Simulation and experimental results are presented in section V, followed by conclusions in section VI.

II. FB-PSPWM CONVERTER WITH AUXILIARY CIRCUIT

Power circuit diagram of the FB-PSPWM converter with LLCC auxiliary circuit is shown in Fig.1. Main FB-PSPWM converter is constituted by four MOSFET M_1-M_4 switches, four anti parallel diodes D_1-D_4, and four snubber capacitors C_1-C_4. The anti-parallel diodes D_1-D_4 across the M_1-M_4 are the intrinsic diodes of the respective switches. Capacitor C_1-C_4 across the MOSFET M_1-M_4 are the internal output parasitic capacitances. The average capacitance value for each of the C_1-C_4 is C and given as [1, 3]

$$C = \frac{4}{3} \text{ Coss} \qquad (1)$$

where C_{OSS} is a depletion-dependant capacity whose value depends upon the impressed drain -source voltage across the respective MOSFET.

Transformer TR has primary to secondary turn ratio of n:1. Total leakage inductance of the transformer referred to primary is L_{lk}. The voltage across the primary winding of transformer is V_{AB} and the voltage across the secondary winding is V_S. D_{r1}- D_{r4} are the diodes on the secondary side forming full bridge rectifier circuit. Inductor L_f and capacitor C_f form the output filter.

In conventional FB-PSPWM converter the energy stored in the leakage inductor is used to charge/discharge the snubber capacitors, and the load range under which ZVS of the switches is maintained strongly depends on the value of the leakage inductance. Due to leakage inductance, there is duty cycle loss ΔD and it is given as [3]

$$\Delta D \cong \frac{4nL_{lk}\, Io}{V_d\, Ts} \qquad (2)$$

where T_s is switching period of converter, V_d is the input DC voltage, I_o is output dc (average) load current.

The auxiliary LLCC circuitry that provides ZVS over the entire load range consists of two inductor L_1 & L_2 and two capacitors C_{d1} & C_{d2}. The two capacitors with equal capacitances are connected in series, across the DC power rail V_d and this forms a voltage divider circuit. Out of the two auxiliary inductors, one inductor L_1 is connected between middle point A of left leg and the middle point M of capacitor divider. The second inductor L_2 is connected between middle point B of right leg and the middle point M of the capacitor divider.

RCD clamp circuit is used to reduce ringing and voltage overshoot across the diode rectifier, arising because of resonance between the stray capacitance (due to winding & diode) and the leakage inductance of the transformer [1].

III. MODES OF OPERATION

Key waveforms of the FB-PSPWM converter with LLCC auxiliary circuit are shown in Fig.2. In these waveforms the voltages V_{g1}-V_{g4} are the gate voltage signals for switches M_1-M_4 respectively and have approximately 50% duty cycle. These signals are generated using standard Phase shift controller UCC3895 [11]. The switches of left leg (M_1 & M_2) and right leg (M_3 & M_4) turn-on and off alternatively with a small dead time between the gate pulses of each leg to allow the capacitor to discharge before the switches are made on. The phase shift between the two legs determine the operating duty cycle of converter. The operation of converter presented in Fig.1 is explained for positive cycle of primary current with five modes. Mode I or power delivery mode, Mode II or powering to freewheeling transition mode, Mode III or freewheeling interval, Mode IV or freewheeling to powering transition interval and Mode V or linear transition mode.

Mode I: Power delivery mode ($t_0 < t \leq t_1$):
During this mode both $M_1$and M_4 are in conduction and D_{r1} & D_{r4} are rectifying. The transformer primary voltage is V_d and the primary current increases with the slope proportional to the total inductance present in the circuit. In this interval power is delivered to load, hence known as power delivery interval. Primary current during this interval is given by

$$i_p(t) = \frac{V_d - nV_0}{Leq}(t - t_0) + I_p(0) \qquad (3)$$

where $I_p(0)$ is the initial value of the primary current and $L_{eq} = L_{lk} + n^2 L_f$
The mode interval ends when the primary current reaches to its peak value I_1.

$$i_p(t_1) = I_1 \qquad (4)$$

During this mode the terminal A of auxiliary inductor L_1 is connected to V_d and voltage across L_1 is $-V_d/2$ and current through L_1 decreases until the MOSFET M_1 turns off. Similarly B terminal of inductor L_2 is connected to ground, hence the voltage across L_2 is $V_d/2$ and current increases and reaches to its peak value I_{L2} at the end of this interval i.e. when M_4 turns-off. The auxiliary circuit acts as independent circuit without influencing the primary current. Currents through auxiliary inductor L_1 & L_2 are given as:

$$i_{L_1}(t) = -\frac{V_d}{2L_1}(t - t_0) + I_{L_1}(0) \qquad (5)$$

$$i_{L_2}(t) = \frac{V_d}{2L_2}(t - t_0) + I_{L_2}(0) \qquad (6)$$

where $I_{L_1}(0), I_{L_2}(0)$ are the initial value of the currents of auxiliary inductor L_1 & L_2 respectively.
Current through the inductor L_2 at the end of this mode is

$$i_{L_2}(t_1) = \frac{V_d}{4L_2}\left(\frac{T_S}{2} - t_{RL}\right) = I_{L_2} \qquad (7)$$

Or

$$I_{L_2} \cong \frac{V_d\, .T_S}{8L_2}; \qquad t_{RL} \ll \frac{T_S}{2} \qquad (8)$$

t_{RL} is known as right leg transition interval or powering to freewheeling transition interval.
The drain current of M_1 is sum of the primary current and auxiliary inductor current I_{L1}. Similarly the drain current of M_4 is the sum of the primary current and auxiliary current I_{L2}.

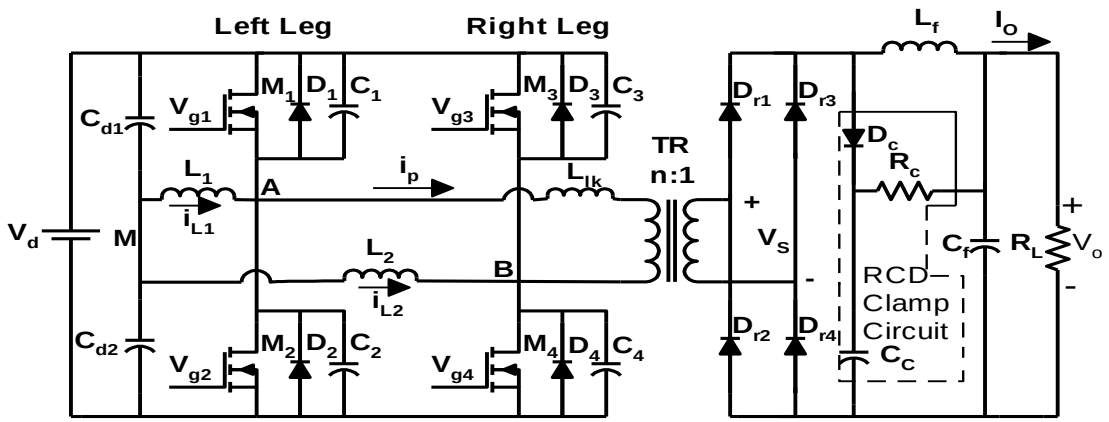

Fig.1 Full bridge phase shift PWM DC-DC converter with auxiliary LLCC circuit

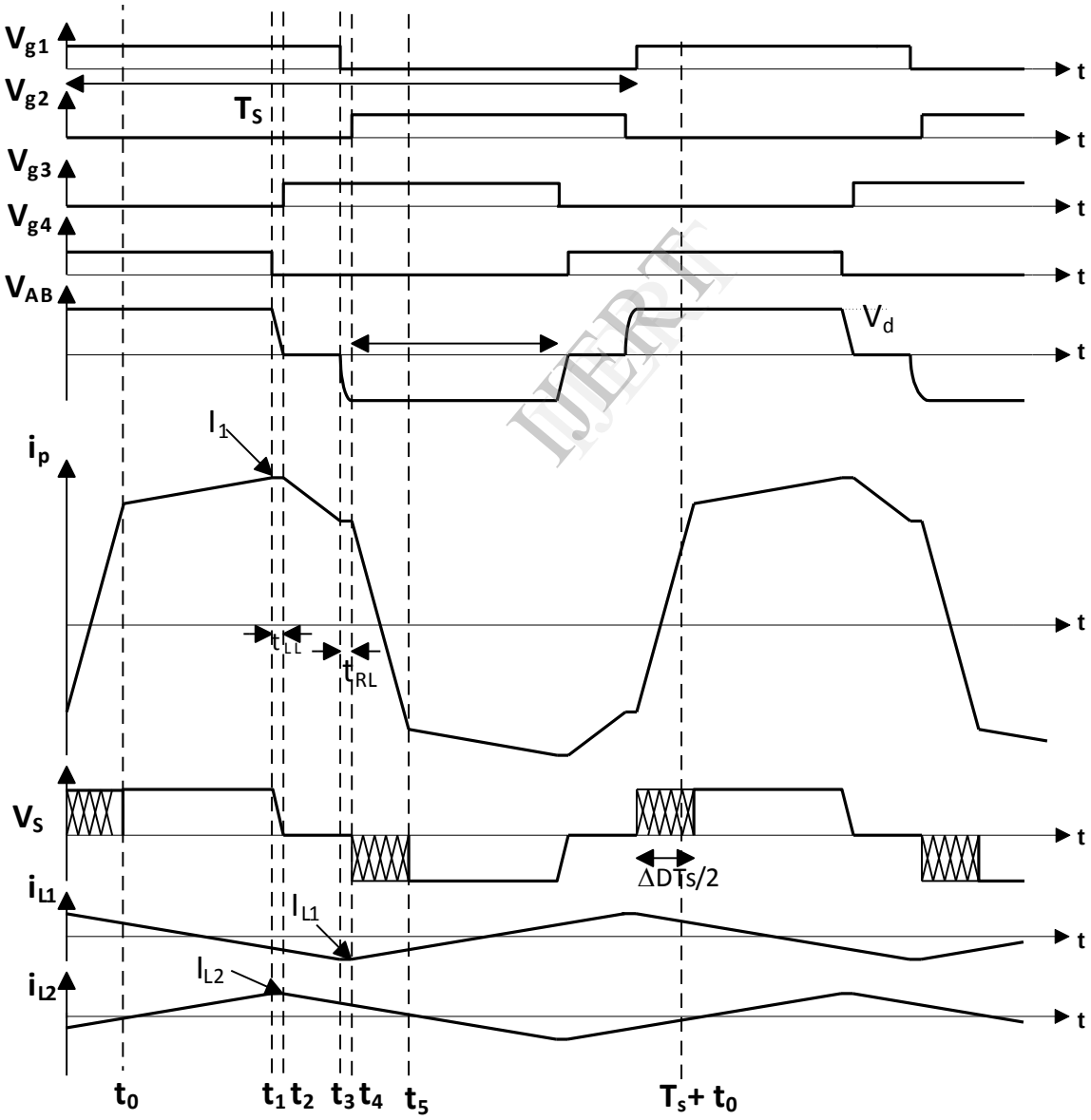

Fig.2 Key waveforms of the Full bridge phase shift PWM DC-DC converter with the auxiliary circuit

Mode II: Powering to freewheeling transition mode ($t_1 < t \leq t_2$):
This mode starts when MOSFET M_4 turns off at time t_1. As M_4 turns off, drain current of M_4 is transferred to C_3 & C_4. Since M_1 is conducting and M_4 is off, transformer continues to see the positive voltage V_d during this interval. Hence D_{r1}& D_{r4} are still conducting as in mode I. The duration of this mode is small, so the primary current and the auxiliary inductor current I_{L2} is almost constant. Hence the charging of C_4 and discharging of C_3 takes place linearly. The time required to complete charge/discharge is given as

$$t_{RL} \geq \frac{V_d \ .(\ C_3 + C_4)}{I_1 + I_{L_2}} \quad or \ \ t_{RL} \geq \frac{2.V_d \ .C}{I_1 + I_{L_2}} \qquad (9)$$

Since M_1 is still on, the current in L_1 is given by eq.(5). This mode ends when the capacitor C_3 voltage reaches to zero and diode D_3 start conducting at $t = t_2$ with ZVS.

Mode III: Freewheeling mode ($t_2 < t \leq t_3$):
This mode starts with zero voltage across capacitor C_3 and diode D_3 initiates its conduction. Primary current freewheels through the MOSFET M_1 & diode D_3. The voltage across the primary of transformer V_{AB} is zero. The rectifier diodes D_{r1}& D_{r4} are still in conduction state. The circuit enters the passive mode i.e. no power is transferred from input to output. This mode ends when gate pulse of M_1 is removed. Primary current during this mode is given by

$$i_p(t) = -\frac{nV_0}{Leq}(t - t_2) + I_p(1) \qquad (10)$$

where $I_p(1)$ is the initial value of the primary current.
As the M_1 is on, current in L_1 is still given by the equation (5). It reaches to its peak value I_{L1} at the end of the interval and given by.

$$i_{L_1}(t_3) = \ \frac{V_d}{4L_1}\left(\frac{T_S}{2} - t_{LL}\right) = \ I_{L_1} \qquad (11)$$

Or

$$I_{L_1} \cong \frac{V_d \ .T_S}{8L_1}; \quad for\ t_{LL} \ll \frac{T_S}{2} \qquad (12)$$

where t_{LL} is known as left leg transition interval or freewheeling to powering transition interval The current in L_2 start decreasing from its peak value and given as

$$i_{L_2}(t) = \ -\frac{V_d}{2L_2}(t - t_3) + \ I_{L_2} \qquad (13)$$

Mode IV: Freewheeling to powering transition mode ($t_3 < t \leq t_4$):
This mode starts at time t_3 when the gate signal of M_1 is removed. At this stage D_3 is still conducting and primary current is same as it was in mode III, and flows through C_1 & C_2. During this mode, contrary to what happened in mode II, all four diodes of rectifier are on. Therefore energy stored in the filter inductor does not contribute to charge/ discharge of C_1/C_2. Because of this reason it is very difficult to obtain ZVS in the conventional converters for light load. However in the converter design presented here, additional energy is stored in inductor L_1 in mode I to III, that helps to achieve ZVS. Thus the total energy (W_L) available to charge/discharge the capacitor C_1/C_2 is the energy stored in leakage inductor of transformer and energy stored in the auxiliary inductor L_1.

$$W_L = \frac{(I_4)^2}{2}(\ L_{lk}\ ) + \frac{(I_{L1})^2}{2}(\ L_1\ ) \qquad (14)$$

where I_4 is the primary current at $t = t_4$ and I_{L1} is the peak current of the auxiliary inductor L_1.

This mode ends when the capacitor C_1 voltage reaches to V_d and capacitor C_2 voltage reaches to zero and diode D_2 starts conducting at time t_4. Current in inductor L_2 during this mode is still given by eq. (13).

Mode V: Linear mode ($t_4 < t \leq t_5$):
At time t_4 diode D_2 initiate its conduction. In this mode primary current changes its polarity. Till the primary current reaches to zero, diode D_2 & D_3 conduct, thereafter M_2 & M_3 start conducting. Primary current in this interval is given as

$$i_p(t) = \ -\frac{V_d}{Leq}(t - t_4) + I_p(2) \qquad (15)$$

where $I_p(2)$ is the initial value of the primary current.

In this mode terminal A of auxiliary indictor L_1 is connected to ground as M_2 is on. The voltage across the L_1 is V_d/2. The current in L_1 starts increasing and given by

$$i_{L_1}(t) = \frac{V_d}{2L_1}(t - t_4) + \ I_{L_1}(1) \qquad (16)$$

where $I_{L_1}(1)$ is the initial value of the primary current.

The time interval of this mode represents the duty cycle loss. In order to reduce the duty cycle loss the slope of primary current should be high i.e. leakage inductance should be minimum. In conventional PSPWM converter, leakage inductance needs to be kept large to store sufficient energy to achieve ZVS of switches for wider range while in the proposed converter, the value of leakage inductance is small and limited by construction of transformer which leads to lower duty cycle loss.

Further for the negative half cycle of primary current these five modes of operations are similarly repeated and the full cycle is completed.

IV. DESIGN CONSIDERATIONS

Zero voltage switching for the left leg switches (M_1 & M_2) always takes place when the output current source is freewheeling through the output diodes. Thus the available energy, to perform the discharge and charge of capacitor C_1/C_2 within left leg interval $t_{LL,}$ is stored in auxiliary inductor L_1 and the leakage inductor. Thus the condition for achieving ZVS for this leg is, stored energy in inductors should be greater than the energy stored in the capacitors C_1 and C_2.

Energy stored in Capacitors C_1 and C_2 is

$$W_{CR} \ = \frac{1}{2}(\ C_1 + C_2\ ).(V_d\ )^2 = \ C.(V_d\ )^2 \qquad (17)$$

Energy stored in inductors L_{lk} and L_1 is

$$W_L = \frac{(I_0/n)^2}{2}.L_{lk} \ + \frac{(I_{L1})^2}{2}.L_1 \qquad (18)$$

In the expression of stored energy in inductors, the first term represents stored energy in the leakage inductor due to load current and the second term represent energy stored in auxiliary inductor L_1 due to current I_{L1} in it. Hence to achieve ZVS

$$\frac{(I_0/n)^2}{2}L_{lk} + \frac{(I_{L1})^2}{2}L_1 \geq C(V_d)^2 \qquad (19)$$

From equation (12) & equation (19)

$$\frac{(I_0/n)^2}{2}L_{lk} + \frac{(V_d)^2(T_S)^2}{128L_1} \geq C(V_d)^2 \qquad (20)$$

Design efforts should be made to minimize the leakage inductance such that there is minimum duty cycle loss. This also results in minimum voltage overshoot and ringing on the secondary side. To achieve ZVS for the left leg switches independent of load, energy stored in inductor L_1 must be higher than the energy stored in capacitor C_1 & C_2 hence condition for achieving ZVS independent of the load can be obtained by putting $I_0 = 0$ in eq. (20)

$$L_1 \leq \frac{(T_S)^2}{128C} \qquad (21)$$

Another condition for selection of auxiliary inductor L_1 is based on the time interval t_{LL} allowed to charge / discharge the snubber capacitor

$$L_1 \leq \frac{T_S\, t_{LL}}{16C} \qquad (22)$$

Hence, value of L_1 that provide the ZVS of left leg switches for entire load range can be obtained by satisfying the eq. (21) & (22).

Zero voltage switching for right leg switches (M_3 & M_4) takes place when the reflected output current in primary is present. The total current which is available to charge and discharge the capacitor C_3/C_4 linearly within right leg interval t_{RL} is sum of the peak primary current I_1 and auxiliary inductor current I_{L2}. Condition for achieving ZVS for the right leg switches is

$$I_1 + I_{L2} \geq \frac{(C_3 + C_4)V_d}{t_{RL}} \qquad (23)$$

Hence to ensure the ZVS for right leg switches independent of load, value of I_{L2} is given as

$$I_{L2} \geq \frac{(C_3 + C_4)\,V_d}{t_{RL}}; \quad or \; I_{L2} \geq \frac{2CV_d}{t_{RL}} \qquad (24)$$

The value of L_2 for achieving ZVS for right leg switches independent of load can be obtained by using eq. (24) & (8) and given as

$$L_2 \leq \frac{T_S\, t_{RL}}{16C} \qquad (25)$$

Output Voltage of the proposed converter is

$$V_0 = \frac{D_{eff}\, V_d}{n} \qquad (26)$$

D_{eff} is effective duty cycle of the converter and given as

$$D_{eff} = D - \Delta D - t_{LL} - t_{RL} \qquad (27)$$

where D is the duty ratio of the primary voltage of transformer.

V. SIMULATION & EXPERIMENTAL RESULTS

To verify the proposed LLCC auxiliary circuit, a 5 kW DC-DC converter is designed to meet the following specifications: Input voltage V_d = 560 V, (standard full wave rectified voltage of 415 V, 3 phase), adjustable output voltage, Vo = 0-450 V DC, switching frequency f_s = 50 kHz and ZVS for 0-100% of full load.

The main parameters and component values used for simulation as well as in the experimental setup can be obtained from the design procedure presented in section IV and [1,3]. Parameters and components based on the specifications for the FB-PSPSWM dc-dc converter under consideration are given in table I.

TABLE I : Parameters and components of the simulation and experimental circuit

Component/Parameter	Value
M_1 - M_4	IXFN44N80
D_{r1}- D_{r4}, D_c	DSEI2x61-10b
TR	Turn ratio = 0.83:1, Using four Mn-Zn U 93/76/30 ferrite core
Leakage Inductance L_{lk}	50 µH
C_1-C_4	1729 pF
t_{LL}, t_{RL}	700 ns
L_f	1.8 mH
C_f	50 µF
L_1	350 µH
L_2	350 µH
C_{d1},C_{d2}	1 µF
R_c	10 kΩ
C_c	0.47µF

The simulated and experimental waveforms of primary current of the transformer at load current of 10.6 A and at input voltage of 560 V with and without auxiliary circuit are shown in Fig.3a and Fig.3b respectively. From results it is clear that these waveforms are identical and hence it is confirmed that there is no additional duty cycle loss with the auxiliary circuit.

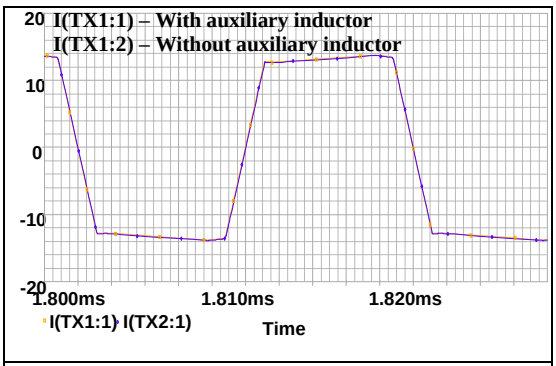

Fig.3a: Simulated waveform for primary current of transformer at full load with and without auxiliary circuit

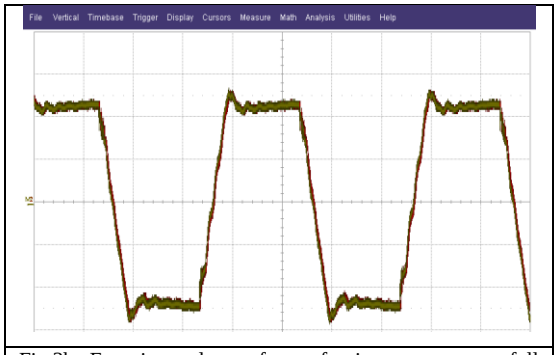

Fig.3b: Experimental waveform of primary current at full load of transformer with (Red) and without (Yellow) auxiliary inductors; X axis (5µs/div), Y axis (5A/div)

The gate-source and drain-source voltage waveform of left leg switch M_2 and right leg switch M_4 are shown in Fig.4a and 4b. The waveforms confirm the ZVS operation of all the switches, as the gate-source voltage appears after the drain-source voltage drops to zero.

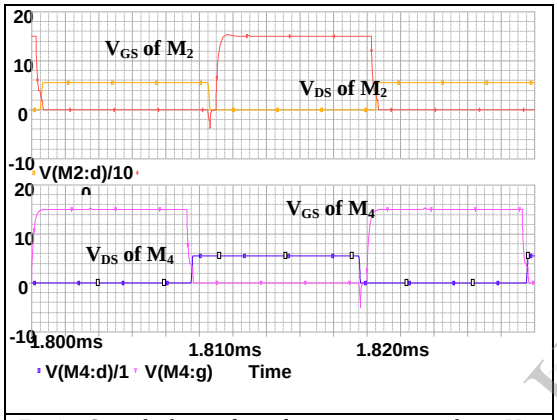

Fig.4a: Simualted waveform for gate-source voltage V_{GS} (5V/div) and drain-source voltage MOSFET M_2 & M_4

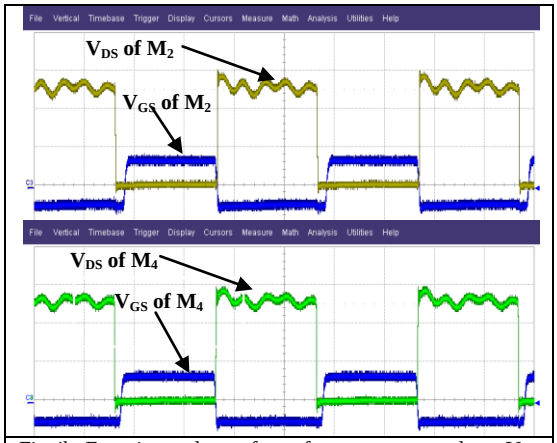

Fig.4b: Experimental waveform for gate-source voltage V_{GS} (5V/div) and drain-source voltage V_{DS} (200V/div) M_2 (Upper) & M_4(Lower); X axis (5µs/div)

Simulated waveforms for drain - source voltage and drain current of MOSFET M_2 & M_4 at 8% of full load current without auxiliary circuit are shown in Fig.5. From the waveforms it is clear that there is no ZVS for the switches at light load. There is high peak current through the switches at light load without auxiliary circuit which results in high switching losses. Under this condition the switch will damage and to protect it switches with higher current rating are required.

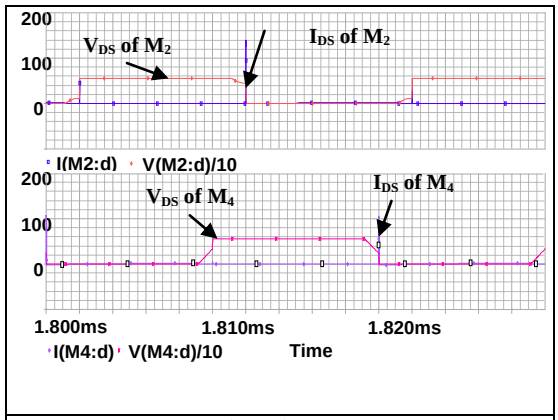

Fig.5: Simualted waveform for drain-source voltage and drain current of MOSFET M_2 & M_4 without LLCC auxiliary circuit

Experimental waveforms of current through auxiliary inductor L_1 and L_2 are shown in Fig.6. The peak current supplied by inductors is 3.6 A for input voltage of 560 V. This additional current is supplied to get the ZVS at light load or no load for left leg and right leg.

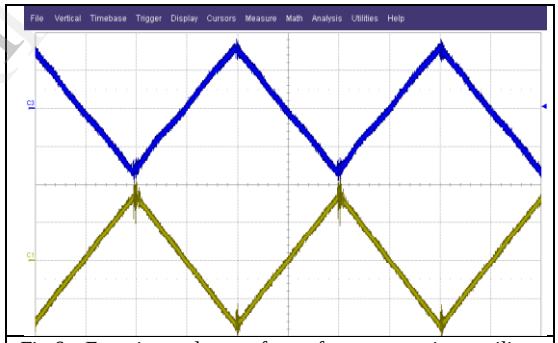

Fig.6: Experimental waveform for current in auxiliary inductor L_1 (Upper) & L_2 (Lower); X axis (5µs/div),Y axis (2A/div)

The simulated and experimental drain–source voltage and drain current waveforms of the switch M_2 of left leg & M_4 of right leg at 95% of full load and 450V output with LLCC auxiliary circuit are shown in Fig.7a and 7b respectively. Similarly the simulated and experimental drain–source voltage and drain current waveforms of the switch M_2 of left leg & M_4 of right leg at 8% of full load and 450V output with LLCC auxiliary circuit are shown in Fig.8a and 8b respectively. Since in all the waveform drain current through the switch crosses the zero after drain-source voltage of switch drops to zero. Hence ZVS of all the switches over the entire conversion range is demonstrated.

Output rectifier waveforms with or without RCD clamp circuit are shown in Fig.9 for input voltage of 385V. Without RCD clamp circuit, there is overshoot of 380 V on rectifier voltage, while with RCD clamp circuit the overshoot is 100 V.

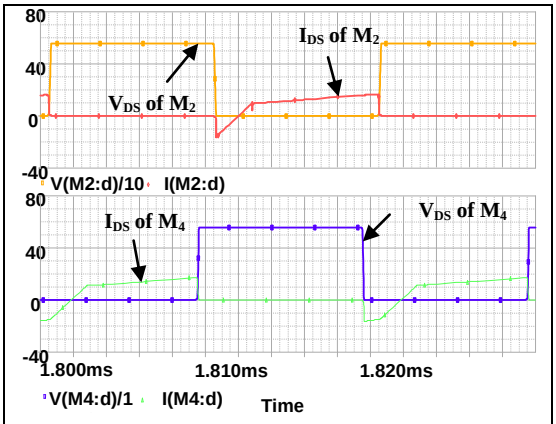

Fig.7a: Simulated waveforms for drain-source voltage and drain current of MOSFET M_2 & M_4 with auxiliary circuit at 95% of load current

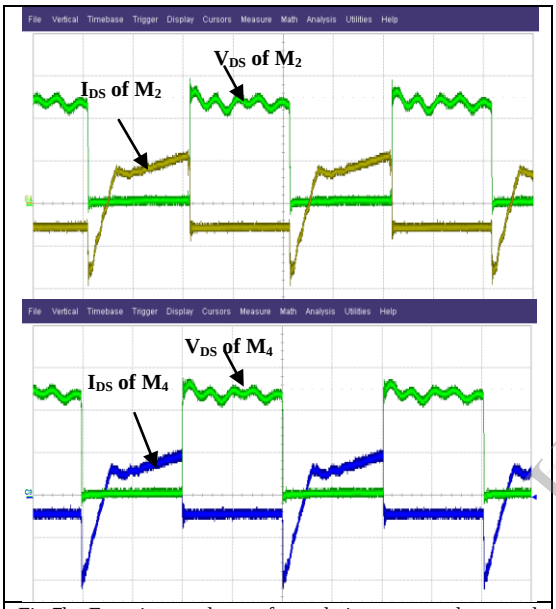

Fig.7b: Experimaental waveform drain-source volatge and drain current of MOSFET M_2 & M_4 auxiliary circuit at 95% of load current; X axis (5µs/div) ,Y axis (V_{DS}: 200V/div, I_{DS} (10A/div))

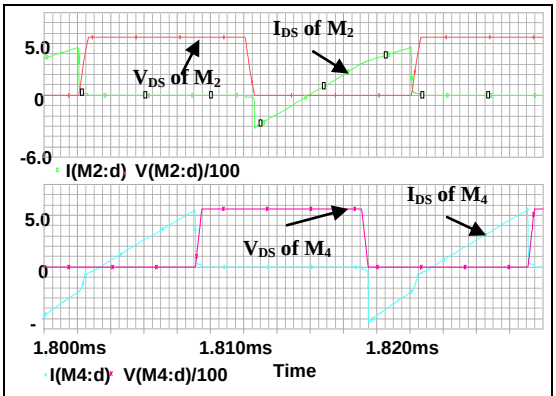

Fig.8a: Simualted waveforms for drain-source voltage and drain current of MOSFET M_2 & M_4 with auxiliary circuit at 8% of full load.

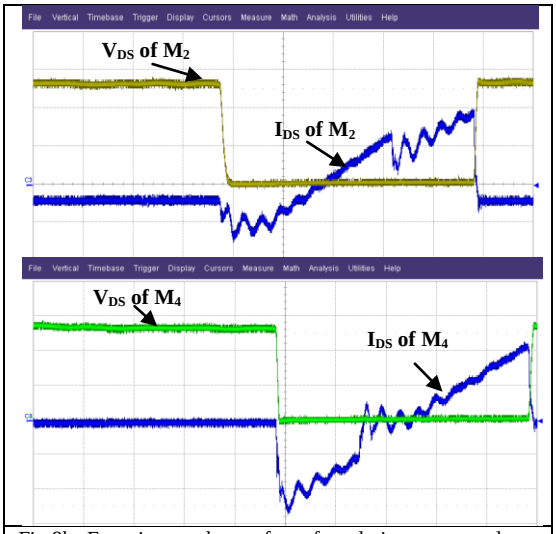

Fig.8b: Experimaental waveform for drain -source voltage and drain current of MOSFET M_2 & M_4 with auxiliary circuit circuit at 8% of full load; X axis (2µs/div) ,Y axis (V_{DS}: 200V/div, I_{DS} :2A/div).

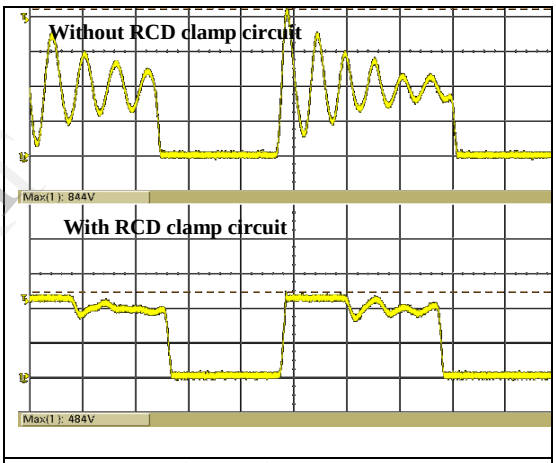

Fig:9: Output rectifier waveform (X- axis 200V/div, Y-axis 2µs/div)

The improvement of efficiency with proposed converter compare to conventional PSPWM converter at light loads depends on switching losses saved by achiveing ZVS operation and the additional conduction losses in the switches due to circulating current and losses in inductor. The saving in switching losses achieved by this ZVS scheme will be very effective for the converters operating at higher swithcing frequency or in higher power converters (> 5 kW) where the snubber capacitors are large (tens of nano-farads).

The efficiency of the FB-PSPWM DC-DC converter developed is around 94% under full power (5 kW) output condition that is with input voltage of 560 V, and output voltage 450 V. The efficency is calculated based on measurement of input and output DC volatge and current.

VI. CONCLUSION

Design, simulation and performance of a high power (5 kW), high voltage dc to dc converter based on modified Full Bridge Phase- Shift PWM topology is presented here that provides zero voltage switching of the switches over the full range of output load. The converter has efficiency of 94% at

full load under nominal input voltage. The modification over conventional Full Bridge Phase Shift PWM DC-DC converter is use of two inductors and two capacitors forming an auxiliary circuit. This enables the converter to achieve zero voltage switching of all the switches independent of load conditions. The simulation and experimental results of the converter demonstrated zero voltage switching over the entire conversion range without any additional duty cycle loss. The only disadvantage of the proposed converter is small increase of the peak current in the switches. This design can be easily adopted for high power DC-DC converter.

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