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Design and Implementation of a Processor using Reversible Logic

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***Abstract*—Reversible logic has presented itself as a prominent Technology which plays an imperative role in Quantum computing. The aim of this project is to design the schematic and layout for a 32-bit processor using reversible logic gates. Beside the functional development, by optimizing the speed of our processor in every block which is inside that, and to minimize the overall delay conventional gates are replaced with reversible gates. This reversible gates which are applicable in Nano technology, Quantum computing, Low power CMOS, Optical computing**.

Index Terms—Reversible gates, Conventional gates, Delay, Low power CMOS, Optical Computing

I. INTRODUCTION

In VLSI which is the growing technology in our day to day life. Everyday new emerging technologies are introducing in market. So the technology development is the most important in our current life. In past the computer occupied the entire room. Gradually the size has reduced and today come to the level of hand based equipment's. At first in any device is made by the IC which is based on the conventional gates. In VLSI it having the ultimate goal is less area, high speed, and low power. In those technologies the CMOS gates are better than the bipolar gates. But the CMOS gates are having its own limitations for that reason we are moving to reversible gates. Reversible logic has received great attention in the recent years due to their ability to reduce the power dissipation which is the main requirement in low power VLSI design. It has wide applications in low power CMOS and Optical information processing, DNA computing, quantum computation and nanotechnology [3]. High-performance chips releasing large amounts of heat impose practical limitation on how far can we improve the performance of the system. Reversible circuits that conserve information, by uncomputing bits instead of throwing them away, will soon offer the only physically possible way to keep improving performance.

II. REVERSIBLE LOGIC

Reversible logic is widely used in low power VLSI. Reversible circuits are capable of back-computation and reduction in dissipated power, as there is no loss of information. Basic reversible gates are employed to achieve the required functionality of a reversible circuit[4]. The uniqueness of reversible logic is that, there is no loss of information since there is one-to-one correspondence between inputs and outputs. This enables the system to run backwards and while doing so, any intermediate design stage can be thoroughly examined. The fan-out of each block in the circuit has to be one [6].In combinational logic circuits as we pack more and more logic elements into smaller and smaller volumes and clock them at higher and higher frequencies. To increase the portability of devices again reversible computing is required. This creates at least three problems: Consume high Energy, Portable systems exhaust their batteries, Systems overheat. According to Landauer's research, the amount of energy dissipated for every irreversible bit operation is at least KTln2 joules, where K=1.3806505*10-23m2kg-2K-1 (joule/Kelvin-1) is the Boltzmann's constant and T is the temperature at which operation is performed[1]. Reversibility in computing implies that no information about the computational states can ever be lost, so we can recover any earlier stage by computing backwards or un-computing the results. This is termed as logical reversibility. The benefits of logical reversibility can be gained only after employing physical reversibility [2].Rather than changing voltages to new levels, reversible circuit elements will gradually move charge from one node to the next. This way, one can only expect to lose a minute amount of energy on each transition. Reversible computing strongly affects digital logic designs [5]. Reversible logic elements are needed to recover the state of inputs from the outputs. It will impact instruction sets and high-level programming languages as well. Eventually, these will also have to be reversible to provide optimal efficiency.

III. BASIC REVERSIBLE LOGIC GATES

There exist many reversible gates in the literature. Among them Feynman gate (FG), Peres gate (PG), Toffoli gate (TG), Fredkin gate (FRG).Because of their simplicity and quantum realization cost there are design approaches and tools that incorporate them separately or in combination with each other [7].

A. Feynman gate (FG)

Feynman gate is a 2*2 one through reversible gate as shown in figure 1. The input vector is I(A, B) and the output vector is O(P, Q). The outputs are defined by P=A, Q=A^B. It is the universal reversible gate.

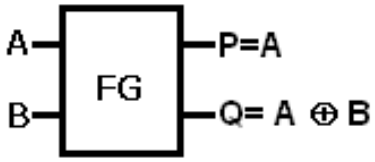

Fig.1 Feynman gate

B. Peres gate (PG)

It is a basic reversible gate which has 3-inputs and 3-outputs having inputs (A, B, C) and the mapped outputs (P=A, Q=A^B, R= (A.B)^C).This PG is depicted in Figure.2

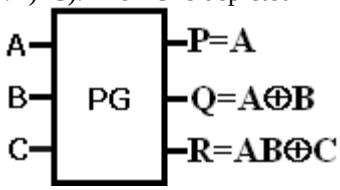

Fig.2 Peres gate

C. Toffoli gate (TG)

Figure.3 shows a 3*3 Toffoli gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The outputs are defined by P=A, Q=B, R=AB^C.

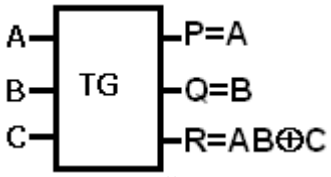

Fig.3 Toffoli gate

D. Fredkin gate (FRG)

It is a basic reversible 3- bit gate used for swapping last two bits depending on the control bit. The control bit here is A, depending on the value of A, bits B and C are selected at outputs Q and R. When A=0, (Q=B, R=C) whereas when A=1, (Q=C, R=B).It is shown in the figure.4

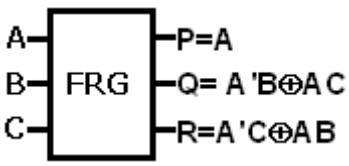

Fig.4 Fredkin gate

IV. Reason for Reversible Logic

Many circuits were designed with using the reversible gates. With one reversible gate we can implement many logic functions. And they all are implemented also verified. The particular reason for going the reversible gates which is it provides the low time delay, less area and consumes low power. This is the ultimate goal for the VLSI design. Behind this reason we've move to reversible gates. But there is a some limitations are given below,

- The output of a certain block in the design can only drive at most one block in the design. Hence it can be said that the Fan-out is restricted to 1.
- Loops are not allowed.
- Though every synthesis method engages them producing less number of garbage outputs, but sometimes garbage outputs are unavoidable.

As the Moore's law continues to hold, the processing power doubles every 18 months. The current irreversible technologies will dissipate a lot of heat and can reduce the life of the circuit. The reversible logic operations do not erase (lose) information and dissipate very less heat. Thus, reversible logic is likely to be in demand in high speed power aware circuits. Reversible circuits are of high interest in low-power CMOS design, optical computing, nanotechnology and quantum computing. The most prominent application of reversible logic lies in quantum computers.

V. Design and Implementation

To this paper we design a processor (it may be RISC, CISC..,) with using the reversible logic gates. In that processor it can hold the many logic blocks with itself. In those blocks we took the main logic block which is ALU block, and design that block with using the reversible gates and also the irreversible gates. At last the two different designs are compared by the use of Time, Power & area (number of LUT's) parameters.

A. Design the ALU block with Irreversible logic

In this ALU block it consists the logic operations, multiplexer, comparator, adder, Subtractor, multiplier etc.., so all the blocks are designed with using the normal gates. To this design the number of gates are increased also power can be doubled. Behind this reason the reversible logic can be introduced. And this design which is done by the QuartusII 9.0 edition and also the Modelsim II 6.4a tools. To using these tools which is very easy to simulate the designs compare the other tools.So to using this tool found the measurements by vaeriy of parameters.

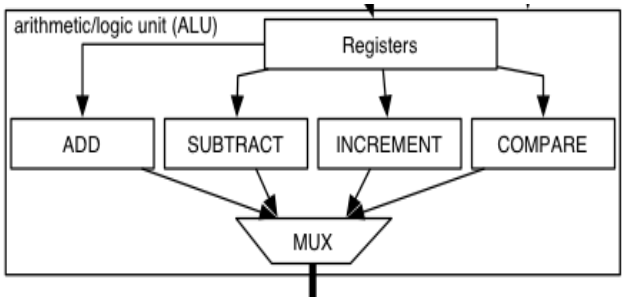

Fig.5 General ALU block

B. Power, Time & Area analysis

The power analysis, timing analysis and also the Area summary can be done by the QuartusII tool. In this paper compare the reversible logic and also the irreversible

logic designs for the same ALU blocks. But the block structure only is the difference between two designs. Under this topic the irreversible logic can be discussed in following sections.

In this timing analysis the Fmax summary which is generate the timing results. Fmax=81.06MHz, i.e.., T=0.012µs.The Total power of this irreversible logic is 98.46mW (dynamic power=13.5mW+static power=46.19mW+input/output power=38.67mW).The total area which is included the 256 Number of registers, 427 number of logic elements.

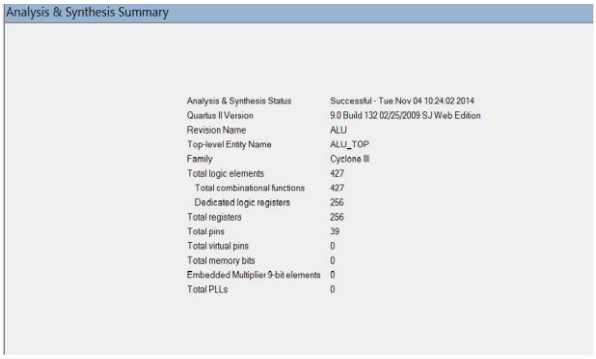

Fig.6 Analysis and simulation summary (Irreversible logic)

C. *Design the ALU block with Reversible logic*

The Reversible logic gates are used to design the ALU block which is depicted the figure.5.And this logic can be done by the variety of the reversible logic gates. And that schematic diagram which is shown in the Fig.7. Then this diagram consists the both part and adder/Subtractor unit.

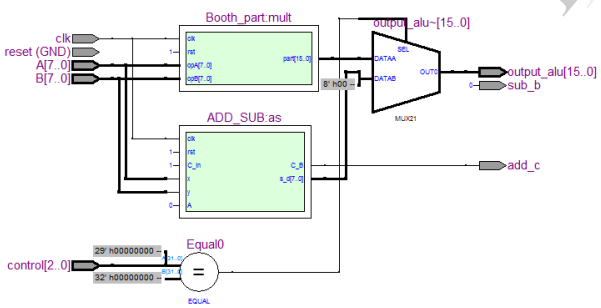

Fig.7 Schematic unit

Define abbreviations and acronyms the first time they are used in the text, even after they have been defined in the abstract. Abbreviations such as IEEE and SI do not have to be defined. Do not use abbreviations in the title or heads unless they are unavoidable.

D. *Power, Time & Area analysis*

The power analysis, timing analysis and also the Area summary can be done by the QuartusII tool. In this paper compare the reversible logic and also the irreversible logic designs for the same ALU blocks. But the block structure only is the difference between two designs. Under this topic the irreversible logic can be discussed in following sections.

In this timing analysis the Fmax summary which is generate the timing results. Fmax=1127.4MHz, i.e.., T=8.86Gs.The Total power of this irreversible logic is 72.30mW (dynamic power=0.43mW+static power=46.13mW+input/output power=25.74mW).The total area which is included the 14 Number of registers, 37 number of logic elements. The analysis and simulation of the reversible logic which is depicted the figure.8.

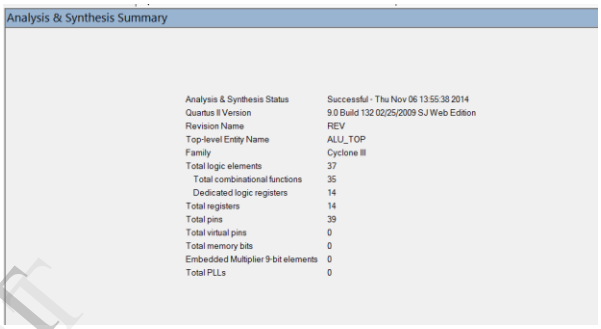

Fig.8 Analysis and simulation summary(Reversible logic)

I. Table

Type of logic	Time	Area	Power
Irreversible	0.012µs	256	98.46mW
Reversible	8.86Gs	14	72.30mW

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