Published by :
http://www.ijert.org

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 5 Issue 08, August-2016

Design and Implementation of Advanced Array Multiplier for Binary Multiplication on FPGA

Pramod V Rampur[1]
Dept. of Electronics and Communication Engineering
PESITM, Shivamogga, karnataka

Jagadish M[2]
Dept. of Electronics and Communication Engineering
PESITM, Shivamogga, karnataka

Yogeesha G[3]
Dept. of Electronics and Communication Engineering
PESITM, Shivamogga, karnataka

***Abstract*— Multiplication is crucial building block of Image Processing, Digital Signal Processing (DSP) applications like Fast Fourier Transform (FFT), Digital Filters etc. To achieve High Execution Speed or to meet the performance demands in DSP applications Parallel Array Multiplier are used to perform Multiplication. In this paper, an Advanced Array Multiplier using different types of compressors was designed and implemented on FPGA. The area consumed by Braun's Multiplier was reduced by using the different order compressors. The comparison of device utilization summary for conventional and proposed array design is presented.**

***Keywords*— Array Multiplier, Braun Multiplier, IFFT, OFDM**

I. INTRODUCTION

Multipliers play a significant role in advanced digital signal processing. In modern day processors addition and multiplication of two binary numbers are frequently used arithmetic operations and share more than 70 percent of the execution time. This necessitates the need for high speed processing for expanding computer and signal processing applications. Diverse multipliers and adders such as Braun Multiplier, Wallace Multiplier, Booth Multiplier, Array Multiplier, Sequential Multiplier, and Combinational Multiplier, Half adder, Full Adder and Ripple Carry Adder are realized in [1-8]. Researchers ameliorate these designs with the aim to scale down the complexity in the design and execution time.

In this paper, an array multiplier is realized using different type of compressor on FPGA. The area consumed by the multiplier was analyzed and treated for reduction using different higher order compressor.

II. SYSTEM DESIGN

The architecture of the multiplier was divided into three stages- a partial product generation stage, a partial product addition stage and final addition stage.

A. Conventional Array Multiplier

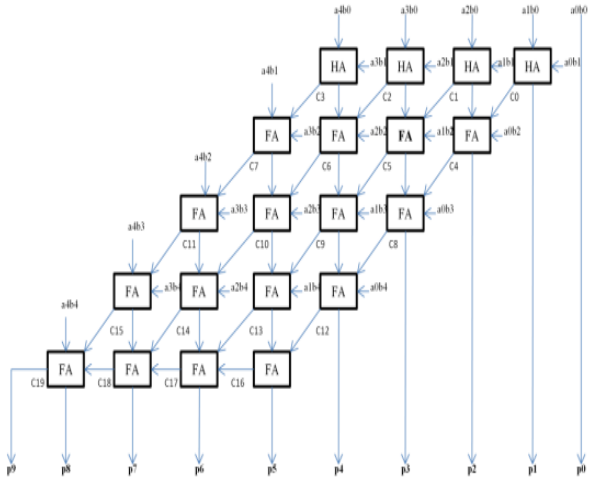

Fig 1: Conventional Array Multiplier

The process of binary array multiplication involves the AND operation of multiplicand and multiplier bits and subsequent addition [3]. As shown in Fig. 1, the conventional array multiplier comprises sixteen full adders and four half adders. The carry generated by each half or full adder is diagonally forwarded to the next row of the adder. In the last stage, carry and sum are united in the ripple carry adder.

B. Proposed Advanced Array Multiplier

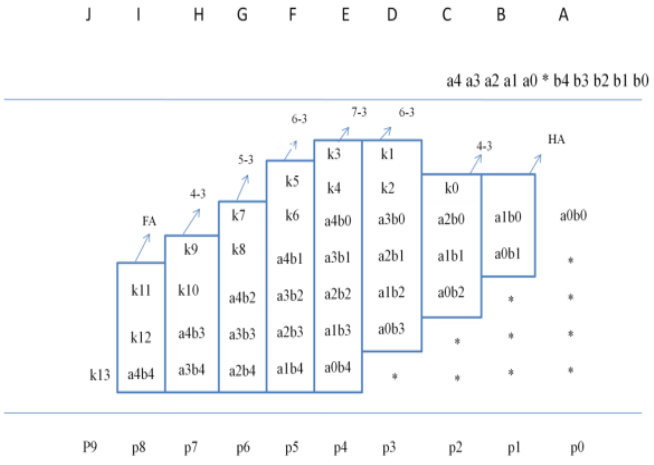

Fig. 2 Multiplication of two 5 bit binary numbers

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 5 Issue 08, August-2016

Fig. 2 shows the proposed array multiplier for multiplication of two 5-bit binary numbers. Here, the partial products are generated by AND operation and then they are added using different compressors i.e., 4:3 compressor, 5:3 compressor, 6:3 compressor and 7:3 compressor along with half adder and full adder.

Consider A=25(11001) and B=9(01001)
Expected result=>25*9=225(011100001)

```
                11001
              * 01001
---------------------------
                11001
               00000*
              00000**
             11001***
            00000****
---------------------------
             011100001
```

III. COMPRESSOR

Compressors are primary component of the multiplier. Large delay was observed in partial products addition stage that increase the amount of power consumed. Using compressor adders, that add four, five, six or seven bits at a time, the number of full adders and half adders are reduced and hence the power consumed is less.

A. 4 : 3 Compressor

In a 4:3 compressor, if A, B, C and D are the inputs and Z_2, Z_1 and Z_0 are outputs then Z_2, Z_1 and Z_0 provides the count of the number of 1's at inputs A,B,C and D. The design of 4-3 compressor and Counter Property of 4-3 compressor are shown in Fig. 3.

Inputs	Outputs			Decimal equivalent
	z0	z1	z0	
All inputs are zero	0	0	0	0
Any one input is 1	0	0	1	1
Any two inputs are 1	0	1	0	2
Any three inputs are1	0	1	1	3
Any four inputs are 1	1	0	0	4

Fig. 3 Compressor (4 : 3)

B. 6:3 Compressor

In a 6:3 compressor, if A, B, C , D, E and G are the inputs and Z_2, Z_1 and Z_0 are outputs then Z_2, Z_1 and Z_0 provides the count of the number of 1's at inputs A, B, C, D, E and G. The design of 6-3 compressor and Counter Property of 6-3 compressor are shown in Fig 4.

Inputs	Outputs			Decimal Equivalent
	z0	z1	z0	
All inputs are zero	0	0	0	0
Any one input is 1	0	0	1	1
Any two inputs are 1	0	1	0	2
Any three inputs are1	0	1	1	3
Any four inputs are 1	1	0	0	4
Any five inputs are 1	1	0	1	5
All six inputs are 1	1	1	0	6

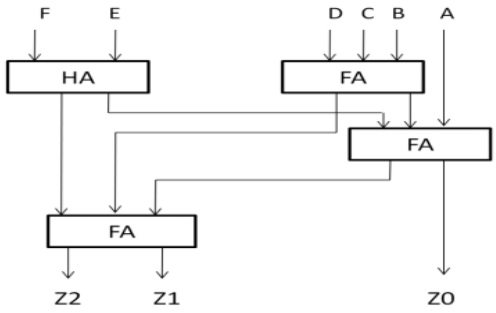

Fig. 4 Compressor (6 : 3)

C. 7:3 Compressor

In a 7:3 compressor, if A, B, C , D, E, G and F are the inputs and Z_2, Z_1 and Z_0 are outputs then Z_2, Z_1 and Z_0 provides the count of the number of 1's at inputs A, B, C, D, E, G and F. The design of 7-3 compressor and Counter Property of 7-3 compressor [1] are shown in Fig. 5.

Inputs	Outputs			Decimal Equivalent
	z0	z1	z0	
All inputs are zero	0	0	0	0
Any one input is 1	0	0	1	1
Any two inputs are 1	0	1	0	2
Any three inputs are1	0	1	1	3
Any four inputs are 1	0	0	0	4
Any five inputs are 1	1	0	1	5
Any six inputs are 1	1	1	0	6
All seven inputs are 1	1	1	1	7

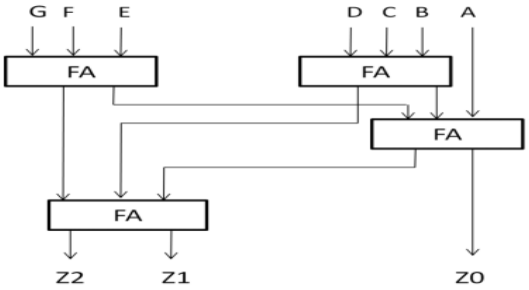

Fig. 5 Compressor (7 : 3)

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 5 Issue 08, August-2016

IV. SIMULATION RESULTS

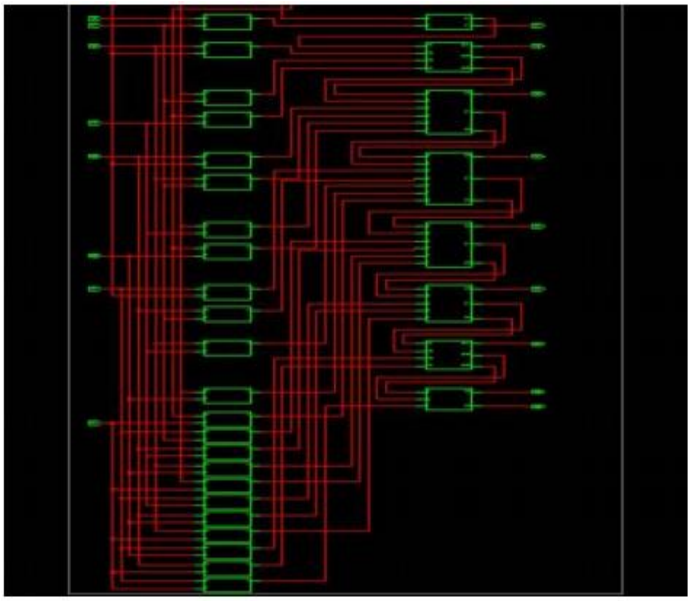

Fig. 6 RTL Schematic of Advanced Array Multiplier

Schematic of the proposed Advanced Array Multiplier is as shown in Fig 6. This Advanced Array Multiplier is designed using Half Adder, Full Adder and different compressors such as 4-3 compressor, 5-3 compressor, 6-3 compressor and 7-3 compressor. The number of adders is minimized by introducing different high order compressors.

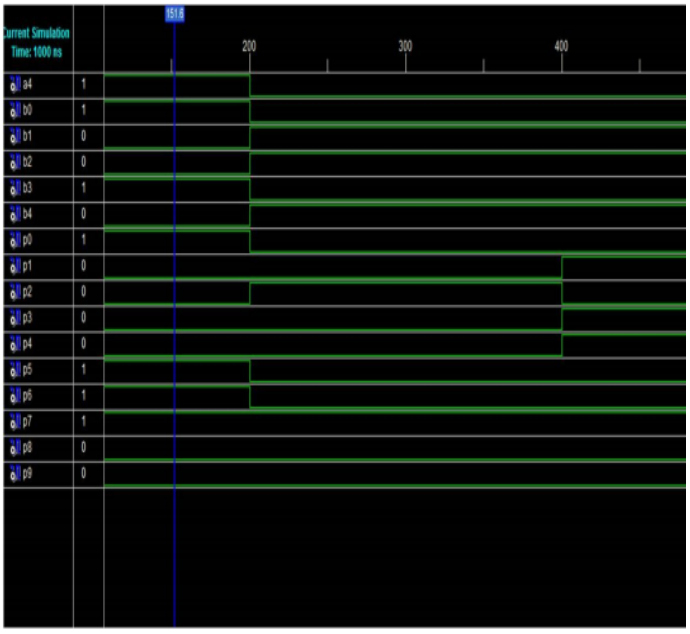

Fig.7 Simultaion results

Simulation Result of the proposed Advanced Array Multiplier is as shown in Fig 7. Here, the input is 5x5 bits data and output is 10 bit data. For example let A=11001 be the multiplicand and B=01001 be the multiplier and product of these two is Y=0011100001.

TABLE I. COMPARISON OF DEVICE UTILIZATION SUMMARY

Logic Utilization	Conventional Array Multiplier	Advanced Array Multiplier
Number of Slices	30	28
Number of 4 input LUTs	52	48
Number of bonded IOBs	20	20

Comparison of Device Utilization Summary for conventional Array Multiplier and Advanced Array Multiplier is as shown in Table. 1. As depicted in the table, the device utilization parameters such as number of slices, number of 4-input LUTs are less in the proposed design compared to the conventional design. The number of bonded IOBs remains same for both the designs.

V. CONCLUSION

To speed up Array Multiplier, Wallace tree and Booth multipliers, compressors are the key in partial product reduction. The use of compressors in the multipliers not only reduces the vertical critical path but also reduce the stage operations simultaneously. To show better performance the compressors are tested with efficient adders and showed that large Binary Multiplication Advanced Array Multiplier performs better than the Conventional Array Multiplier in term of area.

VI. ACKNOWLEDGEMENT

This work was carried out under the infrastructure provided by the Department of Electronics & Communication Engineering, PESITM, Shivamogga. The authors would like to thank the Head of the Department, Principal and Management of the Institution to provide their support throughout the work.

REFERENCES

[1] Mr. Ravi Nirlakalla, Mr. Thota Subba Rao, Mr. Talari Jayachandra Prasad "Performance Evaluation of High Speed Compressors for High Speed Multipliers", Serbian Journal Of Electrical Engineering Vol. 8, No. 3, November 2011, 293-306.

[2] Nidhi Pokhriyal, Neelam Rup Prakash "Area Efficient Low Power Compressor Design Using GDI Technique" , International Journal of Engineering Trends and Technology (IJETT) – Volume 12 Number 3 - Jun 2014.

[3] A. M. Borkar, Mr. A. K. Sharma, Mr. Y. M. Gaidhane5 N. S. Panchbudhe, Mr. N. D. Bhomle " VHDL Implementation of Low-Power Sign and Unsigned 5-Bit Multiplier" , International Journal of Advanced Research in Computer Science and Software Engineering Volume 3, Issue 7, July 2013 ISSN: 2277 128X.

[4] Mr.Mohammed H. Al Mijalli "Braun's Multipliers: A Delay Study", Proceedings of the World Congress on Engineering 2012 Volume IIWCE 2012, July 4 - 6, 2012, London, U.K.

[5] Aditya Kumar Singh, Bishnu Prasad De, Santanu Maity "Design and Comparison of Multipliers Using Different Logic Styles", International Journal of Soft Computing and Engineering (IJSCE) ISSN: 2231-2307, Volume-2, Issue-2, May 2012.

[6] Soniya, Suresh Kumar " A Review of Different Type of Multipliers and MultiplierAccumulator Unit", International Journal of Emerging Trends & Technology in Computer Science (IJETTCS) Volume 2, Issue 4, July – August 2013.

[7] Mr. A. Bellaouar, M.I. Elmasry"Low-power Digital VLSI Design Circuits and Systems" Kluwer Academic Publishers, Boston, USA, 1995.

[8] V.G. Oklobdzija, D. Villeger, S.S. "Liu A Method for Speed Optimized Partial Product Reduction and Generation of Fast Parallel Multipliers using an Algorithmic Approach", IEEE Transaction on Computers, Vol. 45, No. 3, March 1996, pp. 294 – 306.