Design and Implementation of FIR Filter Using Multi-Bit Flip-Flops

S. Mani
PG Scholar/ VLSI & Embedded System
B.S.Abdur Rahman University
Chennai, India
mani.kvsr@gmail.com

Mrs.S. Kalaivani
Assistant Professor/ Department of ECE
B.S.Abdur Rahman University
Chennai, India
skalaivani@bsauniv.ac.in

***Abstract*— Power consumption is an important issue in modern high frequency and low power VLSI design. In modern VLSI designs, power consumed by clocking is taken as a major part of the design. The basic memory elements of designer considerations are Latch and flip flop. One way to improve the flip-flop performance is to merge the clock pulse given to multiple flip-flops. Multi-bit flip-flop is designed by single clock pulse thereby maintaining the same functionality as that of two single-bit flip-flop. In the proposed work, different tap size of FIR filter is designed using multi-bit flip-flops and its performance comparison over the single-bit flip-flop is verified. The FIR filter is coded using Verilog HDL and synthesized in FPGA of family Virtex-5**(XC5VLX110T-FF136) **using Xilinx ISE 14.5 Simulator and it has been concluded from the comparison that the clock buffer, number of flip-flop used, gate delay and net delay are reduced by using multi-bit flip-flops.**

***Index Terms*—Clock power reduction, SBFF, MBFF, Merging, FIR filter, Multipliers, Adders**

I. INTRODUCTION

Finite impulse response (FIR) is a commonly used digital filter in many digital signal processing (DSP), motion estimation, noise reduction, image and video processing applications [1]. FIR Filters are widely used because they have linear phase characteristics and guaranteed stability. Digital filters are mainly used for removing the undesirable parts of the input signal such as random noise or components of a given frequency content. Finite impulse response (FIR) filter, also known as non recursive filters (in a non recursive filter the current output is calculated solely from the current and previous input values). Direct form FIR filters are also known as tapped delay line or transversal filters [2] and [3].

Figure 1 shows an ASIC chip power distribution. The flip-flops on clock tree accounted for 27% of the total power consumption and its contribution goes to 43% when only the dynamic power component is considered [4]. The power consumed by clocking can be reduced further by replacing several flip-flops with multi-bit flip-flops. Using multi- bit flip-flops can reduce clock dynamic power and the total flip-flop area effectively [5].

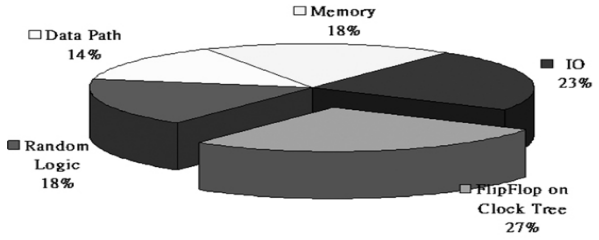

Fig. 1 Examples of ASIC chip power distribution

Fig. 2 shows the basic structure of single-bit flip-flop. A single-bit flip-flop has two latches (Master latch and Slave latch) [6] and [7]. The latches need CLK and CLK` signals to perform operations, such as figure2 shows.

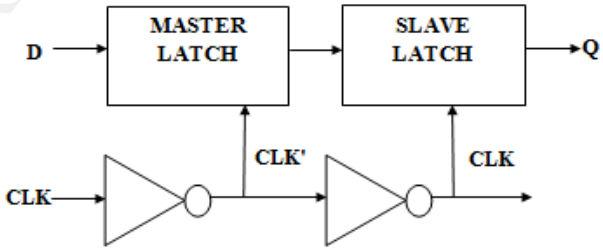

Fig. 2 Single-bit flip-flop

The rest of the paper is organized as follows. Section II introduces the concept of multi-bit flip-flop methodology. Section III presents the proposed FIR filter implementation. Section IV describes the experimental results such as RTL schematic, simulation and comparison of various tap size of FIR filter and Section V concludes the paper.

II. MULTI-BIT FLIP-FLOP METHODOLOGY

Fig. 3 (a) and (b) shows the block diagrams of 1- and 2-bit flip-flops. The two 1-bit flip-flops as shown in Fig. 3(a) are replaced by the 2-bit flip-flop as shown in Fig. 3(b), the total power consumption can be reduced because the two 1-bit flip-flops can share the same clock buffer. Each 1-bit flip–flop contains two inverters, which generate opposite-phase clock signals [9]. Replacing several 1-bit flip-flops with one MBFF will significantly reduce the number of inverters.

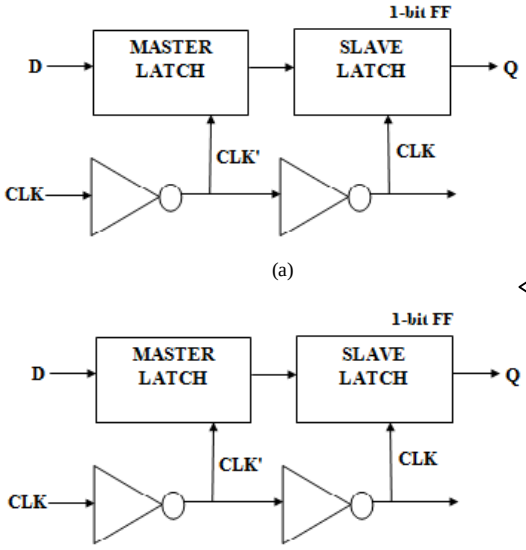

Fig. 3 (a) 1-bit flip-flops (before merging).

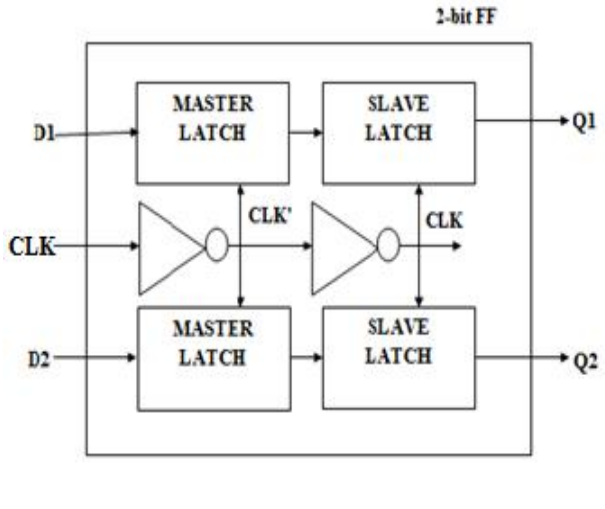

Fig. 3 (b) 2-bit flip-flops (after merging).

A. Multi-Bit Flip-flops

Fig. 4 shows the basic block diagram of multi-bit flip-flop. It takes multiple data input and results in multiple data output. The working of multi-bit flip flop is same as single-bit flip-flop, whenever the clock gets active state flip- flop latches all input to output and remaining state the flip-flop holds the data.

Applying to [5] and [6], MBFFs may have the following advantages:

1) Smaller design area due to shared clock drivers and clock gating cells.
2) Less delay and power of the clock network due to fewer clock sinks.
3) Controllable clock skew because of common clock and enable signals for a group of flip-flops.
4) Improved routing resource utilization especially when considering design for testability. The required routing resource for a scan chain is greatly reduced because of fewer cells in a scan chain.

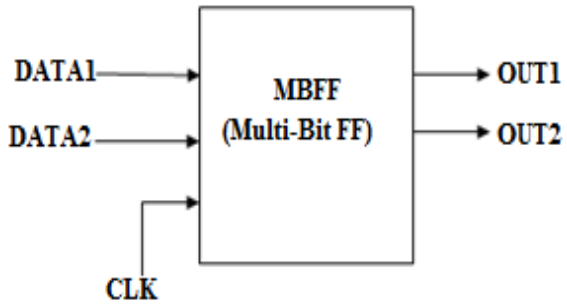

Fig. 4 Multi-bit flip-flops

III. FIR FILTER IMPLEMENTATION

The Fig. 5 shows the basic structure of direct form 5-tap FIR filter because the multiplier coefficients are obtained directly from the filter transfer function. The size of the FIR filter is sometimes expressed in taps which is the number of delay elements+1[7]. Consider the five tap finite impulse response (FIR) filter.

$$Y(k) = H1x(k) + H2x(k-1) + H3x(k-2) + H4x(k-3) + H5x(k-4) \quad (1)$$

In the Eq. 1 Y (k) is known as output signal and x (k) is known as input signal. For an N order filter the number of shift register and adders required is N and the number of multipliers required is N+1[8].

A. 5-Tap FIR Filter Using Single-Bit Flip-Flops

Fig. 5 shows the basic structure of five-tap FIR filter using single-bit flip-flops. The implementation of an FIR requires three basic building blocks such as Signal Delay, Adder and Multiplier.

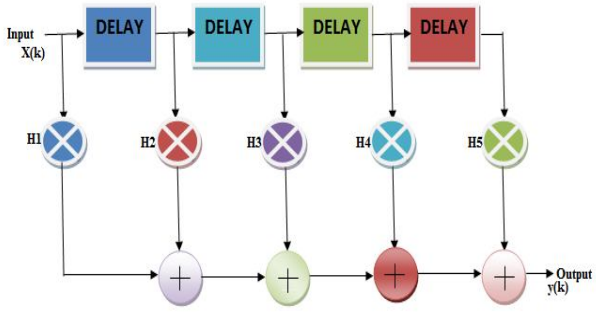

Fig. 5 Five tap direct form FIR filter diagram

B. 5-Tap FIR Filter Using Multi-Bit Flip-Flops

Fig. 6 shows the modified architecture of five-tap FIR filter using multi-bit flip-flops. In normal 5-tap FIR filter, the output is obtained at 4th clock pulse. In the proposed technique, we obtain the output at 2nd clock pulse. Thus the proposed FIR filter designed by multi-bit flip-flops has the advantage in terms of area, delay and power consumption. Therefore, the circuit performance is high compared to FIR filter designed by single-bit flip-flops. In this architecture, we have used carry look ahead adder and array multiplier for implementing FIR filter.

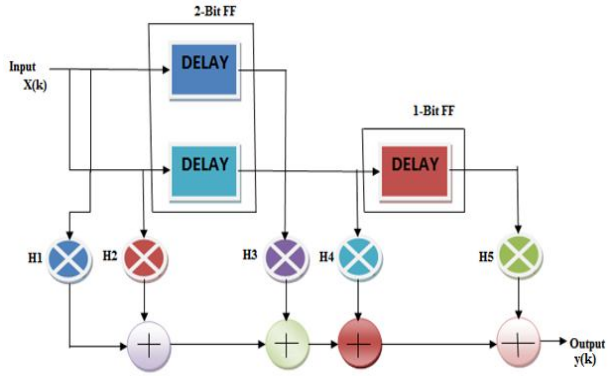

Fig. 6 Five-tap Direct form FIR filter diagram using MBFF

C. Delay

The unit delay provides a one sample signal delay. A sample value is stored in a memory slot for one sample clock cycle, and then made available as an input to the next processing stage. An *M*-unit delay requires *M* memory cells (note each memory cell must store say *B*-bits) configured as a shift register (*B*-bits wide).

D. Multipliers

In a DSP system the multiplier must be fast and must have sufficient precision (bit width) to support the desired application. A high quality filter will in general require more multiplications than one of lesser quality, so throughput suffers if the multiplier is not fast.

E. Adders

Signal addition is a very basic DSP function. In an FIR filter additions are required in combination with multiplications, hence DSP Microprocessors feature multiply-accumulate (MAC) units. Adders generally operate with just two inputs at a time.

F. 7-Tap FIR Filter Using Multi-Bit Flip-Flops

Fig. 7 shows the modified block diagram of seven-tap FIR filter using multi-bit flip-flops. In general 7-tap FIR filter, we get the output at 6th clock pulse. In the proposed technique, output is obtained at 3rd clock pulse. Therefore, half of the delay is reduced and performance of the circuit is high by applying multi-bit flip-flops.

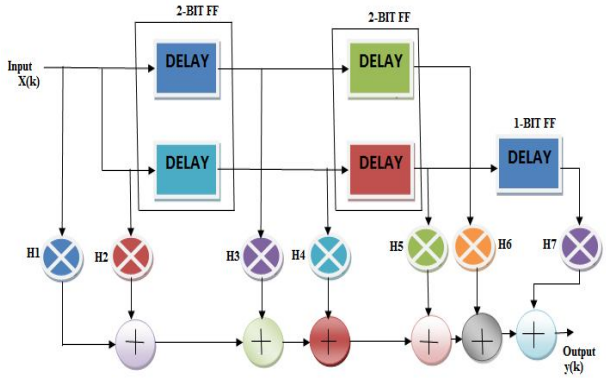

Fig. 7 Seven-tap Direct form FIR filter diagram using MBFF

G. 9-Tap FIR Filter Using Multi-Bit Flip-Flops

Fig. 8 shows the modified architecture of nine-tap FIR filter using multi-bit flip-flops. In general 9-tap FIR filter, we get the output at 8th clock pulse. In the proposed technique, we get the output at 2nd clock pulse. Therefore, delay is reduced and speed of the circuit performance is increased and also power consumption, area of the circuit is reduced due to multi-bit flip-flops.

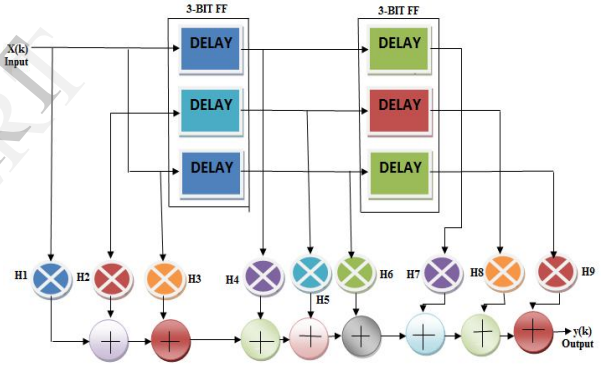

Fig. 8 Nine-tap Direct form FIR filter diagram using MBFF

IV. Experimental Results

This section shows our experimental results. The Single-Bit Flip-Flop and Multi-Bit Flip-Flops are successfully experimented using Xilinx ISE 14.5 Simulator. The various tap size of FIR filter are designed using both SBFF and MBFF and simulated using Verilog HDL. The proposed architecture is implemented using FPGA of family Virtex-5(XC5VLX110T-FF136). The tap coefficients are chosen randomly with an objective to provide something that is observable at the output of FIR filter. These taps could be changed depending on the requirement of the application. The functionality of the FIR filter is verified using Xilinx ISE 14.5 Simulator. The below table I, table II, and table III shows the number of flip-flops used, clock buffer and period analysis as Gate delay and Net delay on various tap size of FIR filter using SBFF and MBFF.

TABLE I. COMPARISON OF 5-TAP FIR FILTER USING SBFF AND MBFF

TAP SIZE	5-TAP FIR FILTER	
NUMBER OF FLIP-FLOP USED	4-SBFF	1-2BIT FF 1-SBFF
CLOCK BUFFER	16	12
GATE DELAY	1.809ns	1.765ns
NET DELAY	0.418ns	0.374ns
DELAY	18.985ns	17.576ns

TABLE II. COMPARISON OF 7-TAP FIR FILTER USING SBFF AND MBFF

TAP SIZE	7-TAP FIR FILTER	
NUMBER OF FLIP-FLOP USED	6-SBFF	2-2BIT FF 1-SBFF
CLOCK BUFFER	24	20
GATE DELAY	1.849ns	1.787ns
NET DELAY	0.458ns	0.396ns
DELAY	26.127ns	24.408ns

TABLE III. COMPARISON OF 9-TAP FIR FILTER USING SBFF AND MBFF

TAP SIZE	9-TAP FIR FILTER	
NUMBER OF FLIP-FLOP USED	8-SBFF	2-3BIT FF
CLOCK BUFFER	32	19
GATE DELAY	1.854ns	1.765ns
NET DELAY	0.463ns	0.374ns
DELAY	32.538ns	28.610ns

A. RTL View of 5-Tap FIR Filter Using Single-Bit Flip-Flops

The Fig. 9 shows the RTL schematic of 5-Tap FIR filter using SBFF.

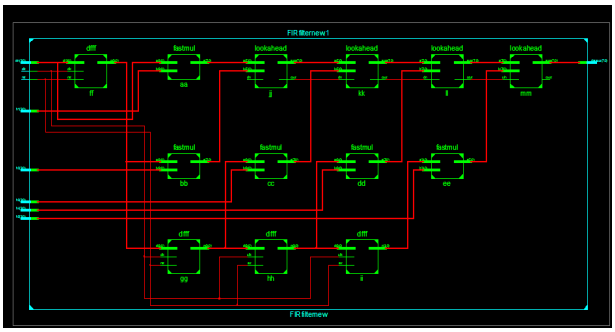

Fig. 9 RTL schematic of 5-tap FIR filter using SBFF

B. RTL View of 5-Tap FIR Filter Using Multi-Bit Flip-Flops

The Fig. 10 shows the RTL schematic of 5-Tap FIR filter using MBFF.

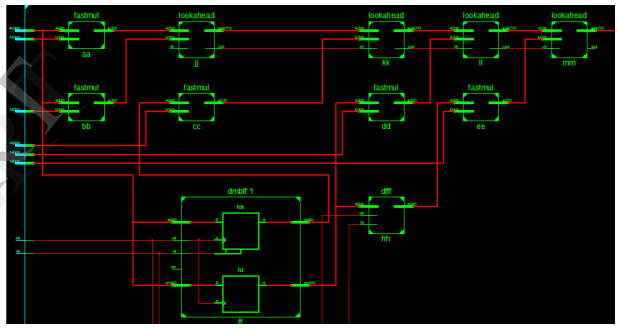

Fig. 10 RTL schematic of 5-tap FIR filter using MBFF

C. Simulation Of 5-Tap FIR Filter Using Single-Bit Flip-Flops

The Fig. 11 shows the simulation result of 5-Tap FIR filter using SBFF.

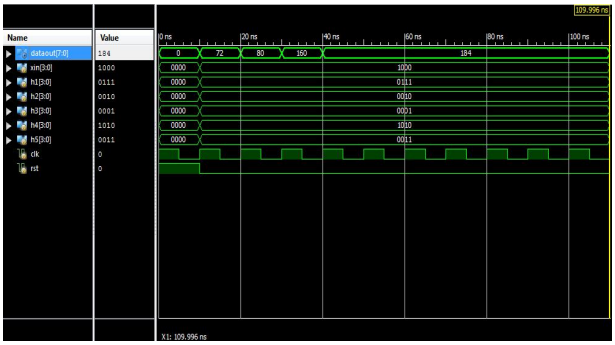

Fig. 11 Simulation waveform for 5-tap FIR filter using SBFF

D. Simulation Of 5-Tap FIR Filter Using Multi-Bit Flip-Flops

The Fig. 12 shows the simulation result of 5-Tap FIR filter using MBFF.

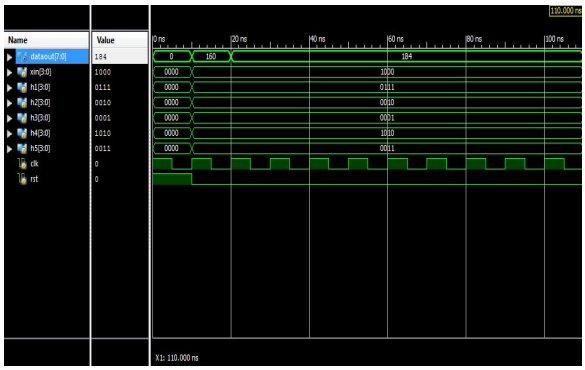

Fig. 12 Simulation waveform for 5-tap FIR filter using MBFF

V. CONCLUSION

In this paper, we have presented a single-bit flip-flop and multi-bit flip-flops. Various taps size of direct form FIR filter has been designed using SBFF and MBFF. We have implemented 5-tap, 7-tap and 9-tap FIR filter using SBFF and MBFF and realized in FPGA of family Virtex-5 using Xilinx ISE 14.5 Simulator. We analyzed the parameter such as number of Flip-flop used, Gate delay, Net delay and Clock buffer in the design of different taps of FIR filter using SBFF and MBFF. It has been concluded from the comparison that the number of flip-flop used, Gate delay, Net delay, power consumption and clock buffer parameter are reduced by using multi-bit flip-flops over single-bit flip-flop.

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