International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 4 Issue 07, July-2015

Design and Implementation of First Two Stages of HFB ADC using Cadence Virtuoso Tool

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***Abstract*— An hybrid filter bank analog-to-digital converter (HFB ADC) uses analog analysis filters to allocate a frequency band to each ADC in the array and digital synthesis filters to reconstruct the digitized signal. The first two stages of filter banks and ADC's are implemented using 180nm CMOS process. A HFB ADC of Resolution 16bits in which the sampling frequency is 4 MHz was designed for the frequency 100 KHz to 800 KHz with a band-width of 100 KHz using Virtuoso which is the main layout editor of Cadence. Signal to noise ratio is 25.84 dB was obtained for 4 bits with a response time for the Flash ADC being 100ns. The area of the layout for ADC obtained was 1748 um^2. Layouts were generated at transistor level and it can be integrated to meet the required design specifications**

Keywords—ADC, CMOS, HFB, Filters, Frequency bands, Quantization, Sample and hold.

I. INTRODUCTION

Wireless communication system plays an important role to drive day-to-day communications in everyday life. Powerful communication systems can be achieved by configuring the right devices based on the applications. All communication based devices are known as mixed signal design. In mixed signal designs data converters play a vital role to construct the proper communication between the sender and the receiver. Data converters are recognized for converting one form of input signal to another. There are two types of data converters namely Analog to Digital converters (ADC) [1] and Digital to Analog converters (DAC). Digital to Analog converter is used to convert digital signals into analog signals. Analog to Digital converters translates the analog inputs into digital outputs which is used in processing information, data transmission, storing, computing and control systems.Hybrid Filter Bank (HFB) [2] analog to digital converters are multirate system's that uses a three stage process that is analog frequency band decomposition through an analysis filter bank, analog to digital conversion and finally digital reconstruction using synthesis filter bank. This paper describes the implementation of the first two stages of HFB ADC. The hybrid filter bank analog-to-digital converter (HFB ADC) uses analog analysis filters to allocate a frequency band to each ADC in the array and digital synthesis filters to reconstruct the digitized signal. In HFB technique the analog filters will split the input frequencies into different sub bands. Each ADC has to then digitize each sub bands at the sampling rate. The analysis structure is then followed by up samplers and digital synthesis filters. Finally, the channels are recombined at the output, which completes the architecture. The first two stages of filter banks and ADC's are implemented using 180nm CMOS process. Resolution of HFB ADC is 16bits in which the sampling frequency is 4 MHz, input frequencies are 100 KHz to 800 KHz with bandwidth of 100 KHz.
Section II of the paper describes the basic theoretical concepts of a HFB ADC. This is followed by the implementation in section III and results in section IV.

II. THEORITICAL BACKGROUND

A. Basic Architecture

An ADC takes a range of real number line and divides into smaller sub ranges. The size of each sub-range is often referred as step size. During the conversion process input samples are taken and mapped on to the real number line. Filter banks are the important blocks of HFB ADC's which allow the input signals to be divided into simpler frequency band for making processing simpler. A Filter bank is a set of M frequency selective filters in parallel that partitions the frequency range of the input signal spectrum into M adjacent frequency bands. To partition the available frequency band can be beneficial and can be used in case of HFB ADC's where a reduced signal bandwidth allows for a reduced sampling rate and if errors occur during sampling and quantization become attenuated by filters. Fig. 1 shows the HFB architecture. But in TIADC [3] each channel in an ADC array possesses errors like a single ADC; however, a system of parallel ADCs produces additional errors, which are caused by component mismatches among the ADCs in the system and are therefore called mismatches.

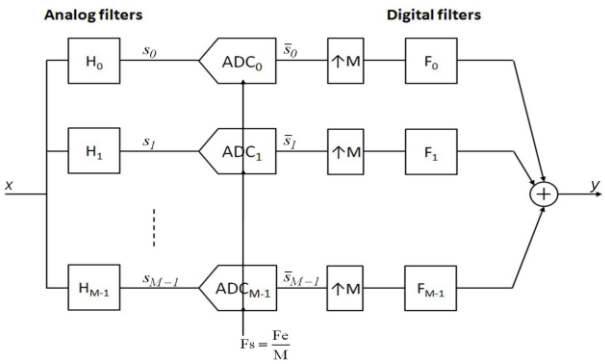

Fig.1: HFB Architecture.

B. Band Pass filters

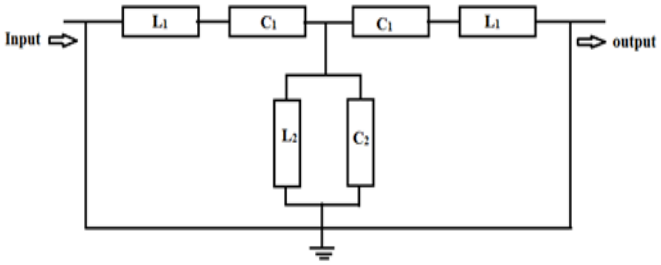

Fig. 2: Constant K band pass filter.

The band pass filters used are constant K type filter [4]. This consists of resistors, inductors and capacitors as components. Fig. 2 shows the constant K band pass filter. There are two arms in the circuit known as the series and shunt arms. The values of inductance L1, L2 and capacitors C1, C2 can be obtained by referring to (1), (2), (3) and (4) where f2 is the upper cut-off frequency and f1 is the lower cut-off frequency and R is the impedance of the filter which is 50 ohms. All band pass-filters [5] are designed band of frequencies so at a time one of the filters will be passing the signal.

$$C_1=\frac{f2-f1}{4\pi Rf1f2} \quad (1)$$

$$L_1=\frac{R}{\pi(f2-f1)} \quad (2)$$

$$C_2=\frac{1}{\pi R(f2-f1)} \quad (3)$$

$$L_2=\frac{R(f2-f1)}{4\pi f1f2} \quad (4)$$

C. ADC Architecture

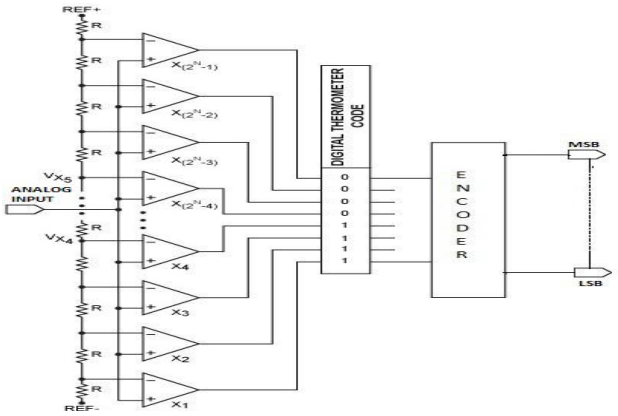

Fig. 3: Flash ADC Architecture

The four different types of ADC architectures are Pipelined ADC, Oversampled ADC, Successive Approximation ADC and Flash ADC. In this project Flash ADC[6] is used to convert analog signal to the digital signal Flash or parallel converters are the high speed ADC's and they utilize one comparator per quantization level (2^N-1) and 2^N resistors. The reference voltage is divided into 2^N values and each of which is fed into a comparator. The input voltage is compared with each reference value and results in a thermometer code at the output of the comparators. A thermometer code will exhibit all zeros for each resistor level if the value of input voltage is less than the value of the resistor string and one if greater than or equal. Flash converters have been limited to 8 bit resolution [7] using CMOS technology. The speed is limited by the switching of comparators and the digital logic.

D. Comparators

Comparators are implemented using differential amplifiers to compare differential voltages. Differential pair has been implemented by matching the transistors M1 and M2 as shown in Fig.4. The transistors M3 and M4 is a load which is made using PMOS based current mirror, since it has current mirror the size of transistors M3 and M4 should be same. The transistor M5 acts as a current sink, M6 and M7 are output transistors.

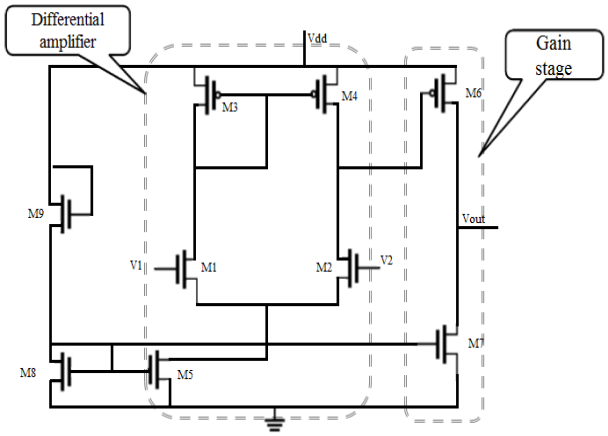

Fig. 4: Schematic of Comparator.

E. Thermometer to Binary code conversion

Table I. Thermometer to Binary code conversion

Thermometer Code															Gray Code				Binary Code			
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0	1	0
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0	0	1	1
0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	1	0	0	1	0	0
0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	1	1	0	1	0	1
0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	0	0	0	1	1	1
0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	1	0	0	0
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	0	1
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0
0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	1
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	1	0	0
0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	0
1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1	1	1	1

The Encoder converts thermometer codes to binary code are given by the equations (5), (6), (7) and (8).

$$G_3 = T_8 \quad (5)$$

$$G_2 = T_4 \overline{T}_{12} \quad (6)$$

$$G_1 = T_2 \overline{T}_5 + T_{10} \overline{T}_{14} \quad (7)$$

$$G_0 = T_1 \overline{T}_3 + T_5 \overline{T}_7 + T_9 \overline{T}_{11} + T_{13} \overline{T}_{15} \quad (8)$$

III. CADENCE IMPLEMENTATION

In Cadence we can have the possibility of placing both analog and digital circuits on the same chip so as to make packaging of CMOS technology attractive.

The HFB ADC consists of 4 filter banks working for different passband frequencies. Four different filters are designed for frequencies 100 KHz- 200 KHz, 300 KHz-400 KHz, 500 KHz-600 KHz and 700 KHz-800 KHz by referring to (1), (2), (3) and (4).

A. Filter with passband 100 KHz to 200 KHz

Design values are C1=7.96nF, C2=63.66nF, L1=159.15uH, L2=19.89uH

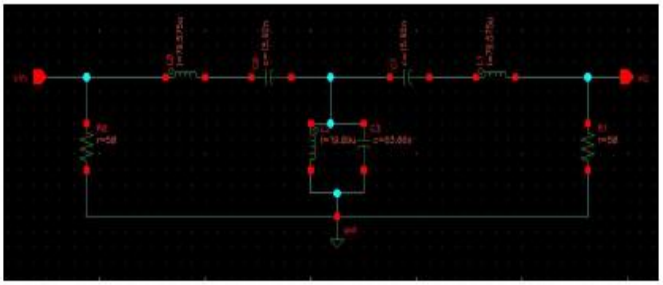

Fig. 5:Schematic of 100 KHz to 200 KHz band pass filter

B. Filter with passband 300 KHz to 400 KHz

Design values are C1=1.326nF, C2=63.66nF, L1=159.15uH, L2=3.316uH

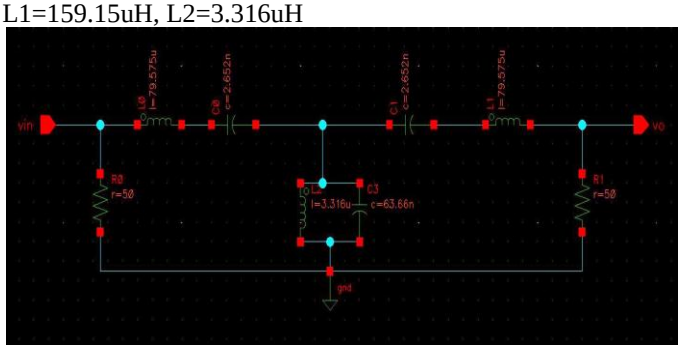

Fig. 6:Schematic of 300 KHz to 400 KHz band pass filter

C. Filter with passband 500 KHz to 600 KHz

Design values are C1=0.5305nF, C2=63.66nF, L1=159.15uH, L2=1.32uH

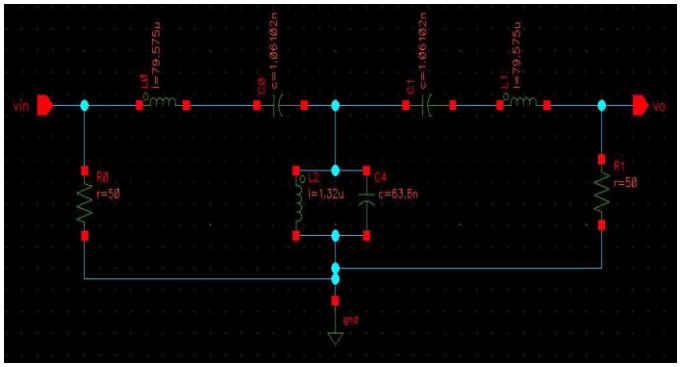

Fig. 7: Schematic of 500 KHz to 600 KHz band pass filter

D. Filter with passband 700 KHz to 800 KHz

Design values are C1=0.2842nF, C2=63.66nF, L1=159.15uH, L2=0.71051uH

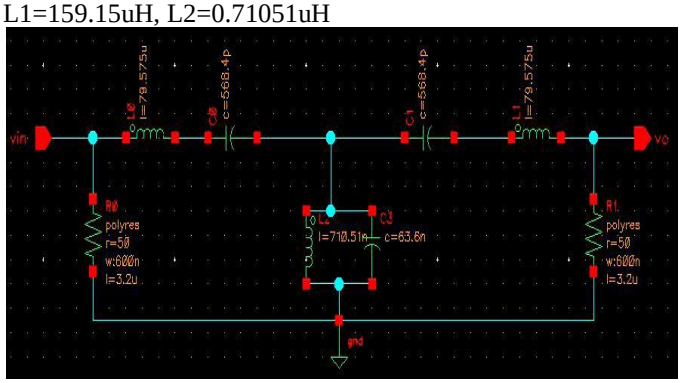

Fig. 8: Schematic of 700 KHz to 800 KHz band pass filter

E. Schematic of Sample and Hold

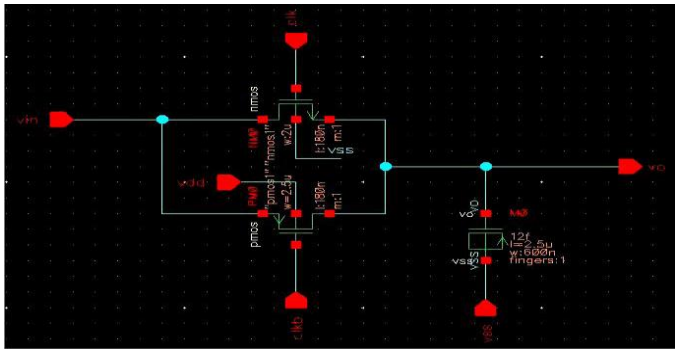

Fig. 9: Schematic of Sample and hold

Sample and hold circuit is used to sample an analog input signal and hold the value over a certain period of time.

F. Schematic of Comparator

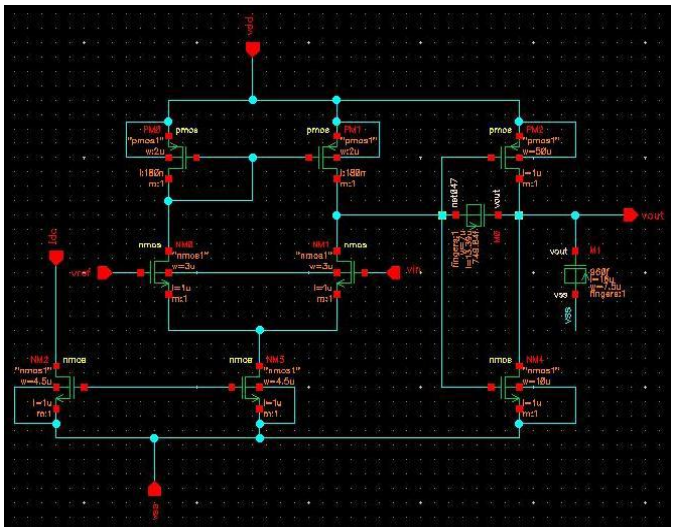

Fig. 10: Schematic of Comparator

G. Schematic of Encoder

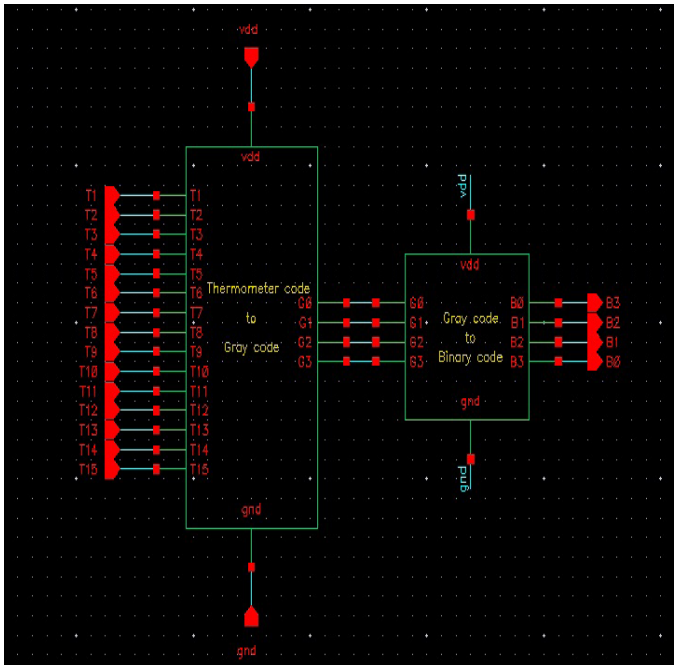

Fig. 11: Schematic of Encoder

H. Schematic of Flash ADC

Resistor string, 15 comparator stages and 15:4 encoder are cascaded to form 4 bit Flash ADC.

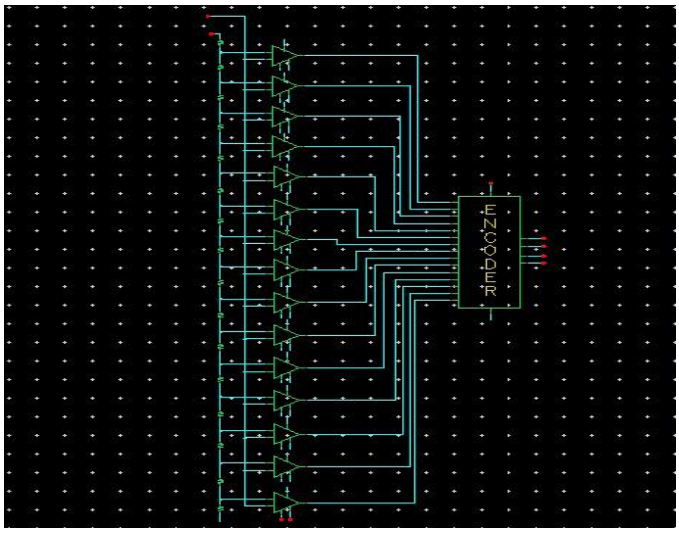

Fig. 12: Schematic of Flash ADC

I. Schematic of first two stages of HFB ADC

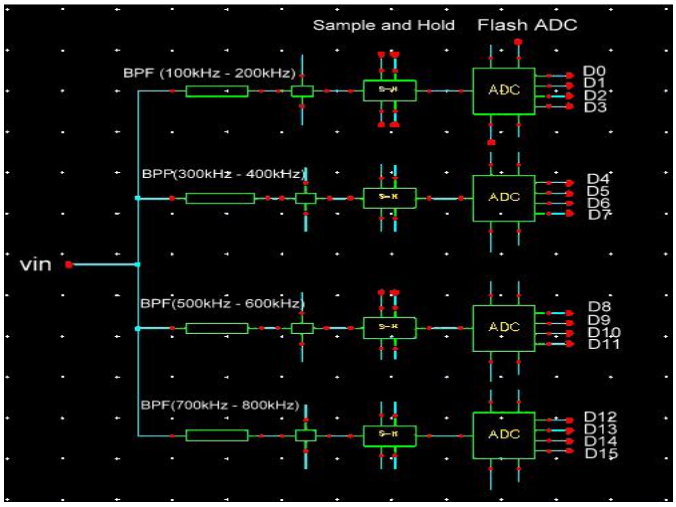

Fig. 13: Schematic of first two stages of HFB ADC

The first two stages of the HFB ADC are implemented and the results are plotted.

IV. RESULTS

The transient response of the sample and hold for the test specification in Table II is observed in Fig.14.

TABLEII. Test specification for Sample and Hold

Input	Voltage 1	Voltage 2	Period	Pulse width
clk pulse	1.8 V	- 1.8 V	250ns	125ns
clkb pulse	-1.8	1.8 V	250 ns	125ns
Vss		-1.8 V		
Vdd		1.8 V		

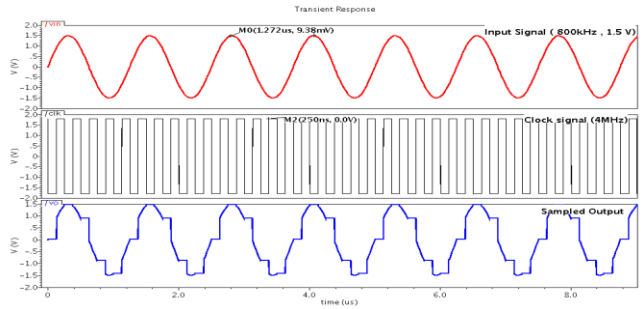

Fig. 14: Transient response of Sample and hold

The transient response of the comparator for the test specification in Table III is observed in Fig.15.

TABLE III. Test Specification for Comparator

Input	Instance	
Vin	Vsin	1V, 100KHz
Vref	Vdc	500mv
Vdd	1.8 V	
Vss	- 1.8 V	
Idc	30u A	

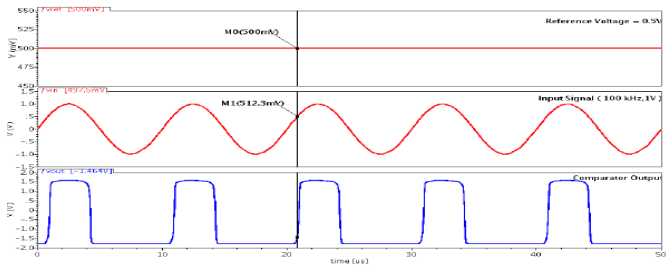

Fig. 15: Transient response of Comparator

The transient response of the comparator is observed for the input frequency of 100 KHz and this result can be used to design the 15 comparators. Minimum voltage range is 62.5mV.

The transient response of the Encoder is observed in Fig.16.

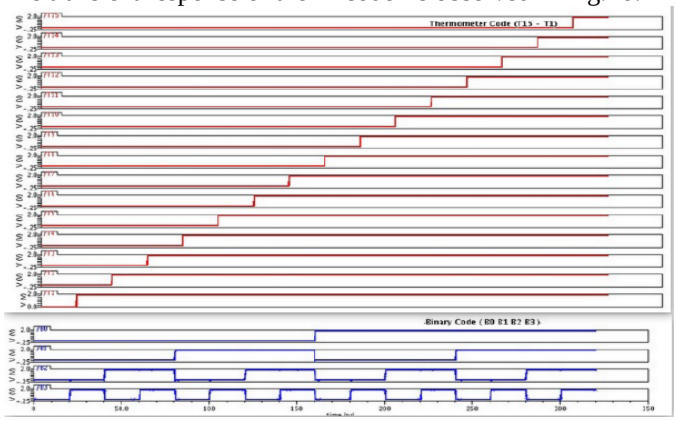

Fig.16: Transient response of Encoder

The transient response of the Encoder is used to test the Encoder circuit and to verify the Thermometer to Binary code conversion.

The transient response of the Flash ADC for the test specification in table IV is observed in Fig.17.

TABLE IV. Test Specification for Flash ADC

Input	Instance	
Vin	Vsin	1.5 V, 100 KHz
Vref	Vdc	1.1 V
Vdd	1.8 V	
Vss	- 1.8 V	
Idc	30u A	

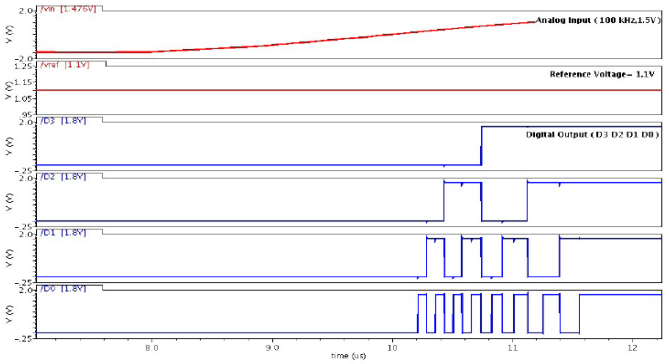

Fig. 17: Transient response of Flash ADC

The Transient responses of HFB ADC are verified for frequencies 175 KHz and 740 KHz present in different frequency bands.

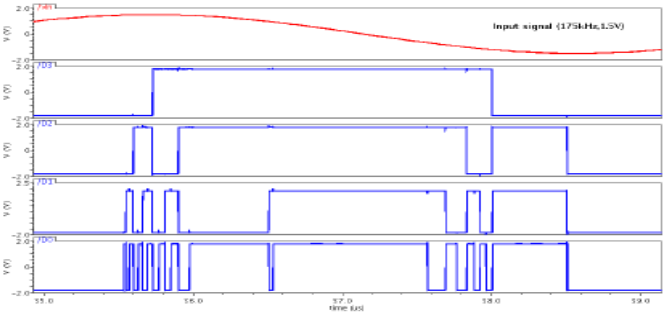

Fig. 18: Digital outputs for input signal of 175 KHz

The transient response is the input to output response for the given specifications of inputs.

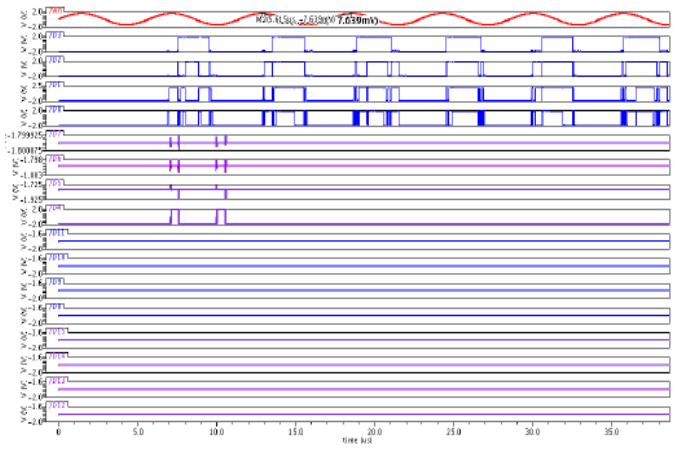

Fig. 19: Transient response for input signal frequency of 175 KHz

For input signal of frequency 740 KHz, transient response is observed in Fig. 20.

Transient response is observed for highest four bit outputs as it passes through filter bank of 700 KHz to 800K Hz.

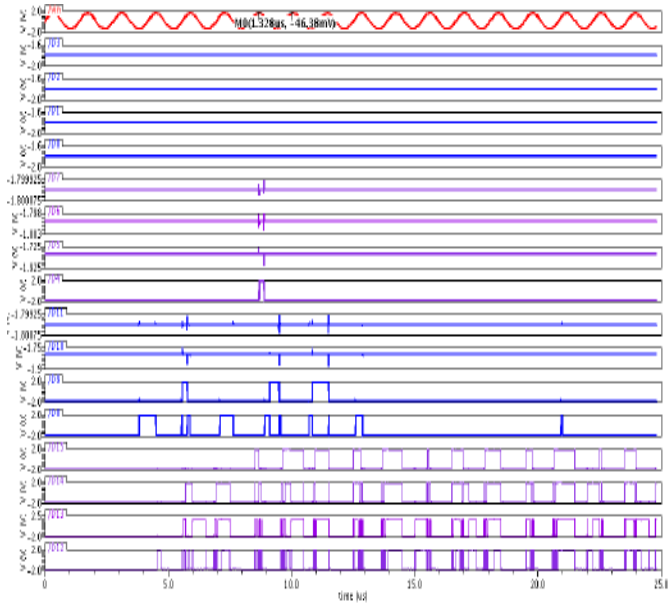

Fig. 20: Transient response for input signal frequency of 740 KHz

The Layouts are generated for each of the circuits and Design Rule Check(DRC), Layout Versus Schematic (LVS)[8] checks are done and can be used for implementation.The creation of the mask layout is one of the most important steps in the full-custom (bottom-up)design flow, where the designer describes the detailed geometry and the relative positioning of eachmask layer to be used in actual fabrication, using a Layout Editor. Physical layout design is verytightly linked to overall circuit performance since the physicalstructure determines the transconductancesof the transistors,the parasitic capacitances andresistances, and obviously, the silicon area that is used to realize a certain function.
Virtuoso is the main layout editor of Cadence design tools. Commonly used functions can be accessed. There is an information line at the top of the window. This information line, (from left to right) contains the Xand Y coordinates of the cursor, number of selected objects, the traveled distance in X and Y, thetotal distance and the command currently in use. This information can be very handy while editing.At the bottom of the window, another line shows what function the mouse buttons have at any given moment.

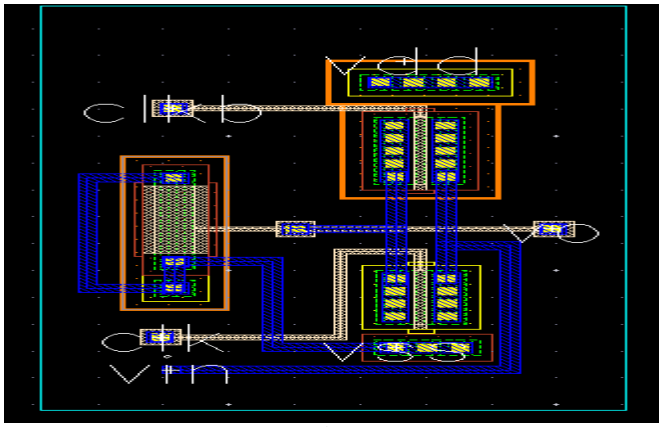

Fig 21: Layout of Sample and Hold

The layout of sample and hold consists of designing pmos and nmos transistors along with the clk and clkb pins with Vss and Vdd.

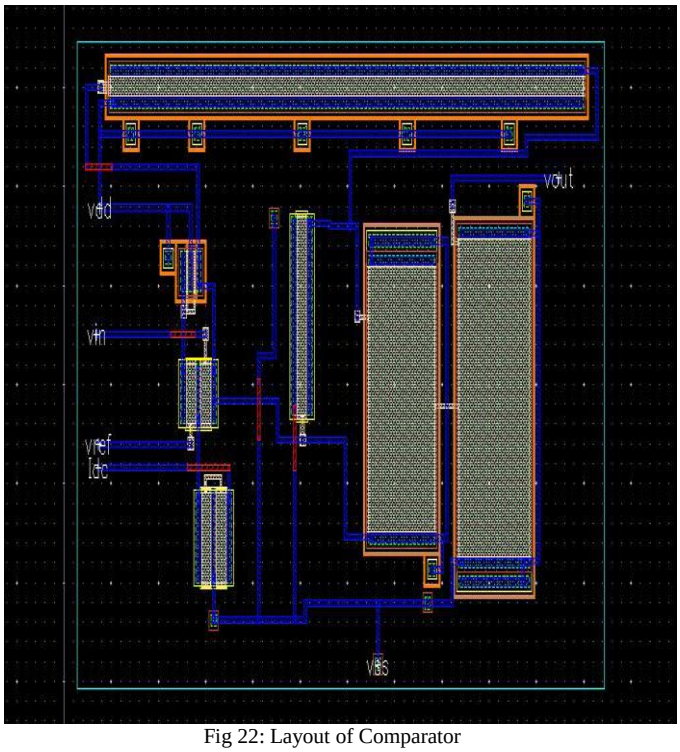

Fig 22: Layout of Comparator

The layout for comparator consists of current mirror circuit along with current sinks and output transistors. The width of output transistors nmos and pmos are 10um and 50um respectively.

Fig. 23: Layout of thermometer to gray code converter.

The layout for thermometer to gray code converter consists of 15 inputs and 4 outputs. The layouts for AND, NOT and NAND gates are implemented and connected according to equations (5), (6), (7) and (8).

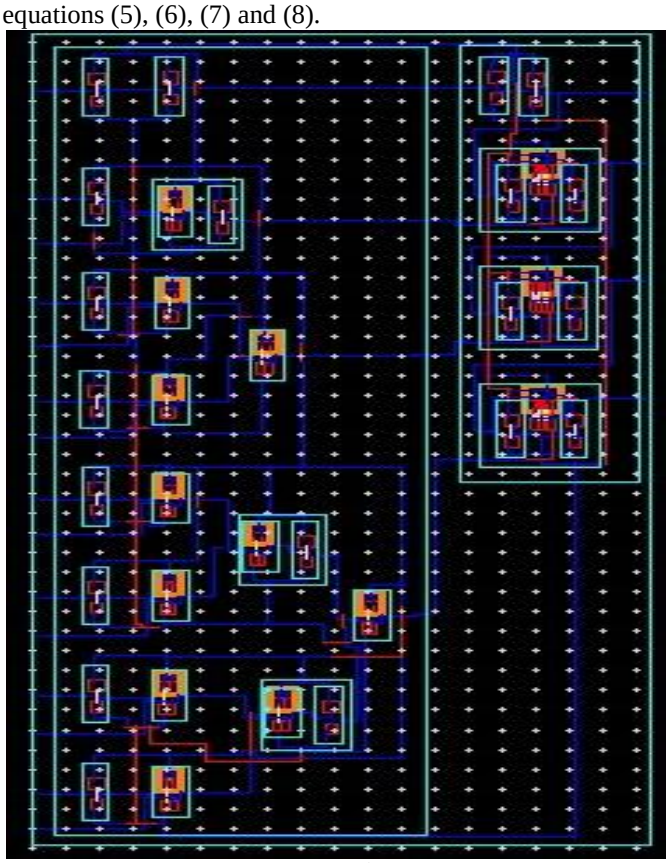

Fig. 24: Layout of Encoder.

The layouts of Thermometer to gray code converter and gray to binary converter are cascaded to implement the layout of Encoder consisting of 15 inputs and 4 outputs.

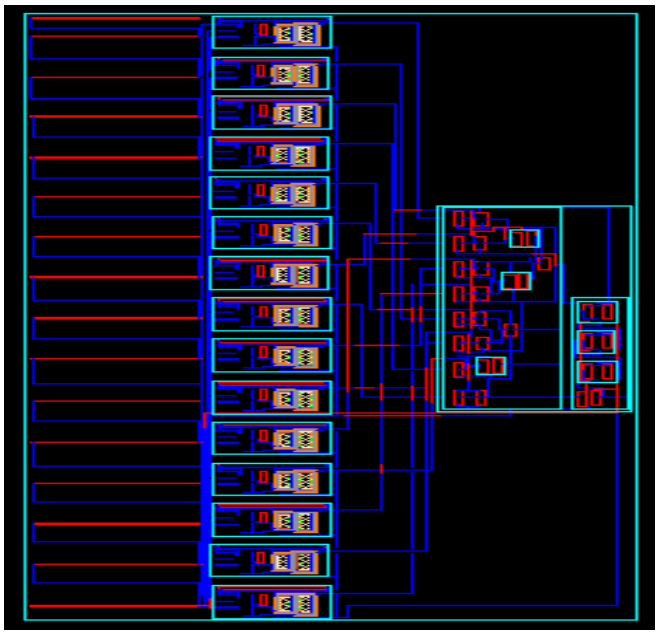

Fig 25: Layout of Flash ADC.

The layout of the flash ADC is implemented by cascading layouts of comparators and encoder. 15 comparators and an encoder are cascaded to form Flash ADC.

V. CONCLUSION

The ADC was designed for the frequency 100 KHz to 800 KHz with a band-width of 100 KHz. Signal to noise ratio of 25.84 dB was obtained for 4 bits with a response time for the Flash ADC being 100ns. The area of the layout for ADC was found to be 1748 um^2. To improve the accuracy of the data, Design of the quantizer with higher resolution can be used. Layouts are generated at transistor level and can be integrated to meet the required design specifications.

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