

Design and Implementation of High Speed Carry Select Adder

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Abstract—In electronic adder is a digital circuit that performs addition of numbers. Adders can be constructed for many numerical representations such as arithmetic and logical operation. The most adders operates on binary numbers. Among the different types of adders, carry select adder is a one of the fastest adder. The gate level modification is to reduce the power and area of carry select adder by using the concept of Arithmetic Logic Unit (ALU). In this paper, different techniques such as Binary To Excess Converter (BEC), Common Boolean Logic (CBL) are implemented in Carry Select Adder (CSLA). On comparing these techniques, the result analysis shows that proposed ALU is consumes less power and area than conventional CSLA.

Keywords— Adder, Carry select adder (CSLA), Arithmetic Logic Unit (ALU), Common Boolean Logic (CBL).

I. INTRODUCTION

Power consumption is an important efficiency factor in designing very large scale integrated (VLSI) circuit. Moreover with the explosive growth of VLSI technology the demand and popularity of portable devices has driving designers to strive for smaller silicon area. The central electronic circuit used for addition is adder.

Adders are fundamental for wide variety of digital system. Many adders exist but the fast adding with Low area and Power still challenging. There are different types of adders such as Ripple carry adder (RCA), carry skip adder (CSKA), carry look ahead adder (CLA), carry save adder (CSLA), etc. among them RCA shows compact design but their computation time is longer. It has lowest speed amongst all adder because it has large propagation delay but occupy less area. Then, in CLA can derive fast result but it leads to increase in area, among these adders CSLA have small area but delay is increased due to ripple carry adder.

We have designed an efficient logic design for CSLA. The brief is structured as follow. Section II(a),(b),(c) deals with structure and details of Carry Select Adder (CSLA), Binary To Excess Converter (BEC), Common Boolean Logic (CBL). Section III presents the detailed structure and design of Arithmetic Logic Unit (ALU). Simulation tool is explained in section IV. Simulation Result is explained in section V. Finally, the work is concluded in section VI.

II. IMPLEMENTATION IN CARRY SELECT ADDER

A. carry select adder (csla)

CSLA use multiple narrow adders to create fast wide adders. A CSLA breaks the addition problem into smaller groups. It is one of the fast type of adder. The adder consists of two independent units. Each unit implements the addition operation in parallel. One way to speed up the addition into several smaller groups, with each having N-bit, say 8-bit groups and then for each group four additions are performed in parallel, one assume carry in is '0' (CIN=0) and the other assuming the carry in is '1' (CIN=1). when the carry in is eventually known the correct sum is simply selected through a N-bit using 2-to-1 mux. The adder based on this approach is known as carry select adder (CSLA). The application CSLA is used in data processing processor to perform fast arithmetic function.

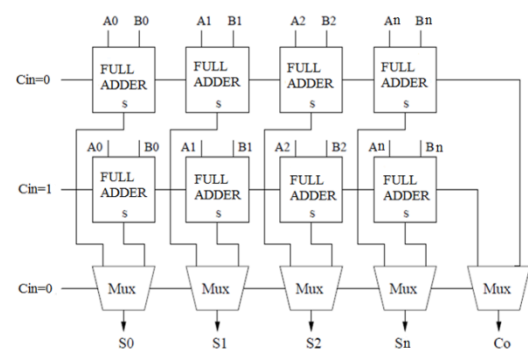


Fig:1 carry select adder

The gate count of 4-bit CSLA is,

$$\text{Gate Count} = 136(\text{FA} + \text{MUX})$$

$$\text{Full adder} = 104(13 \times 8)$$

$$\text{Mux} = 32(4 \times 8)$$

The carry-select adder generally consists of two ripple carry adders and a multiplexer. Adding two n-bit numbers with a carry-select adder is done with two adders (therefore two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one. After the two results are calculated, the correct sum, as well as the correct carry, is then selected with the multiplexer once the correct carry is known. The number of bits in each carry select block can be uniform, or variable. When variable, the block size should

have a delay, from addition inputs A and B to the carry out, equal to that of the multiplexer chain leading into it, so that the carry out is calculated just in time. The delay is derived from uniform sizing, where the ideal number of full-adder elements per block is equal to the square root of the number of bits being added, since that will yield an equal number of MUX delays..

B. BEC based csla

In this csla, the RCA which assume carry in is '1' is replaced using the BEC (BINARY TO EXCESS-1 CONVERTOR).In this the every full adder cell in RCA is wait for every carry in then the carry out is generated. Then to get linear dependency is to anticipate both possible values of carry in and evaluate the result for both possibilities in advance. Once the correct value of carry in is known the correct value is selected using multiplexer.

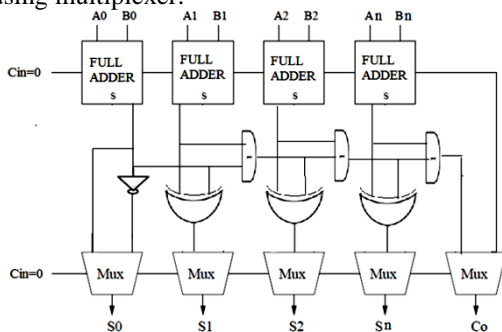


Fig:2 Binary-to-excess-1 convertor

The gate count of 4- bit BEC is ,

GATECOUNT=92 (FA+MUX+NOT+OR)

- FA=52(13*4)
- MUX=32(8*4)
- NOT=4(4*1)
- OR=4(1*4)

Instead of the RCA with cin 1 in order to reduce the area and power consumption of the regular CSLA. To replace the 3-bit RCA, an 4-bit BEC is required. A structure and the function table of a 4-b BEC are shown in Fig and the basic function of the CSLA is obtained by using the 4-bit BEC together with the mux. One input of the 8:4 mux gets as it input (B3, B2, B1, and B0) and another input of the mux is the BEC output. This produces the two possible partial results in parallel and the mux is used to select either the BEC output or the direct inputs according to the control signal Cin. The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed.

C. CBL BASED CSLA

Boolean Logic was introduced in by George Boole in his first book The Mathematical Analysis of Logic (1847), and set forth more fully in his An Investigation Of Laws Thought (1854). According to Huntington the term "Boolean Logic" was first suggested by Sheffer in 1913. Boolean Logic has been fundamental in the development of digital electronics, and is provided for in all modern programming languages.

In mathematics and mathematical logic, Boolean logic is the sub area of algebra in which the values of the variables in the truth table is as true and false, usually denoted as 1 and 0 respectively. Instead of elementary algebra where the values of the variables are numbers, and the important operations are addition and multiplication, the important operations of Boolean logic are the conjunction and, denoted \wedge , the disjunction or, denoted \vee , and the negation not, denoted \neg . It is thus a formalism for describing logical relations in the same way that ordinary Logic describes numeric relations.

To share the common Boolean logic term, we only need to implement one XOR gate with one INV gate to generate the summation signal pair. As the carry-in signal is ready, we can select the correct summation output according to the logic state of carry-in signal. As for the carry propagation path, we construct one OR gate and one AND gate to anticipate possible carry input values in advance.

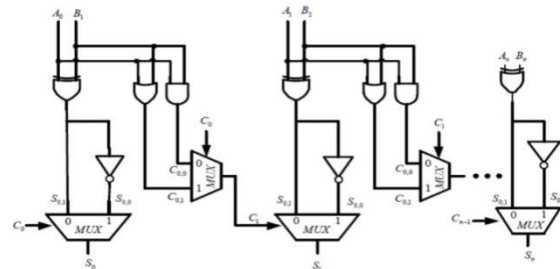


Fig:3 common boolean logic

The gate count of 4- bit CBL is ,

GATECOUNT=88(FA+MUX+AND+NOT+EXOR)

- FA=52(13*4)
- MUX=20(5*4)
- AND=3(3*1)
- NOT=1(1*1)
- EXOR=12(3*4)

Once the carry-in signal is ready, we can select the correct carry-out output according to the logic state of carry-in signal. In this way, we can keep both the summation generation circuit of XOR gate and INV gate and the carry-out generation circuit of OR gate and AND gate in parallel.

III. PROPOSED CSLA

In this proposed adder we implementing the Csla in arithmetic and logic unit (ALU), the John von Neumann proposed the ALU concept. An ALU is a digital circuit that performs arithmetic and logic operation like addition, subtraction so on... ALU is building block of CPU. In digital electronics an ALU is a combinational circuit that performs arithmetic and bitwise logical operation on integer binary number. Many of the operation that we want to perform on group bits can be broken down into repeated operation on individual bits.

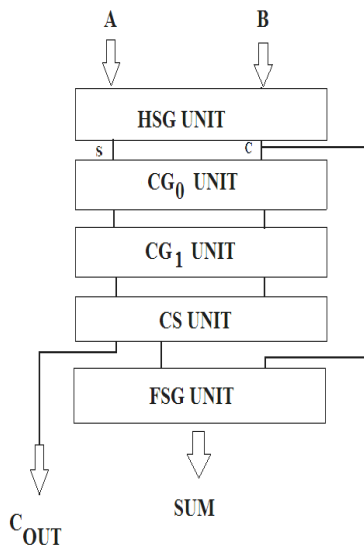


Fig:4 Arithmetic and logic unit

The gate used in the proposed CSLA are:

- The AND and EX-OR gate are used as Half Sum Generator (HSG).
- The OR and AND gate are used as Carry Generator (CG) and also in Carry Selector (CS).
- Then EX-OR is used as Full Sum Generator (FSG).

In this ALU consists of half sum generator (HSG), carry generator for $C_{in}=0$ (CG0), carry generator for $C_{in}=1$ (CG1), carry selector (CS) and full sum generator (FSG). The gate count of 4-bit ALU is ,

$$\text{GATE COUNT} = 60 (\text{EXOR} + \text{AND} + \text{OR})$$

$$\text{EXOR} = 8 (8 * 2)$$

$$\text{AND} = 16 (16 * 1)$$

$$\text{OR} = 12 (12 * 1)$$

The proposed CSLA consists of is an HALF ADDER (HSG), which generate the sum (s0) and carry (C0). Then the C0 and S0 are passed through the carry generators, which one

assume carry in as '0' (CG0) and another assume carry in as '1' (CG1). The carry is selected by using carry selector (CS) with help of C_{in} . The full sum (FSG) is generator using the carry out (Cout) and half adder (S0).

ALGORITHM TO DESIGN ALU

1. Select the required operation to be performed by ALU.
2. At first required to built 1-bit ALU based on the concept "DIVIDE AND CONQUER".
3. The n-bit ALU can be sliced into n-equal part. This is called as "BIT SLICED METHOD".
4. In this bit slice approach, ALU is divided into arithmetic unit and logic unit.

IV. SIMULATION TOOL

Microwind is a Simulation tool to design the IC in physical description level. In microwind, the IC is constructed using stick diagram. Stick diagram is useful to convey the layer information through the use of a colour code. Stick diagram provide a top view of pattern. The colour code allows to trace the signal flow.

The above adder topologies are simulated using Microwind and DSCH. Functional testing and timing analysis were carried out for the entire adder module used in the work. The microwind software is dedicated to the training in sub micron CMOS VLSI design, consisting in a layout editor, electrical circuit and a fast online analog simulator. The technology library used in this work is CMOS 6-metal layers 0.12 μm technology, consequently λ is 0.06 μm (60nm).

The microwind simulation provides two environments like logic editor and simulator. They are DSCH and Microwind used to validate logic design simulation with delay analysis and physical circuit extraction. All the adders used in this work are simulated using schematic entry and its corresponding test patterns are generated and its functionally is verified. After verification the schematic file is converted to VERILOG file. Secondly using Microwind environment, VERILOG file is imported using the command "COMPILE VERILOG FILE", so that the schematic of the logic design will be converted into physical layout.

The physical mask layout of any circuit to be manufactured using a particular process have a conform to a set of geometric constraints or rules, which are called layout design rules.

The main objective of design rules is to achieve a high overall yield and reliability while using the smallest possible silicon area, for any circuit to be manufactured with a particular process. The layout window features in grid, scaled in λ

Lambda design rule is used to construct the pattern using stick diagram in microwind . Lambda unit is fixed to nearly equal parts of the smallest amount available for lithography of the technology. It is based on the reference metric ' λ ' that as unit.

Value= $m\lambda$, Where m-scaling multiples.

V.SIMULATION RESULT

The design of proposed CSLA is successfully tested and synthesized by using MICROWIND 2 AND DSCH. Microwind is a tool for designing and simulating circuits at the layout level. So, microwind is used as simulation tool in this paper to finding the performance of proposed CSLA. The simulation result is tabulated. The simulation result table is in terms of delay, area and power. The area indicates the total cell area design and the total power is the sum of leakage power, internal power and switching power.

Bit size	Adder	Gate count	Power (mW)
4-BIT	CSLA	136	0.867
	BEC	94	0.417
	CBL	88	0.388
	PROPOSED CSLA(ALU)	60	0.147
8-BIT	CSLA	272	3.114
	BEC	188	2.892
	CBL	176	1.177
	PROPOSED CSLA(ALU)	120	0.797

Table:1 Simulation result in terms of AREA and POWER.

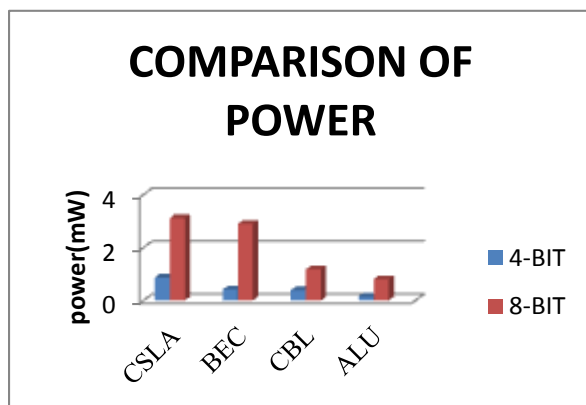


Fig:5 comparison of 8-bit and 4-bit power

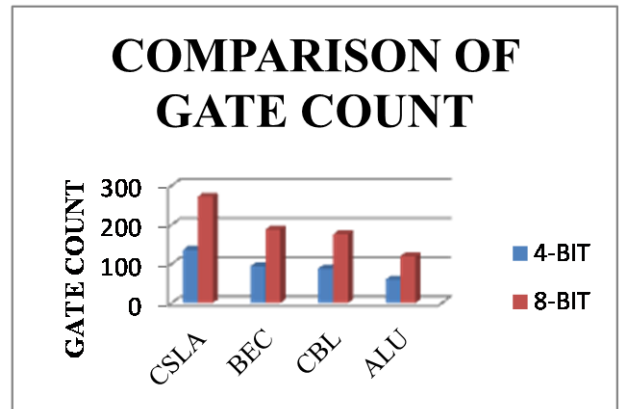


Fig: 6 comparison of 8-bit and 4-bit gate count

VI . CONCLUSION

An efficient approach is planned in this paper to reduce the area and power of CSLA architecture. The reduced number of gates offers great advantage in the reduction of area and power. The compared result shows that the proposed CSLA has a low power and area consumption. The modified proposed CSLA architecture is having low area , low power and efficient for VLSI hardware implementation.

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