Design and Implementation of Programmable Sine Wave Generator for Wireless Applications using PSK/FSK Modulation Technique

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Abstract

With the introduction of digital systems we find ourselves in the time of ever increasing demand for high data rates and optimum bandwidth usage. FSK (Frequency Shift Keying) and PSK (Passé Shift Keying) are the methods used for digital transmission of data. There are several methods we found to implement but Direct Digital Synthesis (DDS) is a method of producing an analog wave form usually a sine wave by generating a time-varying signal in digital form and then performing a digital-to-analog conversion. As we know the operations within a DDS device are digital, it can gives fast switching between output frequencies, fine frequency resolution and Operate in a large range of spectrum frequencies. Now a day's DDS devices are very compact and draw little power due to advances in design and process technology. Here we design and implement the DDS architecture for less area, power and timing by using cadence tool.

1. Introduction

Generally there are three parts to a communications system as the information to be transmitted, medium and the carrier. The information generated from different sources may be analog or digital, but in the modern scenario most of the devices are digital due to low cost, low power, less complexity. So the input analog signal is converted to digital signal by means of sampling and quantization. In wireless communication scenario the medium are analog in nature, so the information is to be transmitted through an analog carrier generally sine wave by means of some modulation technique [1].

Direct digital synthesis (DDS) is a method of producing an analog waveform usually a sine wave by generating a time-varying signal in digital form and then performing a digital-to-analog conversion. Generally the operations within a DDS device are digital, so it can provides fast switching between output frequencies, fine frequency resolution and operate in a large range of frequencies [2], [3].

Applications are currently using DDS based waveform generation fall into two principal categories: Designers of communications systems requiring agile (i.e., immediately responding) frequency sources with excellent phase noise and low spurious performance often choose DDS for its combination of spectral performance and frequency-tuning resolution. DDS can also be used as a reference for a PLL to enhance the overall frequency, as a local oscillator (LO), or even for direct RF transmission. DDS can also be applicable for industrial and biomedical application for generating a sine wave. Since DDS is digitally programmable, so the phase and frequency of a waveform can be easily adjusted. DDS permits simple adjustments of frequency in real time to locate resonant frequencies or compensate for temperature drift [4].

The rest of the paper is outlined as follows. In section 2, we define the modulation technique. Then in section 3, explain about the DDS operation. In section 4 and 5, describes the DDS architecture and the design of NCO. In section 6, the design, simulation and analysis of the sine wave generator are demonstrated. Finally in section 7, describes concluding of this paper.

2. Modulation Technique

Modulation is the process of mapping of information signal with the carrier signal and then be transmitted through the channel. Amplitude-Shift Keying (ASK), Frequency-Shift Keying (FSK) and Phase-Shift Keying (PSK) are the modulation technique used for the mapping of information signal to be transmitted [1].

In ASK, the amplitude of the carrier is changed in response to information and all else is kept fixed. Bit 1 is transmitted by particular amplitude and bit 0 is

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transmitted by other particular amplitude at a constant frequency.

$$ASK(t) = s(t).\sin(2\pi ft) \quad (1)$$

In FSK, we change the frequency in response to information, one particular frequency for bit 1 and another frequency for bit 0 as shown below for the same bit sequence as above.

$$PSK(t) = \begin{cases} \sin(2\pi f_1 t) & \text{for bit 1} \\ \sin(2\pi f_2 t) & \text{for bit 0} \end{cases} \quad (2)$$

In PSK, it uses finite number of phases to transmitting the binary bits. Here bit 1 is transmitted for 0 phase and bit 0 is transmitted for 180 degree phase shift. Phase shift represents the change in the state of the information in this case.

$$PSK(t) = \begin{cases} \sin(2\pi ft) & \text{for bit 1} \\ \sin(2\pi ft+\pi) & \text{for bit 0} \end{cases} \quad (3)$$

3. Direct Digital Synthesis (DDS)

DDS technique is rapidly gaining acceptance for solving frequency (or waveform) generation requirements in both communications and industrial applications because single-chip IC devices can generate programmable analog output waveforms simply and with high resolution and accuracy. Figure 1 show the signal flow through DDS architecture. A DDS produces a sine wave at a given frequency. Generally the frequency depends upon two variables, such as the reference-clock frequency and the binary number that is programmed into the frequency register (tuning word) [5].

For FSK, the data can be transmitted by shifting the frequency of a continuous carrier to one of two discrete frequencies. The frequency tuning word of DDS represents the output frequencies, which may be

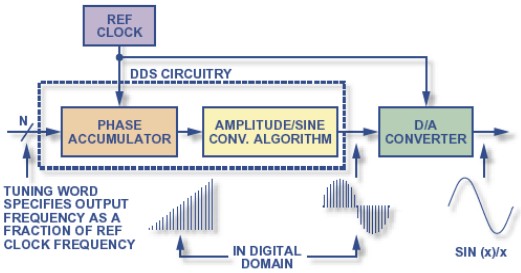

Figure1. Signal flow through a DDS Architecture [5]

generate an appropriate value of f_0 and f_1 as they occur in the pattern of 0's and 1's to be transmitted. Before transmitting to the device the user must program two tuning word. A dedicated pin on the device (FSELECT) accepts the modulating signal and selects the appropriate tuning word (or frequency register). Figure 2 show the DDS based FSK encoder.

PSK encoding is easily implemented with DDS Integrated Circuits. In most of the devices the phase value can be loaded with a phase register and this value is directly added to the phase of the carrier without changing its frequency. Hence for generating a PSK output signal we can change the phase of the carrier by changing the contained of the register module.

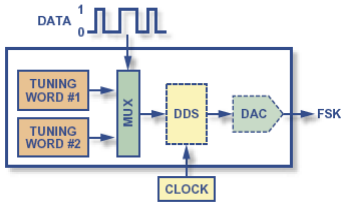

Figure 2 DDS based FSK Encoder [5]

The binary number in the frequency register provides the main input to the phase accumulator. If a sine look up table was used, the phase accumulator computes the phase (angle) address for the look up table, which outputs is the digital value of amplitude corresponding to the sine of that phase angle to the DAC and the DAC converts that number to a corresponding value of analog voltage or current. To generate the fixed-frequency sine wave, a constant value (the phase increment which is determined by the binary number) is added to the phase accumulator with each clock cycle. The phase accumulator continuously goes through the sine look-up table for a phase increment and if the phase increment is large, it generates a high frequency sine wave. For a small phase increment, the phase accumulator will take

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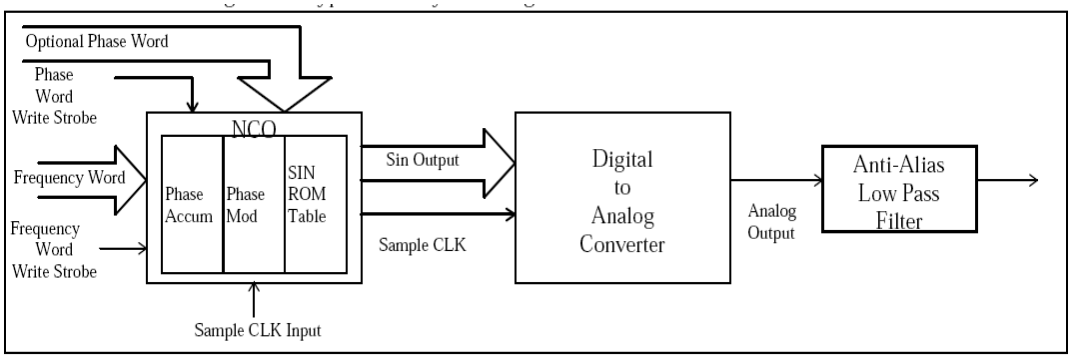

Figure 3. Architecture for DDS System

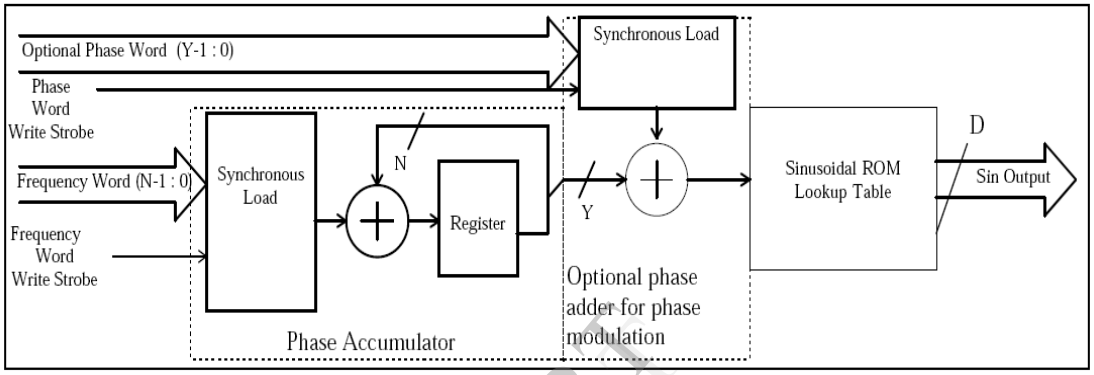

Figure 4. Architecture for NCO Design

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many more steps to generate a bit slower waveform. The phase accumulator is actually a modulo-M counter which increments its stored number each time it receives a clock pulse. So the magnitude of the increment is determined by the binary-coded input word (M) [5], [6].

4. DDS Architecture

A DDS system simply takes a constant reference clock input and divides it down a to a specified output frequency digitally quantized or sampled at the reference clock frequency. So this type of frequency control makes DDS ideal for systems that require precise frequency sweeps [7].

A basic DDS system consists of a numerically controlled oscillator (NCO) used to generate the output carrier wave, and the digital sinusoidal word from the NCO can be converted into a sampled analog carrier with the help of digital to analog converter (DAC). Since the DAC output is sampled at the reference clock frequency, a low pass filter is typically used to eliminate alias components. Figure 3 is the basic architecture of DDS system.

5. Architecture for NCO Design

The generation of the output carrier from the reference sample clock input is performed by the NCO, so the basic components of the NCO are a phase accumulator and a sinusoidal ROM lookup table and an optional phase modulator can also be including in the NCO design. Here the phase modulator will add phase offset to the output of the phase accumulator just before the ROM lookup table, which will enhance the DDS system design by adding the capabilities to phase modulate the carrier output of the NCO. Figure 4 is the block diagram of a typical NCO design.

Components that are required to design a NCO are specified below:

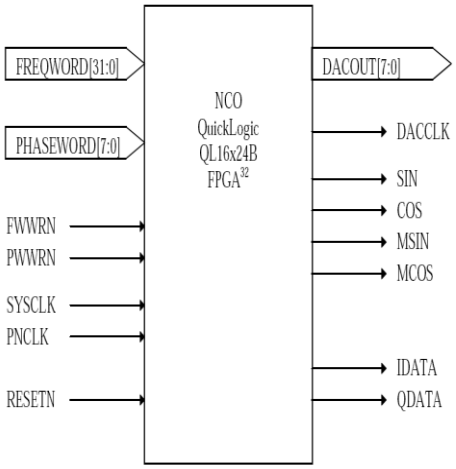

Figure 5 External IO Interface to the Proposed NCO Design

Table 1.Signal Function Table

FREQWORD [31:0]	This input is the frequency control word to the NCO. This word controls the phase accumulator rate and the output frequency of the DACOUT. F_{out}= FREQWORD[31:0]*(SYSCLK/2^{32})Hz
PHASE WORD [7:0]	This input is the phase modulation control word to the NCO. This word control the phase offset of the phase accumulator. Pout= PHASEWORD[7:0]*($2\pi/2^8$)radians
FWWRN	This input is the low asserted frequency word write strobe. This strobe is the input to the FREQWORD on the rising edge. This strobe can be asynchronous to the SYSCLK.
PWWRN	This input is the low asserted phase word write strobe. This strobe is the input to the PHASEWORD on the rising edge. This strobe can be asynchronous to the SYSCLK.
SYSCLK	This is the reference system clock input to the NCO. This clock also the sampling clock of the output carrier.
PNCLK	This input is the pseudo-noise generator clock input. This clock sets the data rate of the I & Q data outputs.
RESETN	This input is a low asserted global reset. When asserted, the internal phase and frequency word registers are clear stopping the output carrier at 0 radians.
DACOUT[7:0]	This output is the sinusoidal DAC amplitude word. This word is valid on the rising edge of the DACCLK. This sinusoidal wave form output is represented by the following: f(t)=sin(2 π F_{out}(t)÷ Pout)
DACCLK	This clock is the SYSCLK feedback to an output pin compensating for the latency of the NCO IO pins. The DACOUT amplitude words will be valid on the rising edge of the DACCLK.
SIN	This sine wave outputs comes from the MSB of the phase accumulator. The output frequency of this pin is controlled by the frequency word input.
COS	This cosine wave outputs comes from the MSB and the next most significant bits of the phase accumulator. The output frequency of this pin is controlled by the frequency word input.
MSIN	This output is a single bit digital sine wave output. The output frequency of this pin is controlled by the frequency word input and the phase offset by the phase word input. This sine wave output is same as the SIN output with a phase offset of plus $2\pi/2^8$*PHASEWORD.
MCOS	This output is a single bit digital cosine wave output. The output frequency of this pin is controlled by the frequency word input and the phase offset by the phase word input.
IDATA /QDATA	These outputs are a 2^5-1 pseudo noise random pattern used to demonstrate phase modulation using the phase port.

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5.1. PN Generator

This module is not part of the NCO design but is used to produce a sample random data pattern to modulate the carrier output. Here this module uses the PNCLK input to clock two Gold code 5 bit PN generators. The outputs of the PN generators are IDATA and QDATA outputs.

5.2. Load Frequency Word

The load frequency word block is a synchronizing loading circuit. The FREQWORD [31:0] input drives the data input to the 32 bit fwreg register that is sampled on the rising edge of the FWWRN write strobe. The FWWRN strobe also drives the data input to a met stable flip flop fwwrn that is used in

conjunction with a synchronous register fwwrns to produce a FWWRN rising edge strobe. This rising edge strobe loadp1 is then piped for an additional 3 clock cycles producing the load strobes loadp2, loadp3, and loadp4. The load strobes are used to signal when to update the synchronous pipe line 8 bit sampled frequency word content. The pipe line registers are concatenated to produce the 32 bit synchronous frequency word output SYNCFREQ [31:0] that is staggered to compensate for the 32 bit pipe lined phase adder.

5.3. Phase Word Accumulator

The phase accumulator block is a 32 bit accumulator that is pipe lined in 8 bit sections. This module instantiates a schematic captured carry lock ahead (CLA) adder that has a carry in and carry out port. The CLA adders add the synchronous frequency word with matched with pipeline architecture. So the carry output of the CLA adders is registered in the piped registers with the output tied to the next most significant CLA adder carry input. The most significant sum output register pipe4 is assigned to the PHASE output port giving a phase value quantized to 8 bits. A digital sine and cosine value is also calculated from the pipe4 register and brought out of the chip as SIN and COS.

5.4. Load Phase Word

The load phase word block is a synchronizing loading circuit. The PHASEWORD [7:0] input drives the data input to the 32 bit pwreg register that is sampled on the rising edge of the PWWRN write strobe. The PWWRN strobe also drives the data input to a metastable flip flop pwwrn that is used in conjunction with a synchronous register pwwrns to produce a FWWRN rising edge strobe. This rising edge strobe load is used to signal when to update the synchronous phase word register phswd. The phswd register is assigned to the synchronous phase word output SYNCPHSWD [7:0].

5.5. Phase Modulator

The phase modulator block is used to phase offset the phase accumulator 8 bit quantized output with the synchronous phase word from the load phase word block. This module instantiates a CLA adder with the input tied to the synchronous phase output and the B input tied to the phase accumulator output. The sum output of the adder is registered in the mphsreg register and assigned to the MODPHASE output port.

5.6. Sine Lockup

This module takes the modulated phase value form the phase modulator block and translated the quantized 8 bit value into a sine wave form amplitude value quantized to 8 bits. The translation from phase to amplitude is performed by a sine ROM table that in instantiated in this module. The ROM table is reduced to a ¼ of the symmetrical sine wave form and the MSB of the sine wave form is equivalent to the modulated phase input.

5.7. Sine ROM Table

This ROM table converts the phase word input to a sine amplitude output. Only ¼ of the symmetrical sine wave form is store in the ROM for conserve the area. The sine values stored in this table are the 0 to pi/2 unsigned values quantized to 8 bits. Thus, the ROM table requires a 6 bit phase address input and outputs a 7 bit amplitude output. The sinlup module processes the phase and amplitude values to produce a complete sine period.

6. Design and Simulation Analysis

Here we design and simulate the DDS architecture using cadence tool. we are written a verilog code for DDS and then after we have taken a MUX for FSK, when data is ‘0’ then frequency ‘1’ will be load to frequency word or when data is ‘1’, then frequency ‘2’ will load. For PSK we have taken a constant phase word which changes the phase value by 180 degree. Then the behavioural simulation was verified using, Cadence Simvision and synthesized using Cadence Encounter RTL Compiler. We got slack as 0ps. Finally the Placement and Routing (P&R) were carried out by Cadence Encounter RTL Compiler [8], [9] with 75.429% of density.

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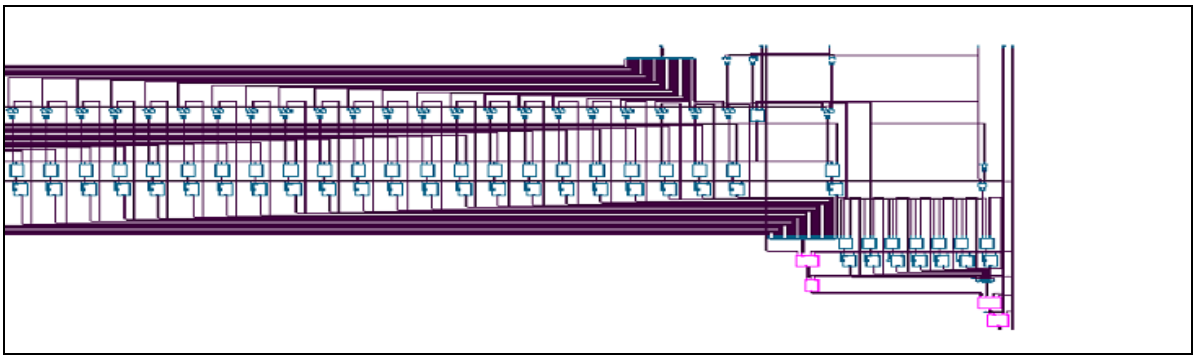

Figure 6 Schematic view of our DDS Architecture

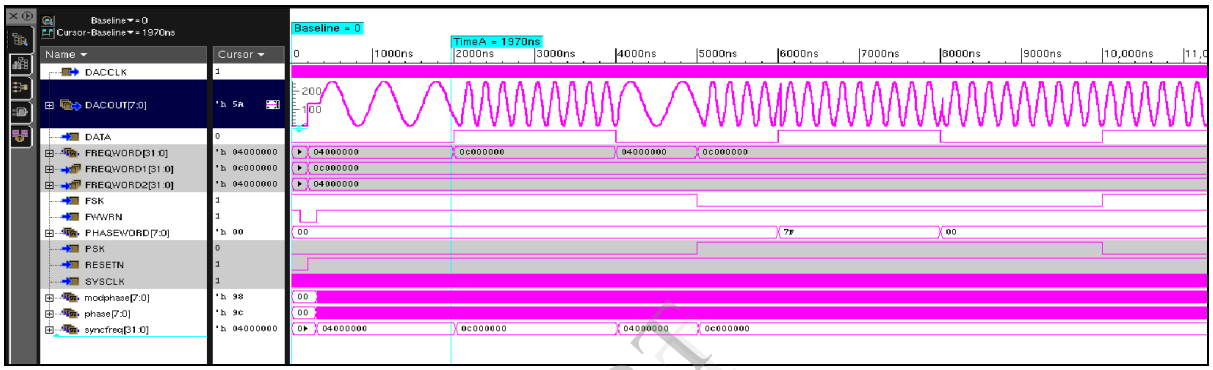

Figure 7 Simulation of DDS system Generating Sine wave for PSK/FSK

Figure 8 Layout of DDS Architecture

Table 2.Synthesis report at 200ns

Specification	DDS
Area	2204.800units
Power	970636.402nw
slack	0ps
Density	75.429%

7. Conclusions

This paper has presented a programmable sine wave generator for wireless application using PSK/FSK modulation technique. The data which are captured having clock period 200ns. On analyzing the synthesis report we get with area of 2204.800 units and 970636.402 nw power. Finally we have completed placement and routing (P&R) of DDS architecture with zero DRC error and 75.429% of density. DDS is the best method for programmable sine wave generator for PSK/FSK modulation with less power, less area, less noise, high speed and high

performance. Apart from the wireless application this architecture can be used in industrial and biomedical application.

Acknowledgements

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