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Design and Implementation of Urdhva-Tiryakbhyam Based Fast 8×8 Vedic Binary Multiplier

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***Abstract*— This paper depict the design of an efficient 8×8 binary arithmetic multiplier by using Vedic Mathematics. From various multiplication techniques, Urdhva-Tiryakbhyam sutra is being implemented because this sutra is applicable to all cases of algorithm for N×N bit numbers and the minimum delay is obtained. A 4×4 Vedic Multiplier is designed using a special 4-bit adder which is having reduced delay. The 8-bit multiplier is designed using four 4-bit multiplier and special designed adders. The computational path delay obtained is less in comparison to Array multiplier and Booth multiplier. The 8×8 Vedic Multiplier is coded in VHDL, synthesized and simulated using Xilinx ISE14.4 Software.**

Keywords: Vedic Mathematics, Urdhva-Tiryakbhyam, Vedic Multiplier , VHDL.

I .INTRODUCTION

Vedic mathematics is the name given to the ancient system of mathematics which was rediscovered from the Vedas. In compare to conventional mathematics Vedic mathematics is simpler and easy to understand. Swami Bharati Krishna Tirthaji Maharaj (1884-1960), re-introduced the concept of ancient system of Vedic mathematics [5].

The word 'Vedic' is resultant from the word 'Veda' which means the store-house of all knowledge. Vedic mathematics includes sixteen-sutras or formulae and thirteen sub-sutras. Various applications of Vedic mathematics includes theory of numbers, compound multiplication, algebraic operation, calculus, squaring, cubing, cube root, simple quadratic, coordinate geometry and wonderful Vedic Numeric Code .

Vedic mathematics is a domain which presents various effective algorithms that can be applied in different branches of engineering such as digital signal processing and computing. Most common multiplication algorithms in math coprocessor are array and booth multiplication algorithm. Due to the parallel calculation of the partial products the array multiplier takes less computation time. For high speed multiplication large booth arrays having partial sum and carry register is required [4].

An 8-bit multiplier is designed using a 4-bit multiplier and ripple –carry adders is discussed in [1]. The number of logic levels and logic delay is being reduced using the Urdhva-Tiryakbhyam sutra. Total delay obtained is less in comparison to other Vedic multiplier designs.

In [2], authors provide a study on high speed 8x8 bit Vedic multiplication architecture which is different from the conventional mathematics of multiplication like add and shift as in [13,14]. A 4x4 multiplier has been designed and implemented in [8] by the help of 6-bit special adder has been proposed for binary multiplication. Similarly in [4], a 32x32 multiplier is proposed for binary multiplication.

Authors have compared implementation of normal multiplication and Vedic multiplication. They claim that same number of multiplication and addition operations is required in both normal multiplier and Vedic multiplier. They have tested and compared various multiplier implementations such as Array multiplier, Multiplier macro, Vedic multiplier with full partitioning, Vedic multiplier using 4 bit macro, fully recursive Vedic multiplier, and Vedic multiplier using 8 bit macro for optimum speed [6]. In [7, 9, 10] implementation of binary multiplication in different applications has been discussed.

In this paper, the multiplication operation is being carried out using Urdhva-Tiryakbhyam sutra in binary, and the design is implemented using VHDL language. The following paper is structured as follows: Section II describes the Urdhva-Tiryakbhyam method. Section III explains the proposed 8x8 Vedic multiplier where as the result is discussed in Section IV followed by conclusion and references in Section V and VI.

II .URDHVA-TIRYAKBHYAM METHOD

The word "Urdhva-Tiryakbhyam" means vertical and crosswise multiplication. This multiplication formula is applicable to all cases of algorithm for N bit numbers [6]. Traditionally the sutra is used for the multiplication of two numbers in decimal number system. The same concept can be applicable to binary number system which is being discussed in this paper. Advantage of using this type of multiplier is that as the number of bits increases, delay and area increases very slowly as compared to other multipliers.

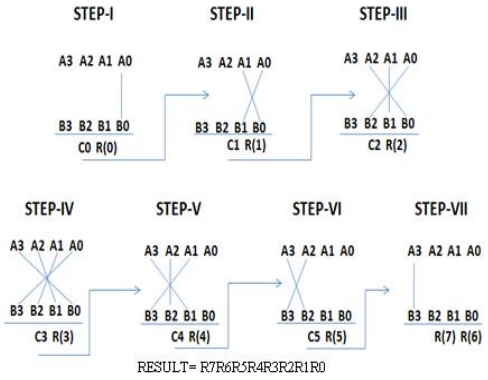

Fig.1 Multiplication method of Urdhva-Tiryakbhyam

In the above figure, 4-bit binary numbers A0A1A2A3 and B0B1B2B3 are considered. The result obtained is stored in R0R1R2R3R4R5R6R7.In the first step [A0, B0] is multiplied and the result obtained is stored in R0. Similarly in second step [A0, B1] and [A1, B0] are multiplied using a full adder and the sum is stored in R1 and carry is transferred to next step. Likewise the process continues till we get the result.

III .PROPOSED TECHNIQUE

The 4×4 multiplier in binary is implemented using VHDL. For reducing the delay of 4×4 multiplier, it is implemented using two half adders, seven full adders and a 4-bit adder.

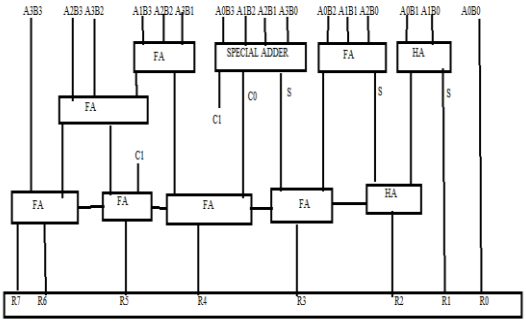

Fig 2 –Architecture of Urdhva-Tiryakbhyam 4×4 multiplier

The 4-bit adder is designed for 4×4 Vedic Multiplier in which four input can be given and three output is generated, out of which one is sum and rest two are carry. The 8×8 Vedic multiplier is designed using four 4×4 Vedic multipliers which employs Urdhva-Tiryakbhyam method. The output of these Vedic multipliers is added by modifying the logic levels of ripple carry adder [5]. The 8-bit input sequence is divided into two 4-bit numbers and given as inputs to the 4-bit multiplier blocks A [7-4] & B [7-4], A [3-0] & B [7-4], A [7-4] & B [3-0], A [3-0] & B [3-0]. The LSB product bits R [3-0] is directly obtained from one of the multipliers. The second and third multiplier block output is added directly using ADDER-1 as the second and third region is overlapping. The higher order bit of first multiplier block is added to the overlapping sum using ADDER-2 which gives the product R [7-4]. Lastly, MSB bits R [15-8] is obtained by adding the fourth multiplier output to the carry from ADDER-1 (added at the fifth bit position) and higher order bits of ADDER-3 [3]. Block diagram of the proposed 8x8 multiplier is illustrated in figure.

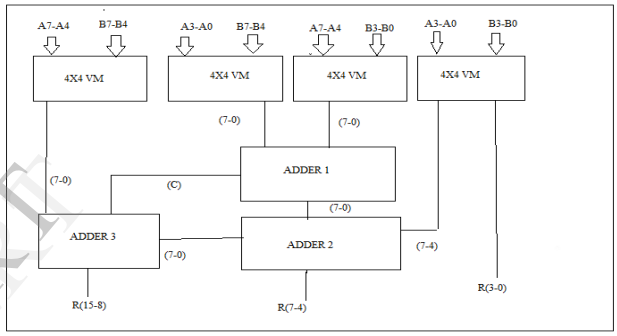

Fig 3 –Architecture of 8×8 Vedic Multiplier

IV .RESULT & SIMULATION

Here the RTL-Schematic, test bench waveform, device utilization summary are shown, which are generated using Xilinx ISE14.4 version.

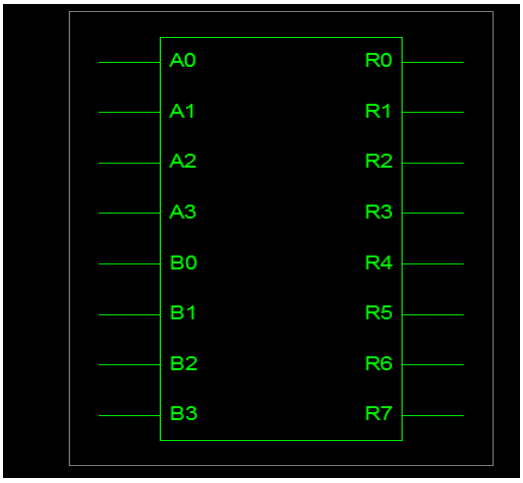

Fig 4 –RTL Schematic of 4×4 Vedic Multiplier

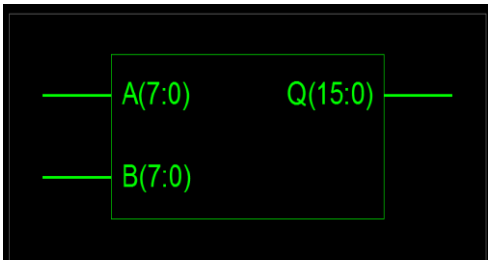

Fig 5 –RTL Schematic of 8×8 Vedic Multiplier

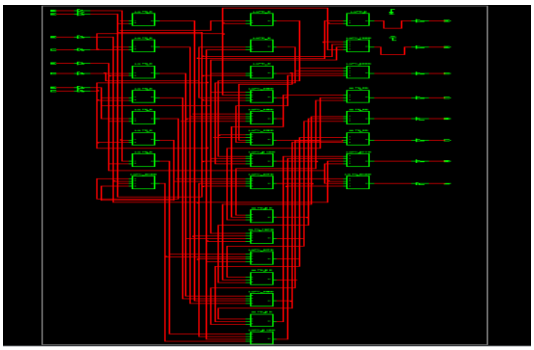

Fig 6 –Technology Schematic of 4×4 Vedic Multiplier

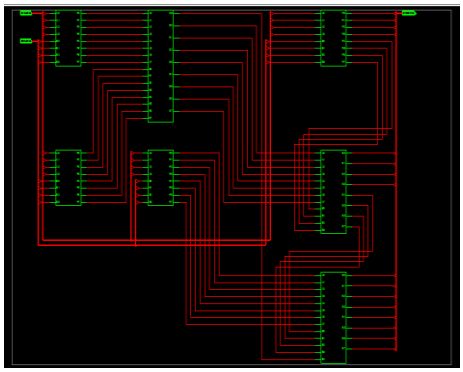

Fig 7 –RTL Schematic of 8×8 Vedic Multiplier

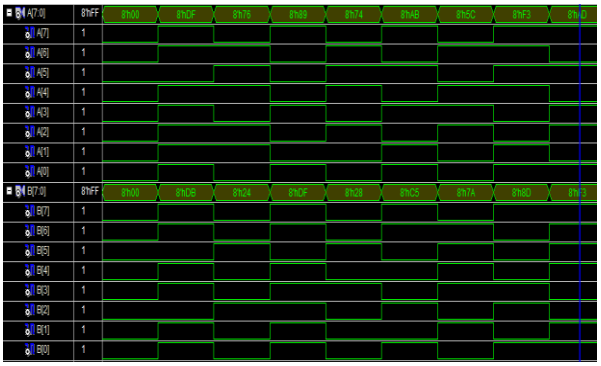

Fig 8 –Test bench Waveform of 8×8 Vedic Multiplier (Input)

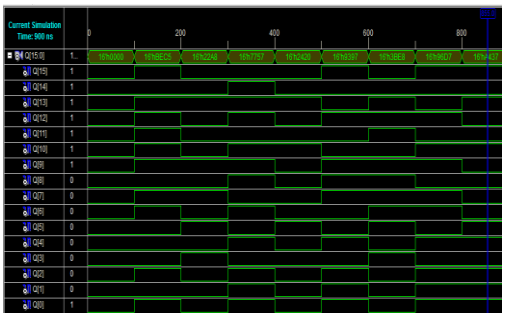

Fig 9 –Test bench Waveform of 8×8 Vedic Multiplier (Output)

TABLE-I Device Utilization Summary

Number of Slices:	91 out of 960 9%
Number of 4 input LUTs:	161 out of 1920 8%
Number of IOs:	32
Number of bonded IOBs:	32 out of 66 48%

V .CONCLUSION

A highly efficient method of multiplication, "Urdhva-Tiryakbhyam Sutra" based on Vedic mathematics is presented in this paper. The code has been simulated on Xilinx ISE 14.4 version, and implemented on Spartan 3e FPGA board. Tough Vedic Mathematics provides various Sutras, but their application to the field is not completely studied. The proposed Vedic multiplier is faster than Array and Booth multiplier in terms of execution time.

VI. REFERENCES

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AUTHOR'S PROFILE

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