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Design and Implemetation of Degarbling Algorithm

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***Abstract* — The Degarble method shall be used in the current IFF systems. A form of interference is present within the system which is called a garble or garbling. Decoder-degarbler used to decode the multiple transponder replies. A degarbler for increasing the decoding efficiency of IFF decoders in the presence of garbled signals. Three delay lines and logic circuitry are utilized to detect the presence of garble condition and bracket decodes condition. A coincidence means then determines if established decoding criteria have been met whereby there is degarbled brackets decode output to permit decoding of the pulse train data input. The bracket decoder portion of the apparatus can be operated alone to detect all the reply conditions except the one of overlapping replies.**

The proposed system is designed by using Verilog HDL, MATLAB software and implementation using Xilinx-System Generator, Xilinx ISE design tools and targeted for Virtex-5 xc5vfx100t-1ff1136 FPGA Board.

Keywords—Degarbling; IFF; Decoder; FPGA; Xilinx ISE system generator, MATLAb, Simulink

I. INTRODUCTION

The paper relates generally to detecting and decoding the reply signals transmitted from aircraft transponders. More specifically, detection and decoding under conditions in which multiple reply signals are received during a receive interval following an interrogation. The interrogation and reply signal waveforms are specified by the Federal aviation administration (FAA). The information contained in the reply signal depends on the type of interrogation – Mode A, Mode C and transponder equipment that the interrogated aircraft has available for responding.

The military identification friend or foe (IFF) system transponder reply signals consist of radio frequency energy which has been pulse modulated according to a specific format. The signal consist of up to fifteen individual pulses of 0.45µs nominal pulse width, spaced in 1.45µs multiples. The first and last pulses, separated by 20.3µs, are always present and are called the framing pulses. The remainder of the pulse positions contains the information pulses, which may or may not be present, depending upon the code being transmitted. The coding of the signal is the presence or the absence of any one, or combination, of the thirteen information pulses. The purpose of decoder is to either determine the code being transmitted, or to act as a filter allowing only selected codes to be passed though.

The form of interference present within the system is called a garble or garbling. A true garble is caused by the time overlapping of two information pulse trains with similar characteristics, i.e. the presence of the two framing pulses.

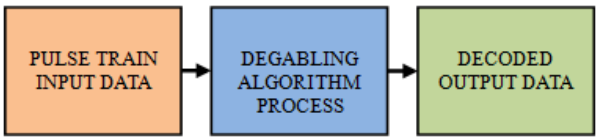

Fig.1. Design flow of degarbling methodology

The time relationship between two pulse trains is such that pulses from the second train are present within or close to the correct time slots for information pulses of the first pulse train. The result is that this type of garble can be and often is an incorrect decode of the pulse train.

The Fig.1 shows the design flow of degarbling methodology. Overall objective of this paper is design of one such logic circuit to detect and decode the multiple transponder replies. This has been implemented to tests the garble condition and decoding inhibiting circuitry to be efficient in the prevention of incorrect decodes. The same tests showed decoding efficiency, obtaining correct decodes under garble conditions, was extremely low.

II. DEGARBLING ALGORITHM

The diagram Fig.2 for electronic circuitry constructed to perform the adaptive decoding. As with most decoders, the heart of the process involves the use of delay lines, both for determining the actual code present by checking for the simultaneous presence of information at various points along the delay line, and for the detection of garble either before after or during decode time. The circuitry contains three delay lines of 20.3µs length, the time delay within each line being equal to the spacing of framing pulse within reply pulse train.

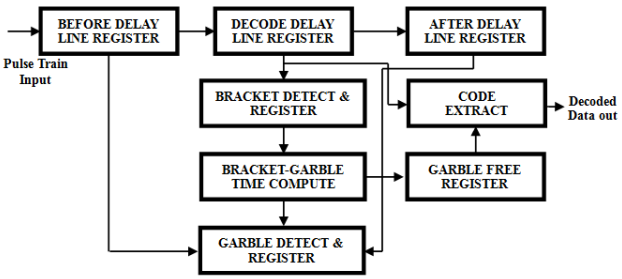

Fig.2. Block of Degarbling methodology algorithm

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The shift registers shown in the Fig.2 uses individual shift register stages for each 1.45 µs increment of delay, corresponding to the nominal information pulse spacing of the pulse train being decoded. The use of 72 stages of shift register per 1.45µs time increment determines the clock frequency of 50MHz.

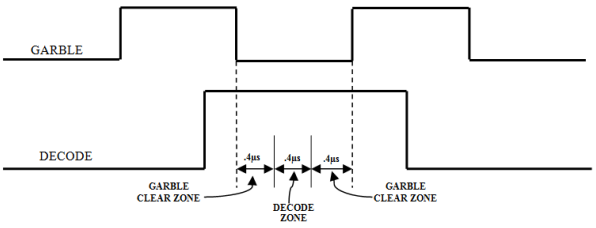

Fig.3. Decoding criteria

The primary improvement to the decoding process made by this research is recognizing decode versus garble situation with respect to time and adapting the actual decode output to that situation. Both garble and decode pulse such as might be produced by normal techniques without the application of degarbling, are present shown in Fig.3. Each of these two pulses are 0.4µs in width, with an overlap of 0.05µs between them, giving 0.3µs of effectively ungarbled decode. Intuitively, one knows that 0.35µs of ungarbled decode is sufficient for a valid decode.

A. Degabling operations and criteria

The design circuitry uses two periods of the shift registers delay line clock as the time duration for both the decode and garble clear sub-zones. This time period, approximately 40 nanoseconds due to the 50MHz clock frequency. As per the clock frequency 50MHz the each register used is of 72 bit shift register for 1.44µs pulse width.

The decoding criteria establishes sub zones, called decode sub zone and garble clear zone, within the normal decode pulse. Application of the decoding criteria at many successive points on the decode pulse, starting from the leading edge and counting to the trailing edge, results in a final decode output which is adaptive to the timing differences between the normal decode and the output of the garble detection.

III. DESIGN ANALYSIS OF DEGARBLING ALGORITHM

The bracket decode and garble output are fed to the individual shift register groups which are clocked from the same source used in the three main delay lines. As the bracket decode and garble detection output are shifted through their respective registers. It examines that a minimum width decode time sub-zone with a minimum garble clear sub-zone on each side of the bracket decode.

The possible garble condition exists when two otherwise valid pulse trains are overlapped in time. For a garble condition to exists it is necessary that an additional bracket decode be present within 20.3µs of the bracket decode detected. The purpose of the before and after delay lines is to detect other bracket decodes resulting from a garble before and after the normal bracket decode is decoded and detected by the circuitry.

The each of three delay lines has an output every 1.45µs time interval. The use of the multiple delay lines permits checking for extra bracket decodes from a garble at each of the decoding delay line information pulse output positions. Internal to the circuit AND gates are used to detect the bracket without missing an other frame of data in the next information pulses.

All the outputs are fed to the multiple AND gates to a multiple OR gates. The output of OR gate is the garble detection signal. The output of OR gate at the same time as a bracket decode from the AND gate occurs means that two overlapping pulse trains have been detected and are garbled with respect to each other.

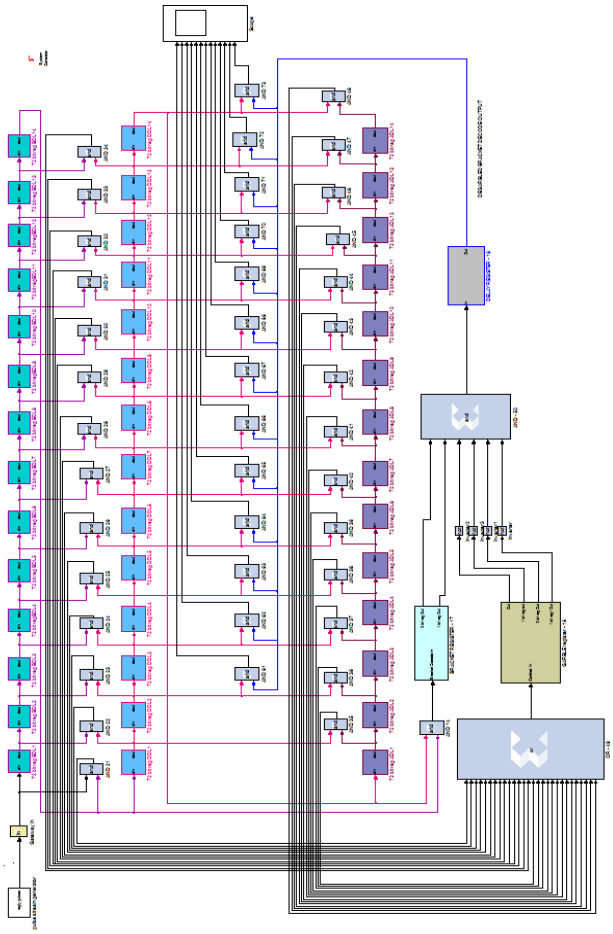

Fig.4. Implementation of degarbling in MATLAB

The Fig 4 shows that the Implementation of degarbling algorithm in system generator- MTALAB tool. The received input data pulse train has been feed to model input pins, which process the data pulse train. The entire system implementation has been done in system Xilinx block sets available in MATLAB, any kind of application in any programming language; we need an IDE which will provide a complete programming environment for the particular high level language.

Here in our system, we used Xilinx system generator, which is an IDE for developing a block level applications and ISE provides the completed environment with all the required tools like compiler, debug and simulation in it. The implementation has been tested in hardware co-simulation and hardware testing in virtex5 fpga board. To test the application, it needs to convert it into a netlist and to download to board requires a bit file, which is handled by system generator tool.

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IV. FPGA IMPLEMENTATION AND SIMULATION RESULTS

The proposed degarbling-decoder processing operators of the system generator blocks are designed using Verilog HDL, Xilinx ISE and implementation using Virtex-5 FPGA. All the basic individual degarbling operators are synthesized and simulated for different test vectors. The list of design tools and design entries are given in table 1.

Table1. Design Tools

Design Action	Tool Name
Design Entry	Verilog HDL
Synthesis	Xilinx Synthesis Tool(XST)
Simulation	MATLAB or ISE Simulator
Implementation	FPGA Editor, Plan Ahead
FPGA Configuration Target Device	iMPACT
Generating test vectors	MATLAB
FPGA Board	FPGA-Virtex5fx100t

The design models for degarbling, test vectors and decoder are designed using Xilinx System generator and pulse validation and buffering has been designed using Xilinx ISE tools. The design model for degarbling, decoder, pulse validation, buffering and its RTL schematic are shown in Fig.5, Fig.6, Fig.7, Fig.8 respectively.

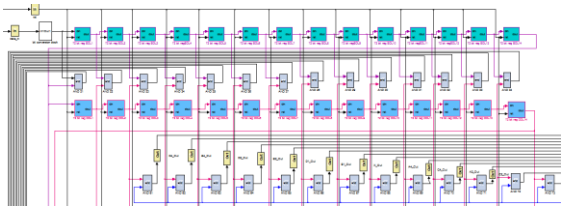

Fig.5. Design Model of degarbling

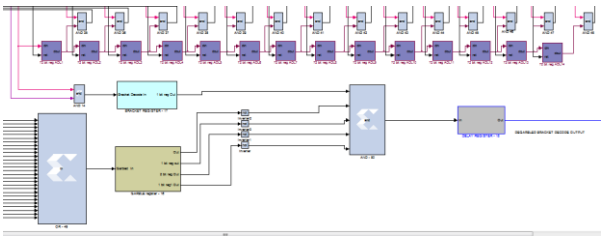

Fig.6. Design Model of Decoder

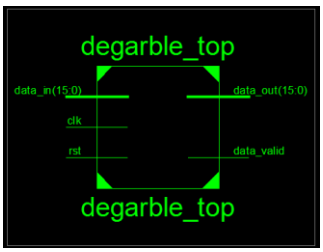

Fig.7. RTL schematic of degarbling model

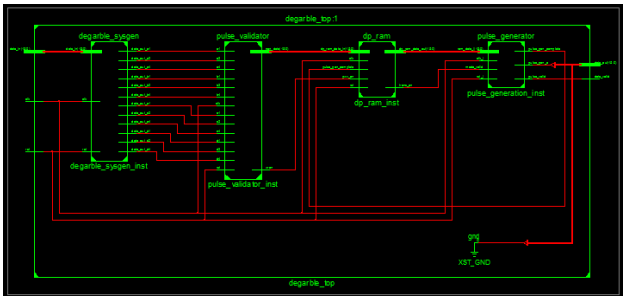

Fig.8. RTL schematic of Decoder and buffering model

The FPGA implementation results for degarbling and decoding operations using MATLAB Simulink pulse generation inputs are shown in Fig.9 a, b, c respectively.

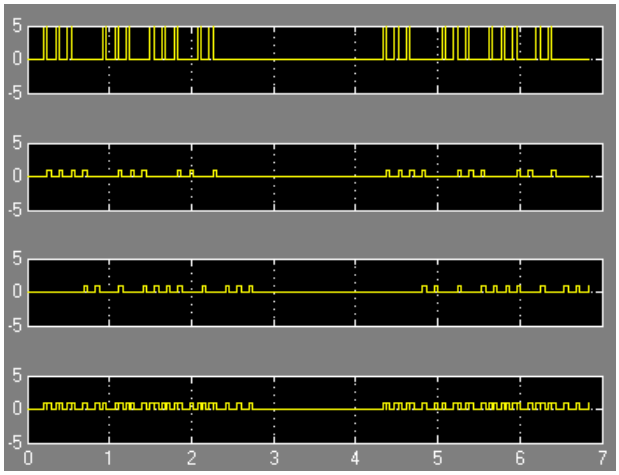

Fig.9a. Simulation input vector with different delay time

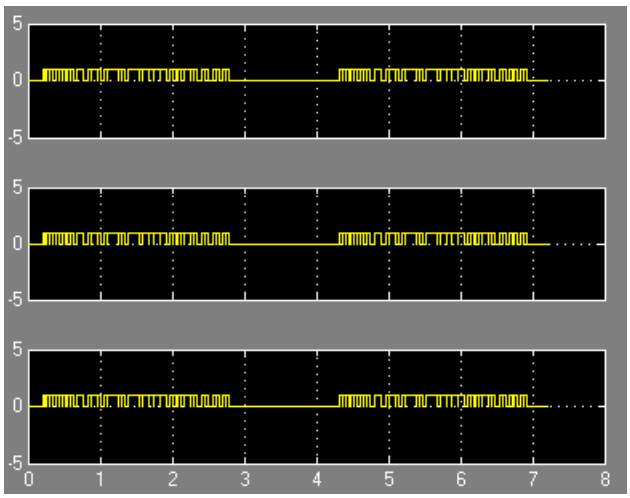

Fig.9b. simulation result for degarbling detection of individual data pulse train

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The design of degarbling model has been verified on fpga vertex-5 board, shows in the fig.10 below.

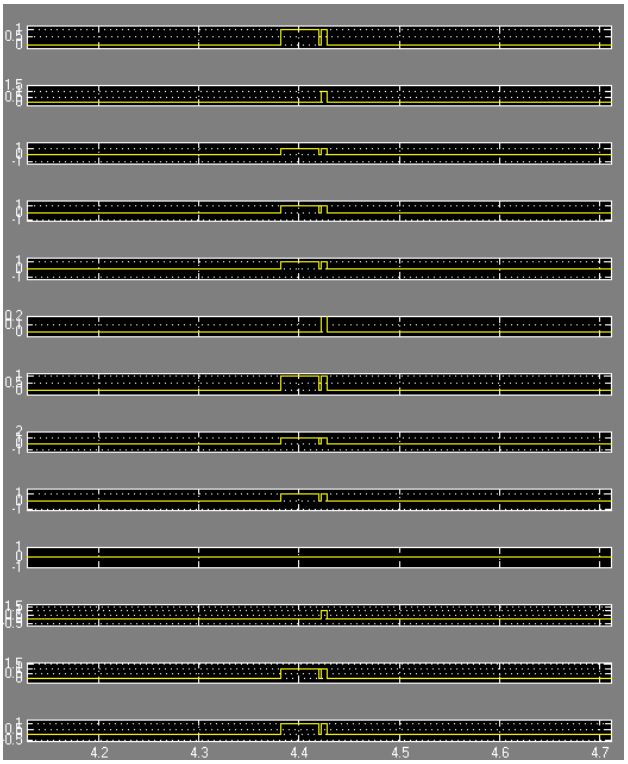

Fig.9c. Simulation result for degarbled pulse – decoded data output

The Fig.9c.Shows that individual data pulses has been decoded and copied into the buffer area. The each frame will be decoded and represented as c1, a1, c2, a2, c4, a4, x, b1, d1, b2, d2, b4, d4.

Fig.10. FPGA carrier board used for verification of degarbling algorithm

Output of degarbling operations has been observed on oscilloscope shown in the Fig.11. It shows that the decoded data pulses on the blue colored line channel, it has all the data pulses train decoded information for the receiver of IFF system for further process. All the radar communication data reception for multiple data input can be used to decode by the degarbling algorithm.

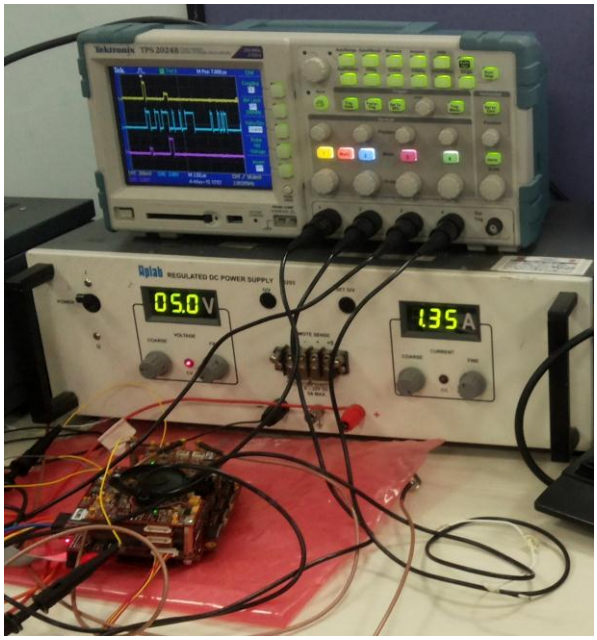

Fig.11. implementation and verification setup for degarbling algorithm

V. CONCLUSION

The Degarbling algorithm operations for detection of multiple replies from transponder is designed and implemented using Xilinx ISE and system generator for virtex-5 FPGA platform. The simulation results for all degarbling operations and implementation results for different test input are observed and analyzed for performance improvements mainly in secondary radar applications such as detection of multiple replies from the target and decoding of data.

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