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Design and Optimization of Asynchronous counter using Reversible Logic

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***Abstract*—Reversible logic design in recent times has gained interest due to its less heat dissipation and low power consumption .Reversible logic design can be used for realizing any Boolean function using the basic reversible gates. This paper presents the design of T Flip flop and counter using reversible logic gates and comparison of existing reversible T Flip Flop design with optimized reversible T Flip Flop. Asynchronous counters are designed using the existing and proposed T FF. The proposed counter has considerably less power consumption improving the performance of the circuit. Various matrices are tabulated for the circuits designed. Proposed reversible counter is found to be better in terms of power dissipation by about 50% and gate cost by 25% .**

Keywords— Reversible logic, Low power VLSI, Power dissipation, garbage outputs, constant inputs.

1. INTRODUCTION

Energy dissipation is one of the main considerations in digital circuit design. The irreversible computation tends to lose information during execution. The information loss dissipates in the form of heat, dissipation of heat results in power dissipation. In order to reduce the power dissipation a new logic called reversible logic has been introduced .The main idea behind this logic is to reduce power dissipation by preserving information content. By implementing circuits using reversible logic a significant amount of heat energy dissipated can be decreased .Due to their capability to reduce power dissipation; it finds applications in low power VLSI design, quantum computation and optical information processing.

It has been showed that for each bit of irreversible logic computation there will be a loss of kTln2 joules of energy, where k is Boltzmann's constant, t is absolute temperature at which execution is performed [1].Bennet showed there would not be kTln2 energy dissipation if the system allows reproduction of inputs from the produced outputs [2].The main difficulties in designing the reversible circuits are to reduce the number of quantum cost, garbage outputs, delay and constant inputs. This paper proposes optimized design for T flip flop and 4 bit asynchronous counter .

Reversible T FF designed using Sayem gate is compared with the proposed T flip flop design. Asynchronous counters are designed using both existing and proposed design and compared for power, garbage outputs, transistor cost.

2. REVERSIBLE LOGIC GATES

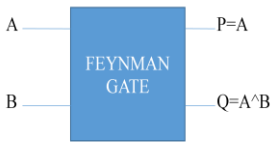
Reversible logic gates have the same number of inputs and outputs and there is a bijective mapping between inputs and outputs. Any gate is said to be reversible if we can reproduce input vector from output vector and vice versa. Fan out is not allowed in reversible logic, it can be achieved using additional reversible basic gate. This paper discusses about reversible basic gates like Feynman gate, Fredkin gate, Sayem gate and their transistor implementation. These gates are used in implementing sequential circuits.

2. A. FEYNMAN GATE

Figure 1 shows a 2*2 Feynman gate of input vector In(A, B) and output vector Out(P, Q).Table 1 shows the truth table of Feynman gate. The quantum cost of Feynman gate is 1.

The outputs defined as P=A , Q=(A xor B).

This gate can be used for fan out or for duplication of required outputs in reversible circuit design.



A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Figure 1: Feynman gate Table 1: Truth table

Transistor Implementation:

Figure 2 shows the transistor implementation of 2*2 Feynman gate.

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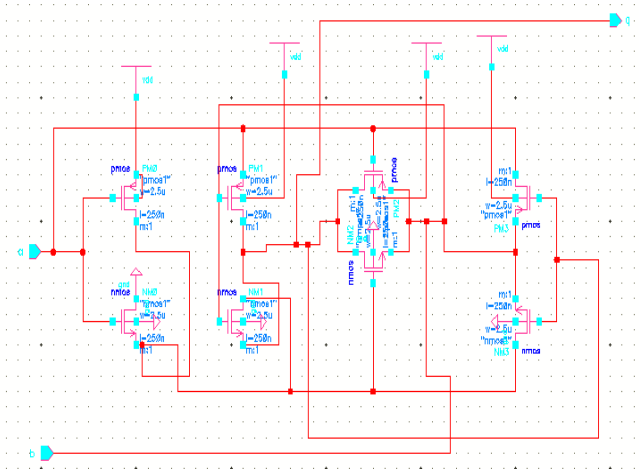


Figure 2: Schematic of Feynman gate.

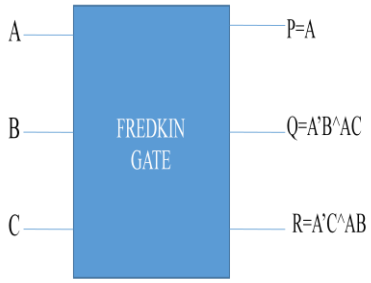
2. B. FREDKIN GATE

A 3*3 Fredkin gate is as shown in figure 3 with inputsA,BandC and outputsP,QandR. The quantum cost is 5.Table 2 shows the truth table of Fredkin gate whose outputs are defined as

P=A

Q= (A'B xor AC)

R= (AB xor A'C).



A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Figure 3: Fredkin gate. Table 2: Truth table.

Transistor Implementation:

Figure 4 shows the transistor implementation of 3*3 Fredkin gate. Fredkin gate needs only four transistors.

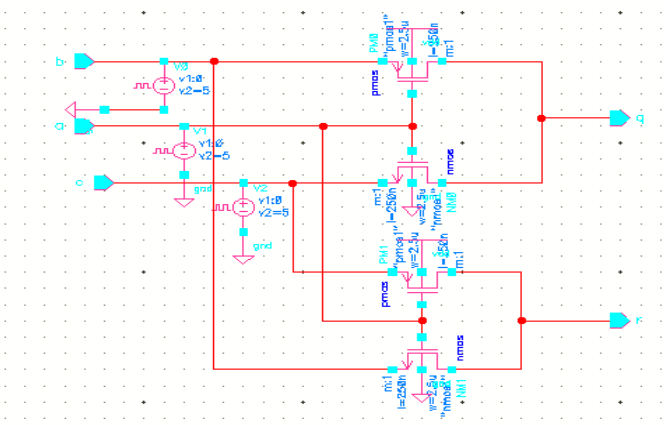


Figure 4: Schematic of Fredkin gate.

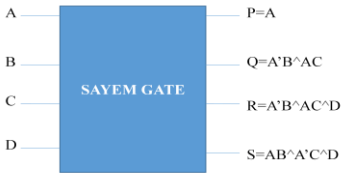
2. C. SAYEM GATE

A 4*4 Sayem gate is as shown in figure 5with inputs A, B, CandD and outputs P, Q, RandS. The quantum cost of Sayem gate is 14.Table 3 shows the truth table of a 4*4 Sayem gate whose outputs defined as P=A

Q= (A'B xor AC)

R= (A'B xor AC xor D)

S= (AB xor A'C xor D).



A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	1
0	0	1	0	0	0	0	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	1
0	1	1	1	0	1	0	0
1	0	0	0	1	0	0	0
1	0	0	1	1	0	1	1
1	0	1	0	1	1	1	0
1	0	1	1	1	1	0	1
1	1	0	0	1	0	0	1
1	1	0	1	1	0	1	0
1	1	1	0	1	1	1	1
1	1	1	1	1	1	0	0

Figure 5: Sayem gate. Table 3: Truth table.

Transistor Implementation:

Figure 6 shows the transistor implementation of 4*4 Sayem gate which is used to design Flip flops.

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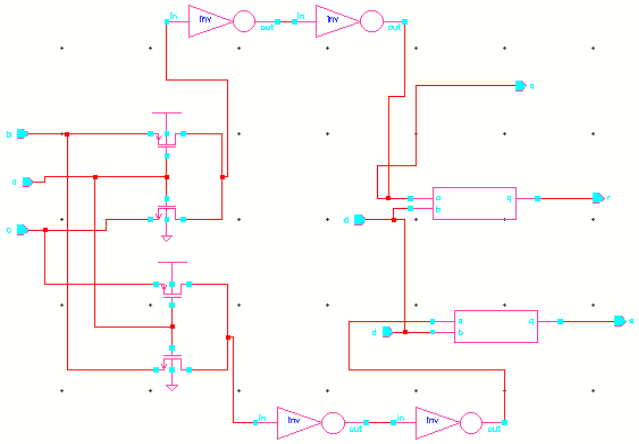

Figure 6: Schematic of Sayem gate

3. EXISTING AND PROPOSED DESIGNS OF T FLIP FLOP

3. A. EXISTING REVERSIBLE T FLIP FLOP.

T FF toggles output whenever the input is high and retains the output when input is low. Depending upon the input it either retains the previous state or toggles the output. Table 4 shows the truth table of T FF. Figure 7 shows the implementation of T FF using Sayem and Feynman gates.

T	Q_t+1
0	Q_t
1	Q_t'

Table4: Truth table of T FF

Existing T FF is made up of 2 Sayem gates and 1 Feynman gate. This has 4 constant inputs and 3 garbage outputs.

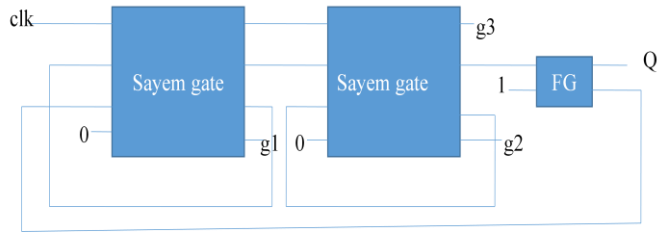

Figure 7:T-Flip Flop Using Sayem And Feynman Gate(Existing design).

Figure 8 shows the schematic of T flip flop using two Sayem gate and one Feynman gate.

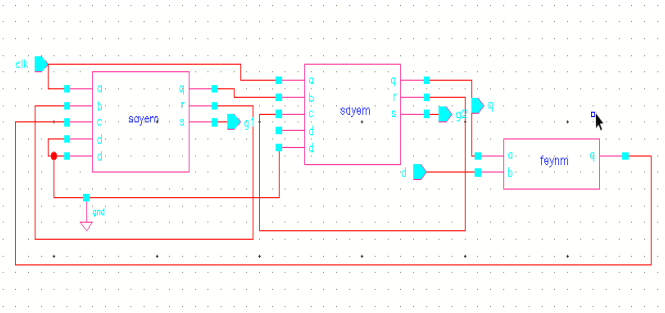

Figure 8: Schematic of existing T flip flop.

3. B. PROPOSED REVERSIBLE T FLIP FLOP.

Figure 9 shows the design of proposed T FF using basic reversible logic gates. This Flip flop is designed using 2 Fredkin gates and 3 Feynman gates. This Flip flop has 3 garbage outputs and 2 constant inputs. T FF works similar to that of existing reversible T FF.

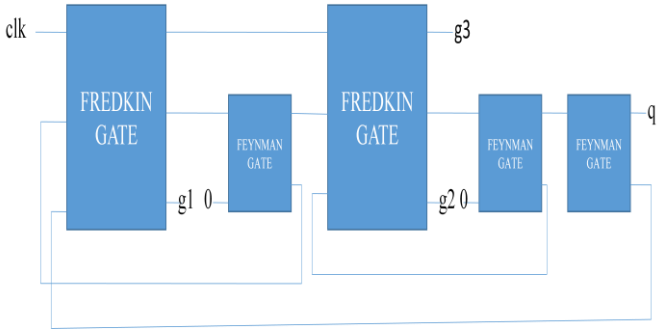

Figure 9: Proposed T flip flop using basic reversible gates.

Figure 10 shows the schematic of the proposed T FF.

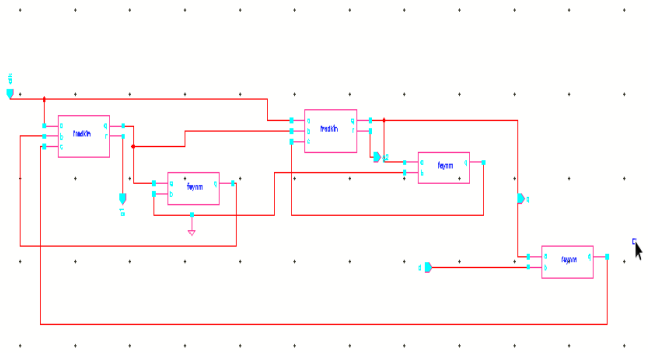

Figure 10: Schematic of Proposed T flip flop.

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3.C. ASYNCHRONOUS UP/DOWN COUNTER USING T FLIP FLOP

The below figure 11 shows a 4 bit asynchronous up/down counter using the reversible T flip flop.The output of each stage is fed to clock of next stage. This has 4 garbage outputs and 4 constant inputs. The proposed T Flip Flop has been used in the design of asynchronous counter instead of existing one.

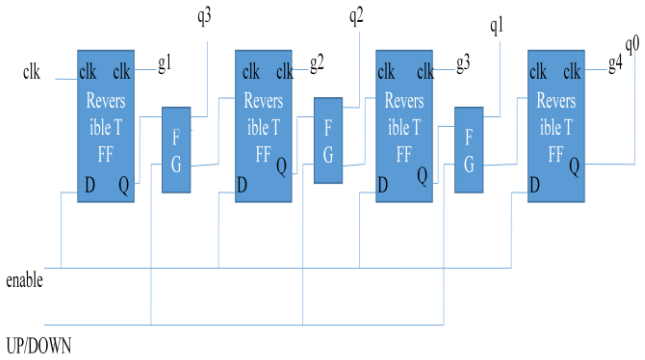

Figure 11:4 bit asynchronous up/down counter using proposed reversible T flip flop.

3.SIMULATION AND RESULTS

Simulation is based on "Cadence Virtuoso ADEL"tool180nmtechnology. Figure 11 shows the simulation output of reversible T FF .The Flip flop is a negative edge triggered flip flop.

Figure 12 shows the simulation output of proposed T FF using basic reversible logic gates. The flip flop toggles at negative edge of clock and if T is 1.

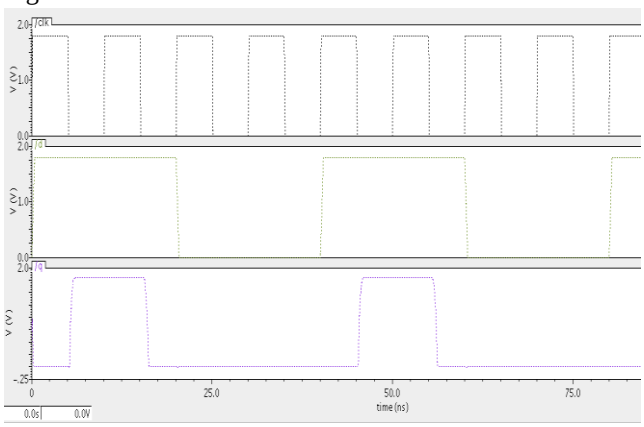

Figure 12 : Simulation of proposed T FF.

Figure 13 shows the output of a 4 bit asynchronous up/down counter. The counter counts downwards when the up/down signal is high and counts down when up/down control signal is low as shown below.

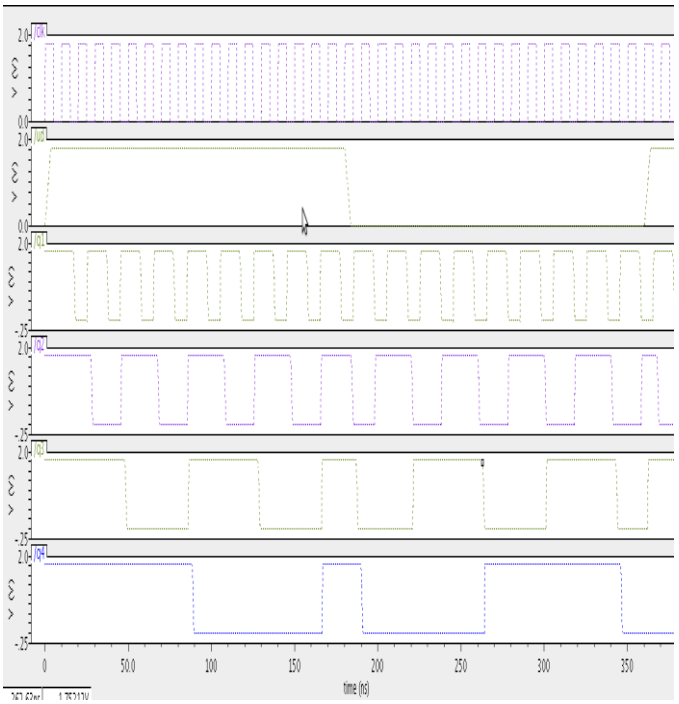

Figure 13: Simulation of a 4bit asynchronous counter using proposed T flip flop.

4.CONCLUSION AND RESULTS

This paper presents the design of basic reversible gates, T flip flops ,asynchronous counters. Comparison of Gate cost, Quantum cost, Power dissipation, Garbage outputs and constant inputs of existing reversible T FF with the proposed reversible T FF is as shown in Table 5. Also comparison of counters using existing and proposed T flip flops is as shown in Table 6. Proposed reversible T flip flop have considerably less power dissipation than the existing improving the performance of circuits. Hence proposed reversible T flip flop shows a better performance in terms of power and gate cost, quantum cost.

Figure 14 shows the graphical representation of comparison of various metrics of existing and proposed T Flip flops. Figure 15 shows the graphical representation of comparison of power dissipated by existing and proposed T Flip flops.

Figure 16 shows the graphical representation of comparison of various metrics of existing and proposed Asynchronous counters. Figure 17 shows the graphical representation of comparison of power dissipated by existing and proposed Asynchronous counters.

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	Gate cost	Quantum cost	Power (W)	Garbage outputs	Constant inputs
Existing design	7	15	516.4e-6	3	4
Proposed design	5	13	278.7e-6	3	2

Table 5: Comparison of existing and proposed T FF.

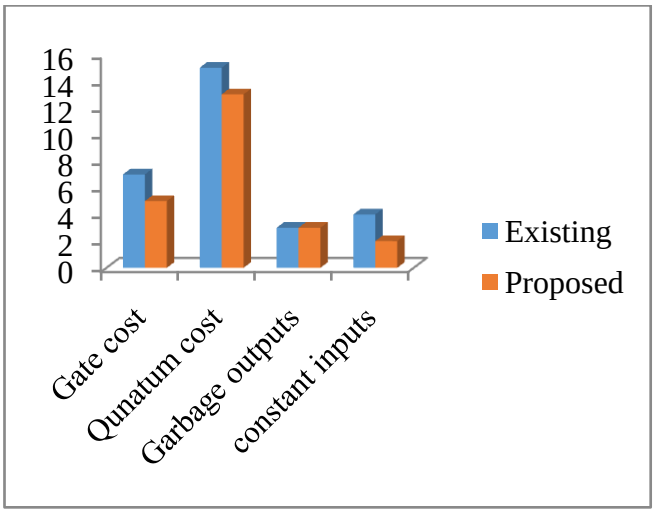

Figure 14: Comparision of various metrics of T flip flop.

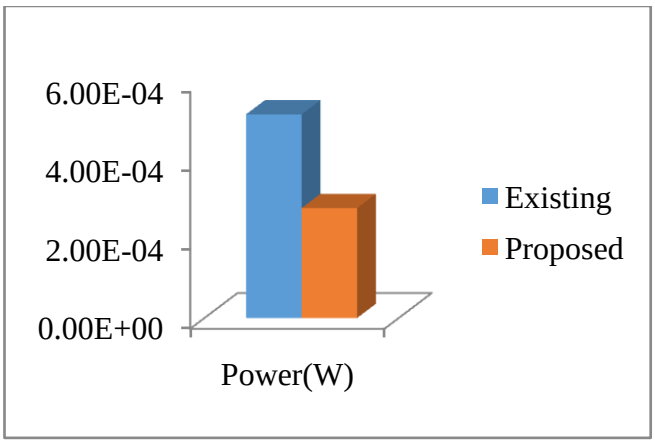

Figure 15: Comparison of power consumption of existing and proposed T FF.

There is 25% reduction in gate cost and 56% reduction in power consumption when compared to the existing design.

	Gate cost	Quantum cost	Power (W)	Garbage outputs	Constant inputs
Existing design	31	63	2.11e-3	12	16
Proposed design	23	55	913.2e-6	12	8

Table 6: Comparison of counters using existing and proposed T FF.

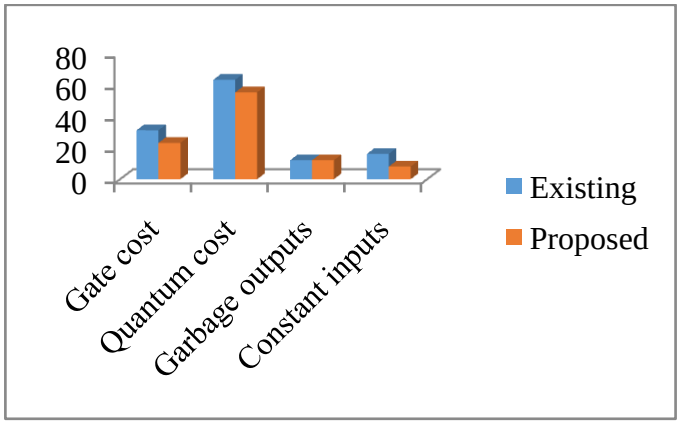

Figure 16: Comparision of metrics for counter design using existing and proposed T flip flops.

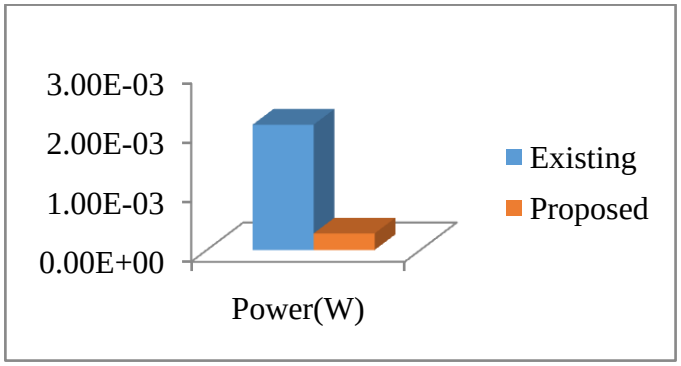

Figure 17: Comparison of Power for counters using existing and proposed T FF.

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