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Design and Performance Evaluation of FPGA-based Audio Systems on Zed Board-Zynq SoC

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Abstract **- Field Programmable Gate Arrays (FPGAs) have become a vital part of the global electronic industry since their discovery in 1985. Compared to traditional Application Specific Integrated Circuits (ASICs), FPGAs are more versatile due to their lower non-recurring engineering (NRE) cost and re-engineering feature, allowing anyone with a FPGA board and programming skill to design and implement electronic models. For many applications, modern FPGAs can exceed the performance requirements of ASICs, making them widely accepted in various fields, including audio systems. This paper presents two audio systems developed using the ZedBoard-Zynq SoC Development Board, which will be compared in terms of design and performance. Results show that the second audio system outperforms the first in terms of performance.**

Index terms - Field Programmable Gate Array, Audio System, Intellectual Property, Noise, Sampling rate, Sound Pressure Level.

I. INTRODUCTION

Audio systems are ubiquitous in today's society, playing a crucial role in a wide range of applications, from consumer electronics to professional audio equipment. Traditional audio system design has been dominated by Application Specific Integrated Circuits (ASICs), which are custom-built for a specific task. However, the design process for ASICs can be time-consuming and expensive, and they lack the flexibility to adapt to changing requirements.

Field Programmable Gate Arrays (FPGAs) provide a flexible, cost-effective alternative to ASICs, allowing for the implementation of complex digital circuits in a programmable manner. FPGAs consist of configurable logic blocks and programmable interconnects, allowing for the implementation of complex digital systems. In recent years, there has been a growing interest in using FPGAs for audio system design, as they provide a high level of flexibility and can be customized to meet specific performance requirements.

The ZedBoard-Zynq SoC Development Board is a popular platform for FPGA-based audio system design. It combines a powerful processing system based on the ARM Cortex-A9 processor with a programmable logic fabric, allowing for the implementation of complex digital circuits. The ZedBoard-Zynq board offers a range of connectivity options, making it suitable for interfacing with a wide range of audio input and output devices.

In this paper, we present two FPGA-based audio systems developed using the ZedBoard-Zynq SoC. The first system serves as a baseline, while the second system utilizes advanced FPGA-based processing techniques to achieve improved performance. The comparison between these systems demonstrates the potential of FPGA-based audio system design using the ZedBoard-Zynq platform.

To implement both Audio models and understand the nature of an Audio signal several related studies were done as follows,

- Several studies have explored the use of FPGAs for audio system design. For instance, [1] proposed an FPGA-based digital audio amplifier that provides improved power efficiency and reduced distortion compared to traditional Class-D amplifiers. Similarly, [2] presented an FPGA-based audio processor that uses a custom algorithm to reduce noise and improve the signal-to-noise ratio.
- Other studies have explored the use of FPGAs for specific audio applications, such as speech processing and noise reduction. For example, [3] proposed an FPGA-based speech recognition system that uses a custom algorithm to identify spoken words in noisy environments. Similarly, [3] presented an FPGA-based system for noise reduction in speech signals.
- While these studies demonstrate the potential of FPGA-based audio system design, there is still a need for research on the use of FPGAs for general-purpose audio processing. The two audio systems presented in this paper aim to fill this gap by demonstrating the potential of FPGA-based audio system design for general-purpose audio applications.

II. PROPOSED APPROACH

The proposed approach in this paper involves the development of two FPGA-based audio systems using the ZedBoard-Zynq platform. The first system serves as a baseline and is implemented using standard FPGA-based design techniques. The second system utilizes advanced FPGA-based processing techniques to achieve improved performance.

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The first audio system implements a basic audio processing pipeline that consists of an analog-to-digital converter (ADC), a FIR Filter, and a digital-to-analog converter (DAC). The ADC samples the input audio signal and converts it to a digital format, which is then processed by the DSP. The processed signal is then converted back to an analog format by the DAC and output to a speaker.

The second audio system utilizes advanced FPGA-based processing techniques to achieve improved performance. Specifically, [4] it utilizes a digital signal processor (DSP) and custom algorithm that performs real-time noise reduction and equalization. The algorithm is implemented using the programmable logic fabric of the ZedBoard-Zynq board and is optimized for high performance and low latency.

Starting from deciding the Architecture specifications to output measurement I divided the whole process into two sections, [5] Integrated Design Environment (IDE) setup and [5] Hardware setup.

A. Integrated Design Environment (IDE) Setup

Xilinx Vivado is a high-level integrated development environment (IDE) used for designing and implementing Field-Programmable Gate Array (FPGA) projects. [6] It supports a wide range of FPGA families and devices, including Zynq-7000, Kintex UltraScale, and Virtex UltraScale+. Vivado includes the tools for simulation, synthesis/implementation, and bitstream generation in a single environment, most FPGA development tools do not carry the same feature, so Vivado is used throughout this experimental study as IDE.

Xilinx Vivado provides a graphical design flow for creating, editing and managing FPGA designs. It includes a large library of pre-built intellectual property (IP) cores that can be used to accelerate the design process and reduce development time. It also provides debugging features, and it can be integrated with other Xilinx tools such as Xilinx Software Development Kit (SDK) and the Xilinx System Generator for DSP, to provide a complete solution for FPGA design and implementation. Vivado includes optimization features to improve the performance of the design, such as timing analysis and optimization, power analysis, and area optimization.

The FPGA flow which is used in the Vivado design suite for this study is featured in Figure 1.

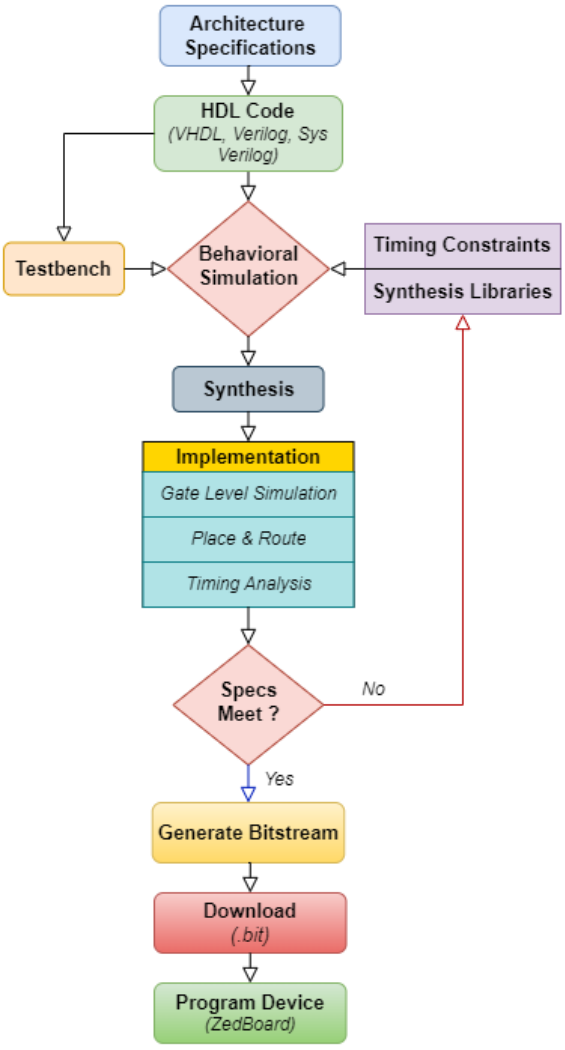

Figure 1- FPGA flow in Vivado suite

After implementing the proposed model for Audio system Intellectual Property (IP) block design is generated. An IP block design for the implemented second Audio system is featured in Figure 2.

The netlists generated at the synthesis stage are used during the implementation stage to perform several steps:

- Translation: merges the incoming netlists and constraints into the required technology of the target FPGA.
- Mapping: fits the design into the available resources, such as CLBs and I/Os.
- Place and Route: places the design and routes the components to satisfy the timing constraints.

Finally, a bitstream, which is used to program the FPGA with the design, is generated and downloaded to the device.

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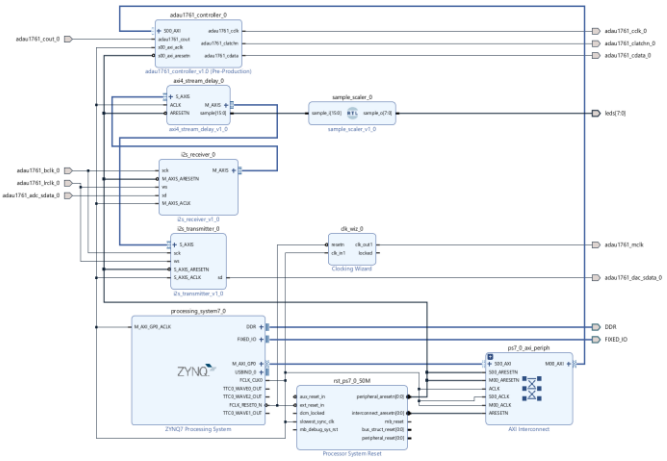

Figure 2- IP Block, Advanced Audio System

B. *Hardware setup*

[7] The ZedBoard-Zynq board is a powerful development platform that combines a field-programmable gate array (FPGA) with a dual-core ARM Cortex-A9 processor. This combination makes it an ideal platform for simulating the bitstream of an audio system.

In an audio system, a bitstream is a series of digital audio samples that represent an analog audio signal. The Zynq board can generate and process bitstreams using the FPGA, which can be programmed using hardware description languages such as Verilog and VHDL. To simulate a bitstream of an audio system, a user would typically write software code that configures the FPGA to generate a series of digital audio samples. These samples can be generated at a specific rate, which is typically referred to as the sample rate.

The sample rate of an audio signal is the number of samples that are taken per unit of time. It is typically measured in Hertz (Hz), which represents the number of samples per second. The mathematical expression for the sample rate can be expressed as:

$$fs = N/T$$

Where:
fs is the sample rate (in Hz)
N is the total number of samples taken
T is the duration of the audio signal (in seconds)
In our case, a 10-second audio signal contains 48,000 samples, the sample rate can be calculated as follows:

$$fs = 48{,}000 / 10 = 4800 \text{ Hz}$$

This means that the audio signal was sampled 4800 times per second.

The Nyquist-Shannon sampling theorem, also known as the Nyquist criterion, states that to accurately reconstruct a continuous signal from its samples, the sampling frequency must be at least twice the highest frequency component present in the signal.

Mathematically, if we denote the continuous signal as x(t) and its Fourier transform as X(f), then the Nyquist-Shannon sampling theorem can be expressed as:

$$f_s \geq 2B$$

where f_s is the sampling frequency, B is the highest frequency component present in the signal x(t), and the inequality symbol (\geq) means "greater than or equal to".

In other words, the sampling frequency must be greater than or equal to twice the bandwidth of the signal. If the sampling frequency is too low, the high-frequency components of the signal will be aliased, resulting in a distorted signal. Therefore, to accurately sample a continuous signal, we must choose an appropriate sampling frequency according to the Nyquist-Shannon sampling theorem.

Once the digital audio samples are generated, they are processed using custom hardware modules implemented in the FPGA. These modules perform various signal processing operations, such as filtering, equalization, or compression. The modules are designed and implemented using hardware description languages such as Verilog, VHDL, and System Verilog.

[7] The ZedBoard board also has an onboard audio codec that is used to convert the digital audio samples back to an analog audio signal. The audio codec consists of digital-to-analog converters (DACs) that convert the digital audio samples to analog signals, which can be amplified and sent to an output device such as headphones or speakers. Figure 3 shows the ZedBoard-Zynq setup for the implemented Audio Systems.

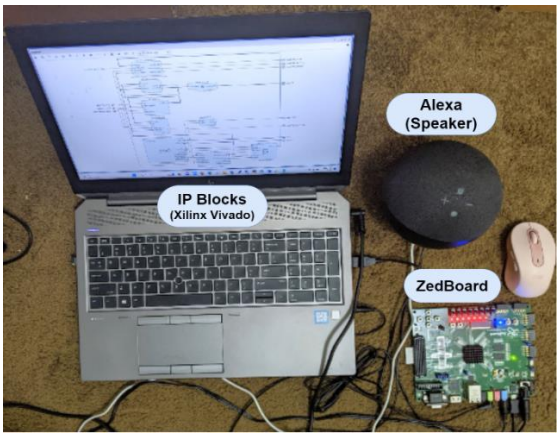

Figure 3- ZedBoard-Zynq Setup

III. RESULTS

[8] For Audio signal output measurement, few parameters need to be considered which are as follows,

- Sampling Rate: 48000Hz
- FFT Size: 1024 bins [47Hz/bin]
- Frequency Weighting: A
- Response Time: Fast
- Scale: Logarithmic

These parameters are constant for both Audio models.

A. *Baseline Audio System*

The first Audio System is developed using a basic FPGA structure where we have a basic Audio Processor, Clock Generator, SPI Controller, Debouncer, and FIR Filter. After

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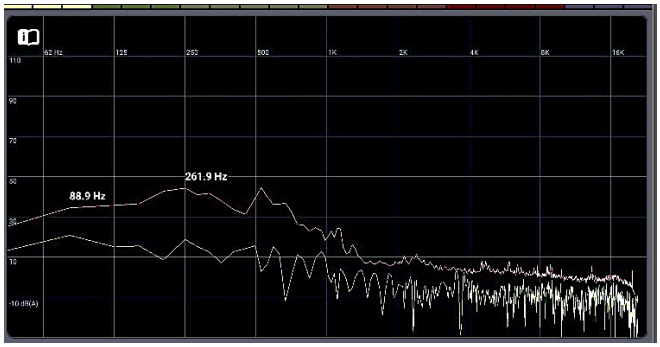
successful implementation in Vivado and ZedBoard, we received Graph 1 below showing Noise/Sound in dB and Frequency in Hz.

X-axis: Sound in dB [-10 to 110]

Y-axis: Frequency in Hz [0 to 16000Hz]



Graph 1- Baseline Audio System measurement

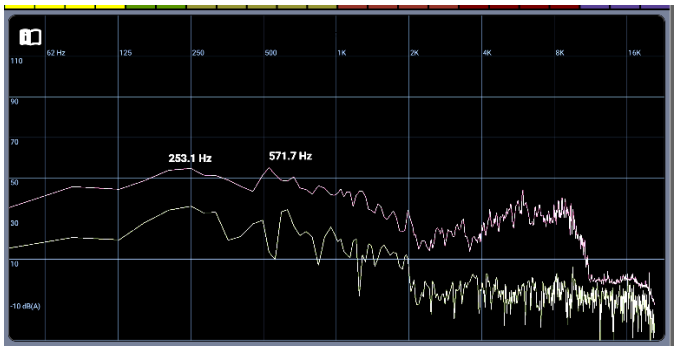
TABLE I. FREQUENCY AND NOISE MEASUREMENT OF BASELINE AUDIO SYSTEM

Frequency (Hz)	Noise/Sound (dB)			
	Min	**Avg**	***Max***	***Peak***
261.9	23.9	40.3	48.1	52.8

Sound Pressure Level (SPL) at 40.3dB = 20 log10 (p/pref)
p = (20 * 10^ (-6)) * 10^ (40.3/20) = 0.0632 Pa

B. Advanced Audio System

The Second Audio System is developed using advanced FPGA techniques where we have Audio Processor, Clock Wizard, Stream Delay, Audio Codec, Audio Processing Receiver, Audio Processing Transmitter, Sample Scalar, Couplers, Peripheral, and Digital Signal Processing (DSP). After successful implementation in Vivado and ZedBoard, we received Graph 2 below showing Sound in dB and Frequency in Hz.



Graph 2- Advanced Audio System measurement

TABLE II. FREQUENCY AND NOISE MEASUREMENT OF ADVANCED AUDIO SYSTEM

Frequency (Hz)	Noise/Sound (dB)			
	Min	**Avg**	***Max***	***Peak***
571.7	22.3	50.2	58.8	63.8

Sound Pressure Level (SPL) at 50.2dB = 20 log10 (p/pref)
p = (20 * 10^ (-6)) * 10^ (50.2/20) = 0.1995 Pa

IV. CONCLUSION

This paper proposed two FPGA-based Audio Systems which are implemented using Xilinx Vivado and ZedBoard-Zynq development board. After successful implementation, the noise and frequency are measured from the output audio signal. The measurement value clearly shows that the second audio system is 10 times more intense as compared to the first audio system as our measurement scale is logarithmic. Also, the Sound Pressure Level (SPL) result implies the second audio system is more powerful as compared to the first one.

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REFERENCES

[1] Yong Yan, “Design and Implementation of Audio Signal Acquisition System Based on FPGA,”, 4th International Conference on Mechanical, Control and Computer Engineering (ICMCCE), pp. 352-354, Oct 2019.

[2] Jingbo Zhang, Xiaofeng Wang, and Shufang Zhang, “Audio Signal Processing Based on FPGA,”, Advanced Research Materials, Vols. 1049-1050, pp 1759-1764, Trans Tech Publications Ltd, Switzerland, 2014

[3] Shing-Tai Pan and Xu-Yu Li, “An FPGA-Based Embedded Robust Speech Recognition System Designed by Combining Empirical Mode Decomposition and a Genetic Algorithm”, IEEE Transactions on Instrumentation and Measurement, Vol. 61, Pp-2560-2572 No. 9, September 2012.

[4] Nian Zhang, Tam Le, Sasan Haghani, “Design and Implementation of FPGA Based LMS Self-Adjusting Adaptive Filtering System for Audio Signal Processing”, WSEAS TRANSACTIONS on SIGNAL PROCESSING, Volume 13, pp- 256-263 2017.

[5] Spenser Gilliland, Pramod Govindan, Thomas Gonnot and Jafar Saniie, “Performance Evaluation of FPGA based Embedded ARM Processor for Ultrasonic Imaging,”, Joint UFFC, EFTF, and PFM Symposium, vol. 2, pp. 519-522, 2013.

[6] Xilinx, “Zynq-7000 All Programmable SoC Technical Reference Manual”, UG585 (v1.5) March 7, 2013 [Online]. Available: http://www.xilinx.com/support/documentation/user_guides/ug585Zynq-7000-TRM.pdf

[7] AVNET,” ZedBoard Getting Started Guide”, Version. 7.0, 2017, [Online], Available: ‘’https://www.avnet.com/wps/wcm/connect/onesite/7ae0f288-1cc5-4283-9e85-300c5401b680/GS-AES-Z7EV-7Z020-G-V7-1.pdf?MOD=AJPERES&CACHEID=ROOTWORKSPACE.Z18_NA5A1I41L0ICD0ABNDMDDG0000-7ae0f288-1cc5-4283-9e85-300c5401b680-nxyWIEs

[8] Ágoston Katalin, “Studying noise measurement and analysis,” 11th International Conference Interdisciplinarity in Engineering, INTER-ENG 2017, 5-6 October 2017, Tirgu-Mures, Romania, Volume 22, 2018, Pages 533-538.