Design and Simulation of 360 MHzX19 SRD Multiplier

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Abstract: **This paper presents an implementation of a SRD-based wide-band picoseconds impulse generator. Through the study of SRD model, a method of abating the nonlinearity of the model is proposed and with proper modeling of the diode, a detailed study of the SRD multiplier has been analyzed. This model permits analysis of harmonic generator circuits with greater generality and can be directly used in commercial circuit simulation for design of SRD circuits. The factors that affect the SRD performance, such as the driving waveform, noise floor close to output frequency, transmission line length and diode parameters are investigated. It has also been verified by comparison of measurement data and model analysis simulation results. The verification confirms the model ability to represent accurately SRD pulse behavior for a wide range of diode operating conditions. The parameters of a wide-band, short impulse generator circuit are analyzed through designing the generator circuit with output spectrum from 0.5 GHz to 10 GHz, and the results gain nice validation by experiment.**

Key Words: Harmonic, inter-modulation, impulse circuit, matching circuits, phase reference, pulse generator, SRD comb generator, ultra-wideband (UWB), step recovery diode (SRD).

I. INTRODUCTION

Step recovery diodes (SRDs) are strongly nonlinear two terminal devices which are used as comb generator, wave formers [1] and are typically used in hybrid local oscillators, especially where low phase noise is required: in terrestrial communications, satellite communications, TVRO, low cost UWB transmitters [2]-[4], mobile communications. As a frequency multiplier the SRD is used for example in millimeter wave link radios. Another typical application of the SRD is as a comb generator in microwave and millimeter wave samplers, which are used in frequency counters, sampling scopes, phase locked synthesizers, and network analyzers [5-7]. One of the most outstanding characteristics of the step recovery diode (SRD) is the high conversion efficiency with high frequency multiplication order. It provides a method for generating power at high frequencies by using a low cost oscillator. Input frequencies of SRD could extend down to 10 MHz and output frequencies up to 94 GHz [1, 8].

There are a large of frequency multipliers designed by means of comb generator [9, 10] which produces a set (or "comb") of discrete harmonically related tones in the frequency domain, corresponding to a periodic waveform in

the time domain [11] and well performance has also been obtained. Several analyses of harmonic generation circuits using the step-recovery diode have been to some extent restricted in their generality of application by their dependence upon some knowledge of the waveforms of currents flowing through the diode [12-15].In the past, designs of SRD frequency multipliers were mainly based on the method of Hamilton and Hall [16]. The circuit solving algorithm used by simulators are based on the Newton-Rapson algoritm so cannot be used directly in commercial circuit simulators. Only one conduction angle per cycle have often been analyzed in the past under the assumption that the amplitude of the nth harmonic was small and recently more than one conduction angle per cycle has been observed in an analog simulation study [17,18]. A new SRD model which is more accurate by considering the voltage ramp during the transition process has been realized using the CAD of SRD, and which can be directly used in commercial circuit simulators [19].A model of the SRD is created based on the extracted diode parameters, and the delay-line SRD impulse generator has been described by G. D. Cormack [20], as its circuit is very typical and could help simplify the analysis. Since 1960s, there have been a great number of publications that studied various topics on SRD pulsers such as modeling, circuit design etc. In 1983, a computer simulation model of a conventional p-n junction diode was proposed by Goldman [21] and characterized by experiments. However, as we know, an SRD is essentially different from a conventional p-n junction diode and due to the very strong nonlinearity of the diode; its characteristics cannot be modeled very well by this method under all design conditions. With the ever rising demand of integrated circuits, more accurate designs are required to develop the circuits in a medium where tuning is not possible. Of course, there are other reasons which influence the medium of the circuit; microstrip circuits have small size, low weight, high reliability, while waveguide has low loss and high power handling capability. In parallel the development of computer technology and computer aided design tools provide us with the possibility of simulation and optimization of the circuits to achieve an accurate design and optimum performance.

The purpose of this paper is to present some of the critical performance characteristics of SRD diode as they represent the critical features of multiplier design for stable operation and maximum efficiency. In this paper a model of the SRD is

developed for the CAD of SRD circuits. It can be used in any circuit simulators. First, a modified basic model of the SRD is established; finally, applications of this model to analyses of comb generators and frequency multipliers are given. In order to improve the efficiency of CAD of SRD frequency multipliers, we have investigated the modeling of the diode and features of SRD frequency multipliers. The method of abating the nonlinearity of' the model is proposed and with proper modeling of the diode, a detailed study of step-recovery-diode multipliers has been analyzed and optimized with the aid of computers, using harmonic balance methods [22,23]. The results show that abating the nonlinearity of the model of the diode to some extent while optimizing the circuit does not change the characteristics of the circuit radically. Due to the strong nonlinearity of the diode and the large number of harmonic involved, harmonic balance analysis of the SRD frequency multiplier can be troublesome and the possible instability make convergence precarious. In addition to choosing an advance simulator for good convergence, other efforts should be made to find the correct solution efficiently for this type of circuit. However, designs based on this model have very limited accuracy, and high performances of actual circuits are usually achieved by experimental adjustments. Thus, simulation and optimization of SRD circuits by computers are desirable to accomplish more accurate circuit designs.

A systematic design of a 360MHzX19 SRD-based comb generator is given as an example and gives detailed analysis to input matching circuits, impulse generator circuit and output matching circuits, and attain the minimum power of -26 dBm in 6.840GHz and achieve the pulse width less than 1ns. The comb generator is fully characterized by varying the input power over the range of 20dBm±5dB and record the output power variation at 19th harmonics. The variation of noise floor close to the output frequency (carrier±1MHz) has also been characterized by changing the input power. Then effect of inserting transmission line between SRD and filter circuit is proposed. Repetitive measurements show that this comb generator has magnitude uncertainty of ±0.3dB at (25±1)[0]C room temperature at rated 21dBm input excitation whose output power fluctuation should be less than 0.8dBm.

The paper is organized as follows. Section II discusses a SRD model and verified through simulation and experiments. Section III analyzes the design detail in ADS software and harmonic balance simulation. Experimental results have been discussed in Section IV and finally a conclusion is provided in Section V.

II. COMPUTER MODEL

The step recovery diode (SRD), which is also called elsewhere the snap-off diode or charge storage diode, was first recognized in the early 1950's. The step recovery diode (SRD), or "snap diode," has an unusual operating characteristic   to store a large amount of charge when it's forward biased, and keep conducting when reverse biased until all the stored charge are recovered by a negative current, then a very abrupt turn-off happens that ends in sub-nanosecond transitions(<1ns) [24]. So an ideal step recovery diode functions as a switch from a high impedance state to a

low impedance state, corresponding to a small reverse bias capacitor (depletion C_r) and a large forward bias capacitor (diffusion C_f),with zero switching time between states. The limiting factor in switching from C_f to C_r is the rapidity with which charge can be extracted from the i layer. The voltage ramp begins when the forward bias is reduced, after that there is a fast transition and finally a rounding off until all the stored charge has been swept out from the i layer. Then the non-conducting state continues as the voltage becomes further negative. Thus, the conducting state is continuously transformed to the non-conducting state through a process of turn-off. A typical C-V curve of the SRD is shown in Fig. 1.
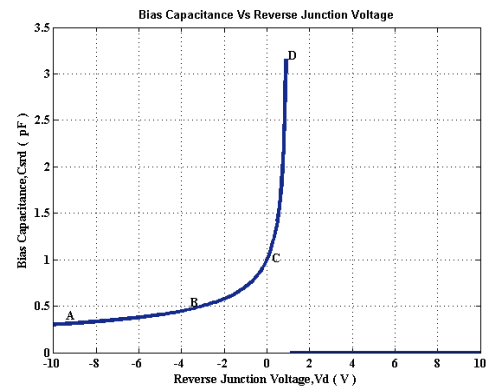

Fig .1.The C-V curve of SRD

Accordingly, straight lines CD and AB represent the conducting and non-conducting bias capacitances, respectively. The BC section is a parabolic curve representing the turn-off process. From Fig. 1 we find in the reverse direction that when SRD is reverse biased, capacitance is nearly constant and also is very small. However, when SRD turns into forward biased, capacitance become quite large rapidly, and come into being abrupt change, which is just intrinsic factor of attaining high harmonics together with high efficiency. The transition process can be described by a parabolic function, which is determined by the two state capacitance [19]. The characteristic of the diode shows that the smaller is the forward capacitance, the weaker is the nonlinearity of the model. This highly nonlinear capacitance characteristic is also accompanied by a highly nonlinear shunt resistance which depends on the forward bias voltage and RF input power. Therefore, the degree of abatement depends on how much C_f is changed, and the operation condition of the diode.

Implementation of the SRD model is based on [25,26] that here the diode series resistance R_S is internal to the PN diode(circuit)while in the referenced publications it is external to the diode and placed in series with the package inductance L_P . The SRD capacitance is the centerpiece of the model. It is a simple piece-wise linear model consisting of three line segments: a small capacitance when the diode is reverse biased (V_d <0), a large capacitance when the diode is forward biased (V_d >$F_C V_j$) and a linear ramp between ($0<V_d<$ $F_C V_j$).Specifically,

$$C_{srd} = C_r \qquad\qquad \text{for } V_d < 0$$

$$= C_r + \frac{\tau/R_f - C_r}{F_C.V_j} V_d \quad \text{for } 0 < V_d < F_C.V_j$$

$$= \frac{\tau}{R_f} \qquad\qquad \text{for } V_d > F_C.V_j$$

where V_d is the voltage across the capacitance and other model parameters C_r, τ, R_f, F_C, V_j are the reverse bias capacitance, minority carrier lifetime, forward bias resistance, forward bias depletion capacitance coefficient, junction potential respectively(model parameters).When the SRD is forward biased, the p-n Junction acts like a dynamic or nonlinear resistor (R_f) · The relationship of C_f, R_f and the minority carrier lifetime can be related as given by Kotzebue [27],

$$\tau = R_f C_f$$

where 'τ' is the minority carrier lifetime of the SRD given by the manufacturer. The assumption is that the value of the forward capacitance $C_f = \tau/R_f$ is larger than the reverse capacitance C_r.If it is not, it will be snapped at C_r, thus making the overall capacitance linear. If both parameters C_r and τ are set to zero, the SRD capacitance C_{srd} is effectively removed from the model. The standard p-n diode junction and diffusion capacitances are available and can be included, if desired, by setting the corresponding parameters C_{io} (zero bias junction capacitance) given by the manufacturer and T_t (transit time) to non zero values. For a realistic model, C_f much larger than C_r thus making the overall model highly nonlinear.In addition to the two constant capacitors, the series parasitic resistance, the package inductance and capacitance should be taken into consideration. The equivalent circuit of an SRD including all these factors is shown in Fig. 2(a) and a fully functional SRD diode model for CAD simulation shown in Fig.2 (b).
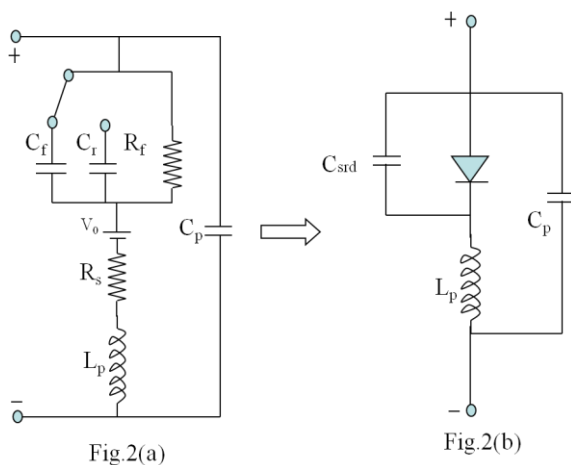

Fig .2. (a) Conventional model of SRD (b) Fully functional SRD model for CAD simulation

III. SIMULATION AND DESIGN OF SRD FREQUENCY MULTIPLIER

The transition process introduced was studied and modeled by Moll and Hamilton [28]. Based on it, a new model that we will apply in the design of impulse circuit was established by Zhang and Raisanen [19]. It can be seen from Fig. 2 that the series parasitic resistance, the package

inductance and capacitance have some influence on the model, in addition to the two constant capacitors. On the other hand, we also need select proper SRD for the simulation model. In the simulation of circuits, good initial conditions are sometimes critical for convergence. Besides that, they often help the simulator use less computational resources (time and memory) to find the correct solution. Normally, there is a way to set initial conditions in the simulator. Using a simplified or less ill-behaving circuit is one way to find good initial conditions. Another process for obtaining convergence at the time of simulation is to start with values of certain components that work and then to move toward the desired values.

Several important parameters of SRD are step recovery time T_t, the minority carrier lifetime τ and reverse junction capacitor C_r and value of the parameters for setting the initial condition in the simulation as follows:

(a), step recovery time $T_t \leq 1/f_0$, ($1/f_0$ is output signal period);

(b), the minority carrier lifetime $\tau \rangle\rangle 1/2\pi f_{in}$ ($\omega_{in}\tau > 10$ is adequate for most purposes).

(c), reverse junction capacitor $C_r <= 1/2f_o X$, where $10 < X < 20$; where X is approximate impedance level assumes $50\,\Omega$ system.

(d), reverse voltage is higher than impulse amplitude. Based on those above, we choose DH543-62A produced by TEMEX, whose T_t =90-140 ps, τ = 20ns, C_r =1pF and the minimum of reverse voltage is 30V.

From the characteristic of SRD shown in Fig. 1 we know that the smaller is the forward bias capacitance, the less nonlinear is the diode model. Thus, we can at first reduce the nonlinearity of the diode model by changing the forward bias capacitance to a smaller value. The reduction of the nonlinearity of the model may vary possibly help the simulator to find a solution, which can be used to obtain the desired final solution efficiently. It can be seen that the forward biased resistance turns into a very small and nearly constant resistance right after the diode is forward biased. In the case of the diode under test, the value of the forward biased resistance is of the order of 1 ohm is given by the data sheet, which corresponds to a forward biased capacitance of 35nF.However, the depletion capacitance of this diode, which is used as the reversed bias capacitance C_r, in our model, is given as about 1 pF. Comparing with the calculated C_r shows the very strong nonlinearity of the diode model. Directly using this model in circuit simulators would definitely cost a lot computational resources and most probably cause convergence problems. By abating the nonlinearity of the model of the diode to an appropriate extent, the simulation and optimization of SRD frequency multipliers can be carried out faster and easier.

Based on the modified SRD model, the simulation is directly done with the Advance Design System@ (ADS).A systematic schematic diagram of the SRD frequency multiplier circuit and ADS-created simulated circuit model has been shown in Fig. 3.
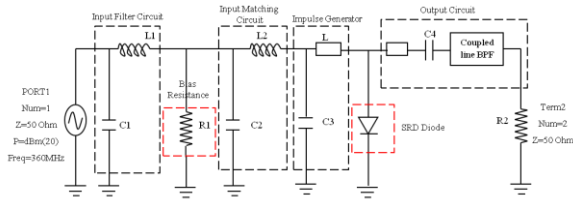
Fig.3. The Schematic circuit of an SRD

Fig.4. Layout of SRD comb generator. Substrate: Alumina, ε_r =9.9, h=25mil

The SRD frequency multiplier can be divided into three parts: the impulse generator, input matching circuit and output circuit of comb generator. The impulse generator which converts the energy in each input cycle into narrow large amplitude voltage pulse occurs one per input cycle. The input matching circuit provides a match to the $50\,\Omega$ source impedance at the 360 MHz generator driven frequency. The output resonant circuit, which converts the impulse into a damped ringing waveform at the output frequency .The output circuit of the comb generator, namely the transmission line, coupling capacitor and the output band pass coupled line filter which filtered out the desired harmonic form the output circuit of the frequency multiplier.

On account of wideband output spectrum for 1GHz ~ 10 GHz of the output port, we cannot go along match for any single frequency from energy point of view. If energy concentrates at a certain frequency point, then energy of other frequencies will become very small. Microstrip line can be regarded as invariableness over very wide frequency band from low frequency to high frequency; therefore, we employ microstrip line connecting with 50 ohm interface system at the output port. However, when the frequency is higher than 5 GHz, TEM wave will produce disperser, so we need to find a substrate which satisfies the above conditions . We find that thin substrate and low relative dielectric constant are able to meet qualifications required by means of ADS simulation. Consequently, we utilize alumina substrate for the output port, whose relative dielectric constant Er=9.9, and substrate thickness we apply is 25 mil.

In order to verify the method for improving the efficiency of the CAD of the SRD frequency multiplier presented above, we designed a 19x 360MHz SRD micro strip frequency multiplier. The harmonic-balance simulation was completed with ADS using 35 harmonics with an input frequency of 360 MHz and power of +21 dBm. At first, the circuit was optimized for high conversion efficiency with driving inductor realized by means of a microstrip line L and RF capacitor C_3. The details calculation [19, 27, 29] of a straight micro strip line inductor is simple and can be estimated by using Hamlton Hall's method [16, 27] to tune it at input frequency is shown in Fig.4. The harmonic-balance analyzes with swept rf power were carried out with C3 equal to 3.6pF and 3.9pF and compared with the experiment. Then the circuit was optimized and refined experimentally for high conversion efficiency with $C3$, equal to 3.6pF.
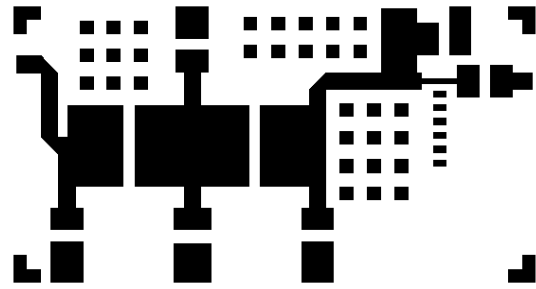
The circuit used for determining the optimum source impedance is shown in Fig 4. The optimum source impedance can be defined as the source impedance which gives the maximum conversion efficiency at the desired harmonic. Once this optimum source impedance is known, an impedance matching circuit can be designed by using ADS simulation software to match the diode to a 50 Ω source. For best efficiency, it is necessary to match the relatively low impedance of the SRD circuit to $50\,\Omega$ at the input frequency. The additional lumped components, L2 and C2, provide a match to the $50\,\Omega$ source impedance at the 360 MHz generator driven frequency and the external bias has been replaced by the self-bias resistor R1. Fig 5. Shows Z_{in} plotted on a Smith chart after matching with an L2, C2 input matching network.
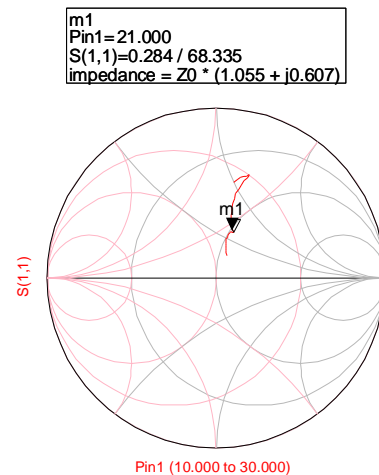
Fig.5. Simulated Smith chart plot of Z_{in}

Meantime, a quarter wave resonant transmission lines at 6.8 GHz is one way to boost the level of the desired harmonic above the other harmonics before additional filtering. The microstrip line length is calculated according to the highest frequency, namely 6.8 GHz, and its length is less than a quarter of wave length. The line is terminated with a resistance chosen so that the loaded Q of the resonant line is approximately (pi/4) N, where N is the ratio of desired output frequency to input frequency (N = 19 for this design). The output of the resonant line for this value of Q is a damped sine wave that spans one input cycle. However, a piece of $50\,\Omega$ transmission line simply for the output port is still not the best so Q is adjusted by varying the degree of coupling to the 50

Ω loads with a small series capacitor which can be used to block the DC and partially reflect the RF output. The length of line is adjusted so that the sinusoid rings with a period of 120 ps .It also provides us with more design freedom for optimization of the circuit. Fig.6(Red curve) notes the voltage waveforms at the input of the comb generator and at the junction of L1, L2, and C1. Note that the impulse has not been totally filtered at this point. Blue curve shows the impulse generated into the 50 ohm load without the output filter.
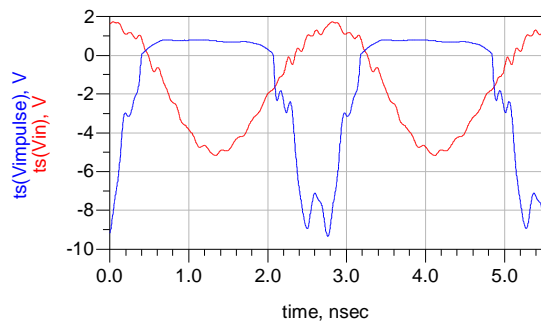
Fig.6. Shows the input waveform and that of the impulse at the diode/transmission line node

By varying parameters such as junction capacitance, reverse recovery time, and parasitic inductance, different pulse shapes optimized for the task required can be manipulated based upon manufacturer's data sheets.Note that the circuit layout in Fig.4 is basically a comb generator and it is going to be used as a part of the frequency multiplier. This part of the circuit can be optimized either at this stage or together with the output filter circuit of the frequency multiplier at a later stage. Thus, the transmission line and the capacitor can be optimized to give the maximum conversion efficiency, though the output signal should be filtered further.

The design of output circuit of the frequency multiplier consists mainly of the design of a band pass filter. The bandwidth of the filter should be determined according to the specific application. Normally, narrow band coupled line band pass filter is used: whereas wide band pass filter could also be employed for a particular application [30]. The design method can be found in other literature [22,31]. Here a microstrip coupled-line band pass filter is designed and simulated by using ADS. Once the designs of the comb generator and the band pass filter are accomplished, they can be put together to form the frequency multiplier. However, since the output of the comb generator is very rich of harmonics and the desired harmonic could be a very high order harmonic, the effects of all those unwanted harmonics can not readily be neglected. Apparently, the filter can extract the desired harmonic from the comb generator, and drop the unwanted harmonics. The circuit layout of coupled line BPF and simulation results are shown in Fig.7and Fig.8 respectively.
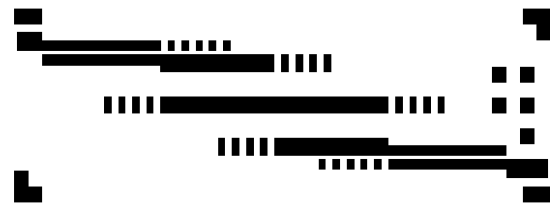

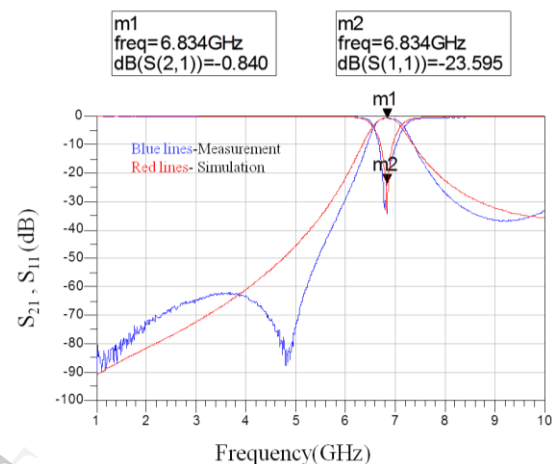Fig.7. Layout of coupled line BPF.Substrate: Alumina, ε_r =9.9, h=25mil

Fig.8. Measured(bule curves) and simulated (red curves)S-parameters of coupled line BPF

Fig.9 illustrates the ringing waveform at the 50 Ohm load at the output of coupled line filter. The electrical length, line impedance, and coupling capacitor all affect the shape and frequency response of the final signal. The goal of varying these component values is to maximize the power available in n^{th} comb.
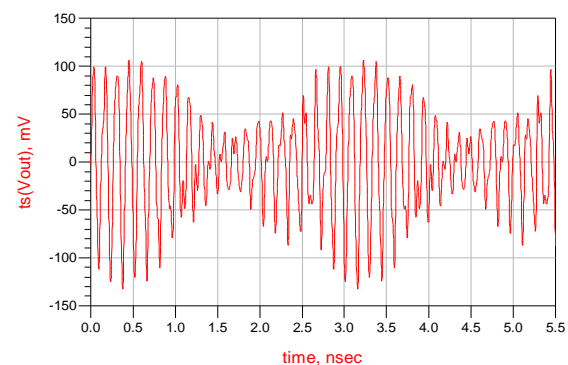

Fig .9. The ringing waveform at the output of 50 Ohm load

Finally, The harmonic balance simulation results at the SRD output and cascading SRD with filter output are shown in Fig.10 and Fig.11 provides a look at the output spectrum centered around 6.834 GHz (X19 of input frequency)when the input power is 21 dBm. It can be seen that the simulated results are relatively satisfying, the minimum output power reach -25dBm. Nevertheless, it should be pointed out that the simulation results are very ideal. Therefore, the input matching circuit and the output circuit consisting of a transmission line, a capacitor and a band pass filter should be re-optimized to get the optimum performance.
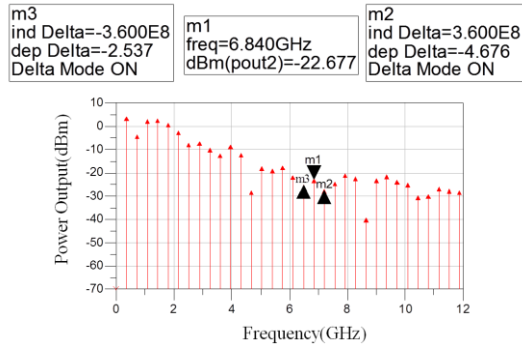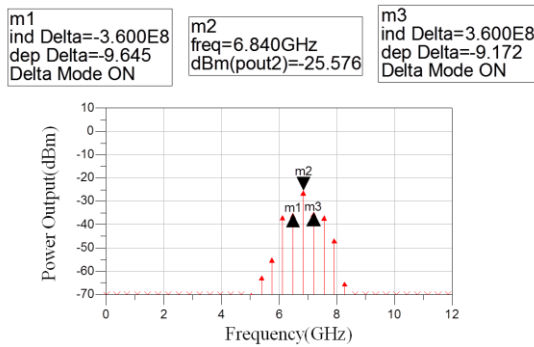
Fig.10. Simulated Power spectrum at at 50 Ohm load

Fig .11. Simulated Power spectrum at filter output

IV. EXPERIMENTAL RESULTS

A 19 x 360 MHz SRD frequency multiplier is realized with microstrip circuits and TEMEX made DH543-62 ceramic package SRD diode has been used. The input circuit is used for impedance matching between the 50 ohm source and the low impedance of the diode. The output circuit consists of a section of transmission line, a capacitor, and a separate microstrip band pass filter. At last, an impulse circuit was fabricated and the experiment was carried out with a 360MHz input sinusoidal signal at the power level of 21 dBm. The comb generator and band pass filter were built separately and layouts are shown in Figs.4 and 7, respectively. The whole pulse generator circuit fabricated on 25mil alumina substrate with its dielectric constant of 9.9, the overall dimension of the assembly is 19 mm × 10mm ×0.6mm. The substrate thickness of the comb generator was chosen to match the ceramic package. The band pass filter could also be integrated on the same substrate as the comb generator. However, a separate band pass filter, which has more freedom in choosing substrates, and which provides the flexibility of experimentation, was used. High performances of actual circuits are usually achieved by experimental adjustments. In the process of adjustments; we found that input power and some components of matching circuits had influence on the output power to a certain extent. Using Agilent E8257D PSG analog signal generator (250KHz-40GHz) as the source and Rohde & Schwarz FSU spectrum analyzer (20Hz-43GHz), the power at SRD and Filter output are measured and the experimental results are shown in Fig. 12 and Fig.13.
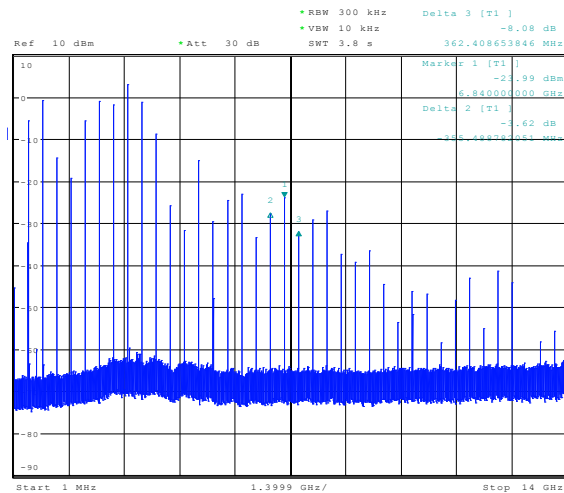

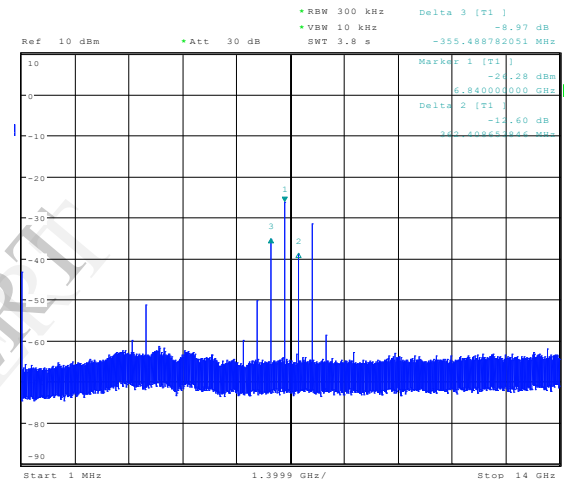Fig.12. Power spectrum at SRD output

Fig.13. Power spectrum at filter output

The experiment is carried out by changing the input power ($20dBm \pm 5dB$) and recording output power at the 19th harmonic. By changing the input power level, the noise floor close to the output frequency ($6.84GHz \pm 1MHz$) has also been characterized. The measurement results are shown in Fig 14.Fig.14 shows that above 21dBm of input power level the output power at 19th harmonic almost saturate and signal to noise ratio has been improved (>10dB) at higher input power (>21dBm).
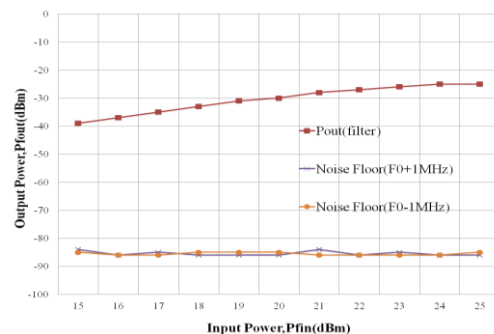

Fig.14. Experimental results (a) output power vs input power (b) noise floor vs input power

It should be noted that the parasitic arising from mounting the packaged diode have been incorporated in the simulations. However, both the simulation and experiment show that the circuit is quite sensitive to the length of the transmission line between the diode circuit and output filter circuit, which is closely related to the mounting structure of the diode. Numerical electromagnetic analyzes the effects of the diode mounting structure should be done for better modeling of the hybrid SRD frequency multiplier. Therefore, the effects of diode mounting structure should not be neglected in more accurate analyzes. The 18th, 19th and 20th harmonics performance have been characterized by inserting various transmission line length between SRD multiplier and filter cascade combination. The measurement results are shown in Fig.15.
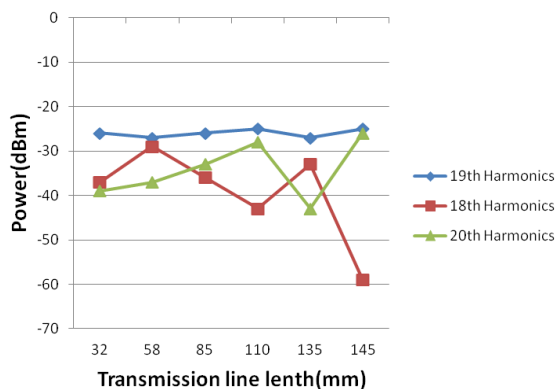

Fig.15 Output power vs transmission line length at18th, 19th and 20th harmonics.

Comparison between simulated and measured performance is shown in Table 1. The lower experimental results than the calculated is expected due to the loss of the circuit.

Results	Input Power	Harmonics		
	P_{in}	P_{out} @ 6.48GHz	P_{out} @ 6.84GHz	P_{out} @7.20GHz
Only SRD				
Simulation	21dBm	-25.21dBm	-22.67dBm	-27.35dBm
Measured	21dBm	-27.61dBm	-23.99dBm	-32.07dBm
SRD+Filter				
Simulation	21dBm	-35.21	-25.57	-34.74
Measured	21dBm	-35.25	-26.28	-38.88

Table1.Simulation vs measured results.

The photograph of impulse generator circuit with filter circuit is shown in Fig. 16.
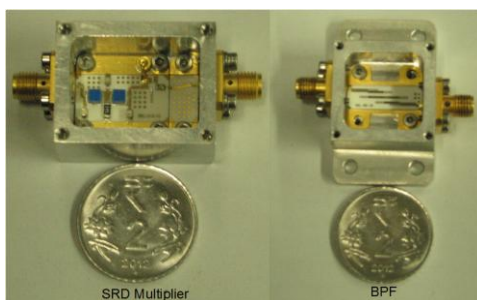

Fig. 16 shows the actual circuit board of SRD and BPF

V. CONCLUSION

The CAD of SRD frequency multipliers can be made more efficient and easier to accomplish by the method of reducing the nonlinearity of the SRD model in the simulation .The simple ADS model of a 360 MHz to 6.84 GHz multiplier predicted actual circuit operation accurately for an output frequency in the low microwave range using the generic ADS models for the SRD and all passive components. A parameter-extracted model of SRD is firstly created for DH543-62A, and its feasibility is verified by a test circuit. By varying the input power, the output power variation at 19th harmonics and spectral purity (noise floor) performance has been characterized for SRD based comb generators. The variation of transmission line length between SRD and output filter circuit that influence the 18th, 19th and 20th harmonic content are studied with simulation and experimental method. The experiment shows that the simulation results can be used to guide the SRD frequency multiplier design very well to achieve a good signal to noise ratio. In general, this design process could also be applied to CAD of circuits using other very strong nonlinear devices. By way of this circuit, we also easily fabricate frequency multipliers, as long as we go along match for single frequency we desire, and then connecting with a band pass filter. The advantages of this approach may include more flexible resolution setup, little hardware modification requirement and better spectrum energy utilization.

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