Design and Simulation of Three State Bootstrapped Sample and Hold Circuit

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***Abstract*— In modern era, the development of high resolution ADCs proves to be crucial task. The design of sample and hold circuit is also sensitive to the design of ADC. This paper describes the design of the three state bootstrapped sample and hold circuit which can be used for three levels of logic values in the Analog-to-digital converters. The simulation is done in HSPICE Synopsis Tool and is verified for performance improvement. The bootstrapped sample and hold circuit proves to be nearly 60% higher for power delay product.**

Keywords—ADCs; S/H circuits

I. INTRODUCTION

Analog-to-digital converters (ADCs) are very important building blocks in modern signal processing and communication systems. With advances in portable electronics, low power, high resolution and high speed ADCs are becoming more necessary. Most SAR ADCs (successive approximation register Analog-to-digital converters) are used in high resolution applications. Hence it is necessary to reduce power as low as possible. Normally *N*-bit single-ended SAR ADCs includes one sample/hold circuit, one charge redistribution DAC, one comparator, *N* normal switches and Digital control. Compared with a differential SAR ADC, the single-ended SAR ADC can save one sample/hold circuit and one DAC

The conversion process of a successive approximation ADC begins at the S/H circuit. In order to reduce overall power consumption in SAR ADCs the concentration in sample and hold circuits. Here in this paper clearly explained about the basic sample and hold circuits they are many types of sample and hold circuits CMOS S/H circuits, Open loop S/H circuits, Closed loop S/H circuits etc. The proposed Sample and hold circuit is a three states bootstrapped PMOS switch is used instead of Simple NMOS S/H circuits to reduce the switches on resistance, especially when the $V_r/2$ value is low. The proposed switch has three states: off, precharge and completely on these are the states which the switch is operating

In ADCs Sample and hold circuits Samples analog input signal and holds value between Samples analog input signal and holds value between clock cycles. Stable input value is required in many ADC-topologies. Reduces ADC-error caused by internal ADC delay variations. Sometimes referred to as Track and Hold (T/H) Sometimes referred to as Track and Hold (T/H).

Important parameters for S/H's

- Hold step: Voltage error during S/H-transition
- Signal isolation in hold mode
- Input signal tracking speed in sample mode
- Droop rate in hold mode: Small change in output voltage

In this paper, the three state bootstrapped switch is explained. The basic sample and hold circuits is presented in section II. The bootstrapped switch is presented in section III. The Results and discussion is presented section IV.

II. BASIC SAMPLE AND HOLD CIRCUITS

A sample-and-hold (S/H) circuit takes samples of its analog input signal and holds these samples in a memory element. The key feature of this circuit, when used as the front end of an ADC, is that it relaxes the timing requirements of the latter. This means that the precision and speed of the converter will be limited to a certain degree by the S/H circuit.

The most basic form of S/H circuit combines a switch and a capacitor. The operation of the circuit proceeds as follows. In sampling mode the switch is "on", creating a signal path that allows the capacitor to track the input voltage. When the switch is "off" an open circuit is created that isolates the capacitor from the input, hence changing the circuit from sampling mode into holding mode.The two most basic elements needed in a sampling circuit are the switch and a memory element. The switch allows the circuit to be configured into one of its two operating modes: sample and hold. In CMOS technology, the clear choice for the implementation of a switch is the MOS transistor. The basic S/H circuit is shown in fig.1.For data storage either voltage sampling or current sampling methods can be used [2]. The first method employs capacitors; the second employs inductors. However, in integrated circuit technology it is easier to fabricate capacitors than inductors [3]. Next, the operation of the MOS transistor as a switch is discussed.

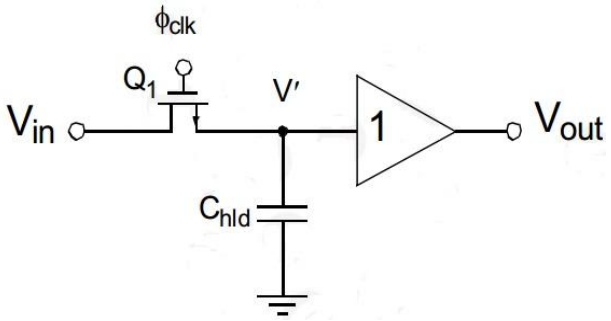

Fig. 1 MOS based S/H Circuit

The operation of S/H circuit is divided into two modes, sample and hold. Usually this is done at uniform time intervals, set by a periodic clock that divides circuit operation into two phases. During the sample-mode the output of the circuit can either track the input or reset to some fixed value. In the hold-mode, the output of the S/H circuit is equal to the input value obtained (sampled) at the end of the sample mode. Fig.2 (a) and (b) illustrate example waveforms for S/H circuit and a T/H (track-and-hold) circuit. Although here a distinction was made between sampling and tracking, the majority of the circuits are referred to as S/H circuits even though they behave as T/H circuits.

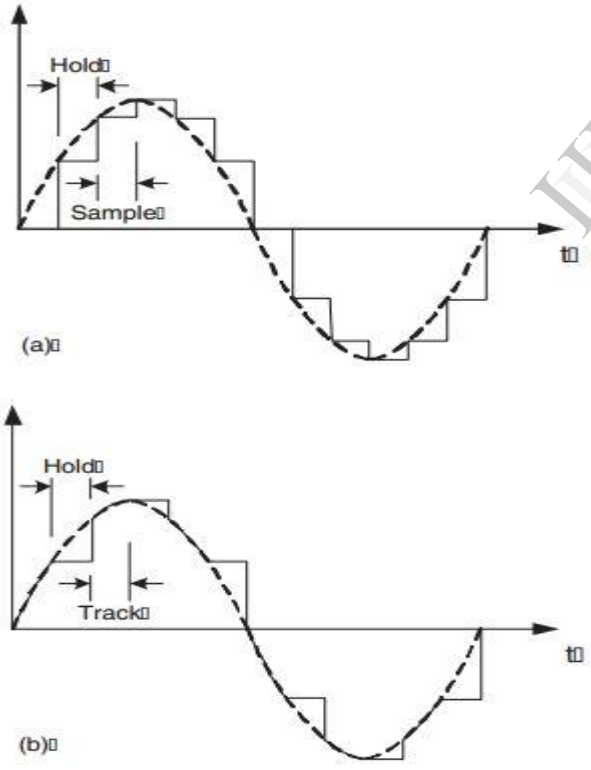

Fig. 2 (a) S/H circuit and (b) T/H circuit output waveforms.

A technique used to extend the input range of the sampling switch consists of using complementary transistors in parallel, so that at least one of the two transistors is "on" over the whole input-signal range while the switch on-resistance is maintained relatively constant [4]. In order to turn "on" or "off" both transistors simultaneously, complementary clock signals are applied at their gate terminals. This is shown in fig.3. Hence these are the basic sample and hold circuits generally using in the ADCs.

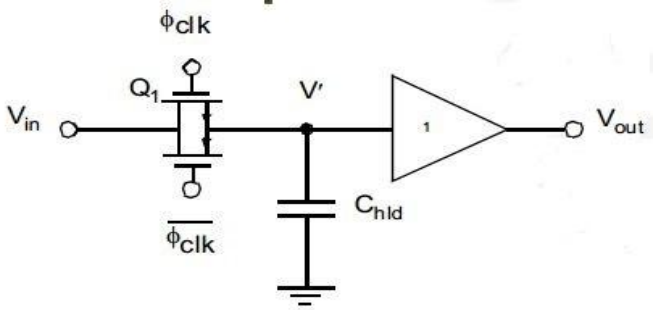

Fig.3 CMOS switch using complementary transistors.

III. THREE STATE BOOTSTRAPED SWITCH AS S/H CIRCUIT

The existing sample and hold circuits have disadvantages like they cannot be used to hold multilevel logic and they depend on the clock signal and do not have any reference voltage. The three state bootstrapped PMOS switch is shown in fig.4 is used to reduce the switch's on resistance.

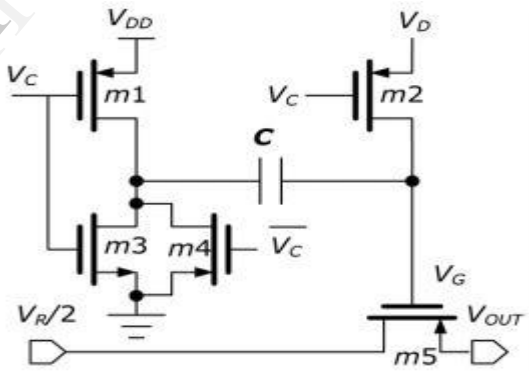

Fig.4. Three-state sample-and-hold switch main schematic

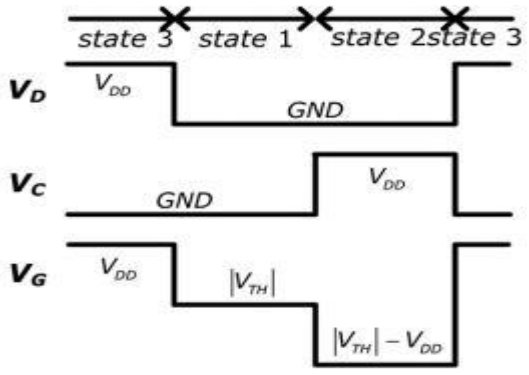

Fig.5.Timing diagrams, state 1: pre-charge; state 2: completely turns on; state 3: turns off.

The bootstrapped switch has three states: off state, precharge state and completely on state. This switch is different from the other bootstrapped switches that have only two states: off (precharge) and on [9]. The purpose of state 1 is to precharge the capacitor. The sampling mainly happens in the state 2 and the digitizing happens in the state 3.During state 1, V_C and V_D are GND and the transistor m2 is ON, while V_G is discharged through m2 to the voltage close to$|V_{TH}|$. At the same time, the left plate of the capacitor 'C' in Fig.4 is charged to V_{DD} by m1 and there is a voltage of V_{DD} - $|V_{TH}|$ across the capacitor. In the two state bootstrapped switch, the capacitor is precharged when the switch is off, so it does not need a separate phase to precharge the capacitor; therefore there should be only two phases.

In the state 2, V_C becomes V_{DD} so the transistor m1 and m2 are off while m3 and m4 are on. The left end of the capacitor is discharged to GND by m3 and m4. In this way, V_G is pushed down by the capacitor to the negative voltage equal to $-V_{DD} + |V_{TH}|$.

IV. RESULTS AND DISCUSSION

The simulation is carried out in HSPICE at 45nm technology. For the basic sample and hold circuit, the simulated waveform consisting of both input and output waveforms is shown in fig.6.

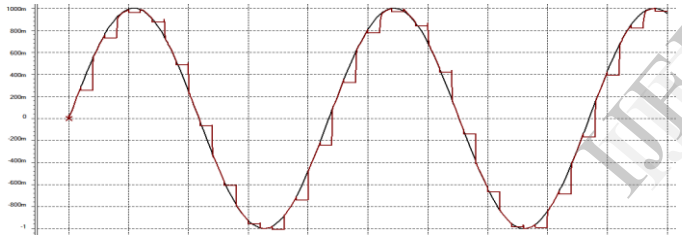

Fig.6 Simulation Results for MOS-Based S/H Circuits

From fig.6, it is clear that the sampling is done according to the signal amplitude variations without much delay. For CMOS based S/H circuit, the simulation results are shown in fig.7 where there is a deviation from the signal in terms of delay.

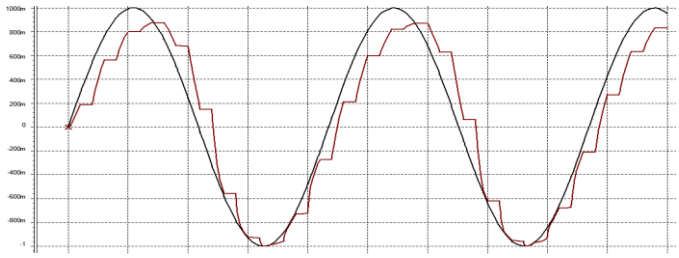

Fig.7 Simulation Results for CMOS-Based S/H Circuits

Fig.8 and fig.9 show the simulated waveforms for bootstrapped S/H circuit. Fig.8 shows the sampling and holding of input signal. Fig.9 shows the three states of the bootstrapped S/H Circuit.

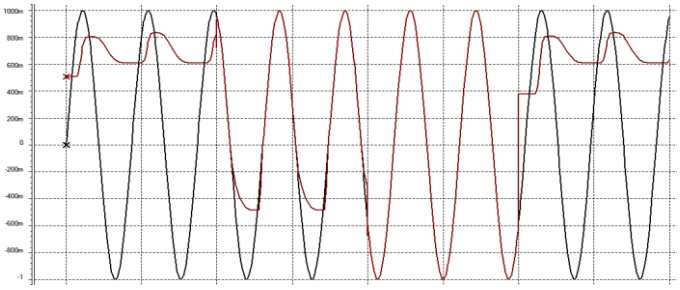

Fig.8 Simulation Results for bootstrapped S/H Circuits

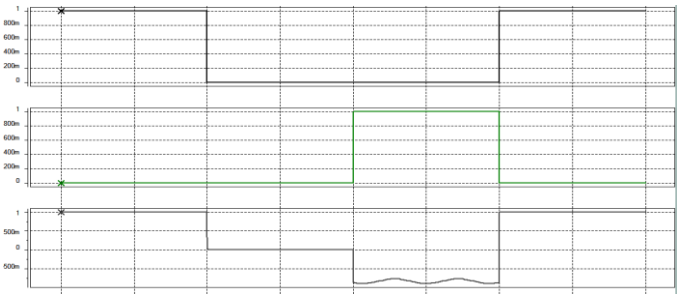

Fig.9. state 1: pre-charge; state 2: completely turns on; state 3: turns off.

TABLE-1

S.No	Comparison of various S/H circuits				
	S/H Name	***No.of. Transistors used***	***Power (mw)***	***Delay (ns)***	***PDP (nJ)***
1.	MOS Based S/H circuit	1	70.232	14.008	0.983
2.	CMOS Based S/H Circuit	2	42.769	16.640	0.712
3.	Three State bootstrapped switch	5	28.156	14.558	0.409

PDP = Power Delay*

CONCLUSION

Sample and Hold circuits are very important in ADCs. The three state bootstrapped switch is compared with existing S/H circuits. The reduction in power when compared to the existing sample and hold circuits was nearly 60%. From Spice simulations the PDP value of bootstrapped switch can reduce by nearly 60% of Basic S/H circuit. Hence the circuit is well suited for high resolution ADCs.

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