Design And Synthesis Of 32 BIT ALU Using Xilinx ISE V9.1i

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Abstract

The paper presents Design and Synthesis of 32-BIT Arithmetic Logic Unit (ALU). The design has been implemented using VHDL Xilinx Synthesis tool ISE 9.1i and targeted for Spartan device. ALU is designed to perform Arithmetic operations such as addition, subtraction, overflow; logical operations such as AND, OR, XOR, XNOR and NOT operations, Parity check, 1's and 2's complement operations, compare, etc. The ALU is a fundamental building block of the Central Processing Unit (CPU) of a computer, and even the simplest microprocessors contain one for purposes such as maintaining timers. The processors found inside modern CPUs and Graphics Processing Units (GPUs) accommodate very powerful and very complex ALUs; a single component may contain a number of ALUs. Flags like Zero, Carry and Odd Parity show the status of each Flag for result of the ALU's operation in each clock cycle. Zero Counter counts number of zeros in the result. The modern ALU must be capable to perform all the binary arithmetic and logical operations to meet the requirements of modern VLSI industry. So, the paper is a forward step to design the ALU and meets the demand of present FPGA based technology. The paper presents a number of new operations (Parity,Overflow,Zero,Zero counter etc.) that an ALU can perform than so far designed ALU in VHDL.

Keywords: 32 BIT ALU, VHDL,Network Interface Card, Processor

1. INTRODUCTION

Design of ALU in VHDL has been more complex to meet the requirements in terms of number of operations and fast operation and so it has been more efficient over the years. The number of operations performed by an ALU has been consistently increasing. ALU is a core component of all Processor and is an Integral part of the execution unit. The ALU performs the decision making operations (logical) and arithmetic operations. Arithmetic operations involve functions such as addition, subtraction, There are a variety of techniques to design these functions. It is most complex with regard to design, amongst all the components of the computer, and it also contributes to most of the delay. Thus, the design of the ALU is critical to the speed of the computer. The ALU can efficiently perform parity check to utilize it in Digital Systems. The faster adder can perform fast addition operation. The ALU is used in Network Interface Card (NIC) to maximize the throughput.

2. 32 BIT ARITHMETIC AND LOGIC UNIT

The 32 BIT ALU can perform advantageous Flag operations e.g. Parity, Carry, Overflow. The Flags play crucial role in Digital System Design. The 32 BIT ALU can perform advantageous Flag operations e.g. Parity, Carry, Overflow. The Flags play crucial role in Digital System Design. Parity Flag can detect the error and thus be used in Digital communication.

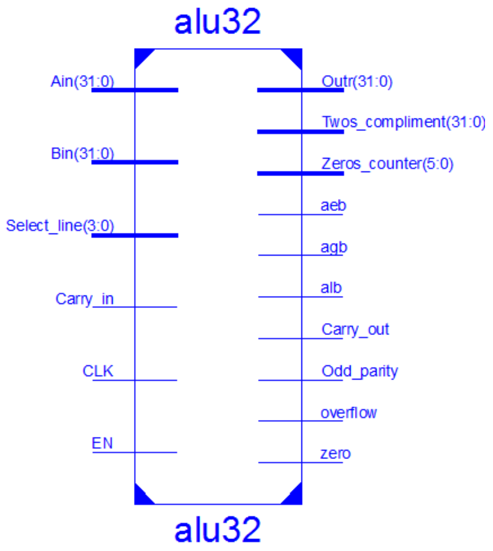

Fig.2.1: Entity 32 bit ALU

Design of Microprocessor through VHDL is importantly dependent over the efficiency of ALU design and synthesis. The less the delay propagation the more ALU is efficient to speed up digital signal operation. Software-based Programmable Network Interfaces excel in their ability to implement various services. These services can be added or removed in the network interface simply by upgrading the code in the system. However, programmable network interfaces suffer from instruction processing overhead. Programmable NICs must spend time executing instructions to run their software whereas ASIC based network interfaces implement their functions directly in hardware.

i). Design of Arithmetic Block:

The ALU can perform 32 BIT Addition and Subtraction operation and Overflow Logic will be HIGH if the result exceeds 32 BIT. Full Adders and Full Subtractor have been designed using Carry Ripple adder concept. Carry Flag show the result status whether output contains carry or not. Overflow Flag will be HIGH when 31st carry and 32nd bit of carry gets HIGH upon XOR operation. Zero Counter counts number of Zeros in the result (i.e. Outr).

ii).Design of Logic Block:

The Logic Block can perform all logical operations e.g. XOR,XNOR,NOR,NAND,AND,NOT,OR etc and generates Flags e.g. Parity, Carry, Zero if required.

iii).Design of Comparator

The ALU compares upon the two inputs and results either Ain>Bin, Ain<Bin or Ain=Bin. The Select Line (4 BIT) decides which operation is to be performed by the ALU e.g. XOR, NOR,NAND ,Addition, Subtraction etc. The Flags e.g. Parity, Zero etc are independent of Select Line. So, Flags will be HIGH or LOW in each clock cycle.

III. Table I

Select Line	Operation
0000	Ain AND Bin
0001	Ain OR Bin
0010	Ain AND (NOT Bin)
0011	Ain XNOR Bin
0100	NOT Bin
0101	Ain NAND Bin
0110	Ain NOR Bin
0111	XNOR
1000	NOT(Ain XNOR Bin)
1001	NOT(Ain NAND Bin)
1010	NOT (Ain NOR Bin)
1011	Carry Ripple Adder, Carry, Overflow
1100	Carry Ripple Subtractor, Carry, Overflow
1101	32bit Adder
1110	32bit Subtractor
1111	Ain NOR (NOT Bin)

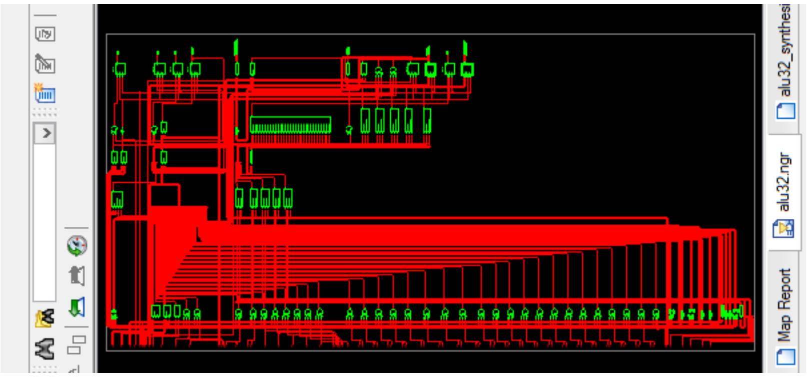

Fig.2.2RTL Schematic

2. Simulation:

Simulation of Behavioral Model for 32 BIT ALU has been performed for 1000 nano-seconds. Each Clock(CLK) cycle has 50 ns rise and fall time. Input Setup time:5 ns, Output Valid delay:3 ns;
The simulation of 32-BIT ALU(if rising_edge(CLK) and EN=’0’) generated from Testbench Waveform is given in figure 2.1 below:

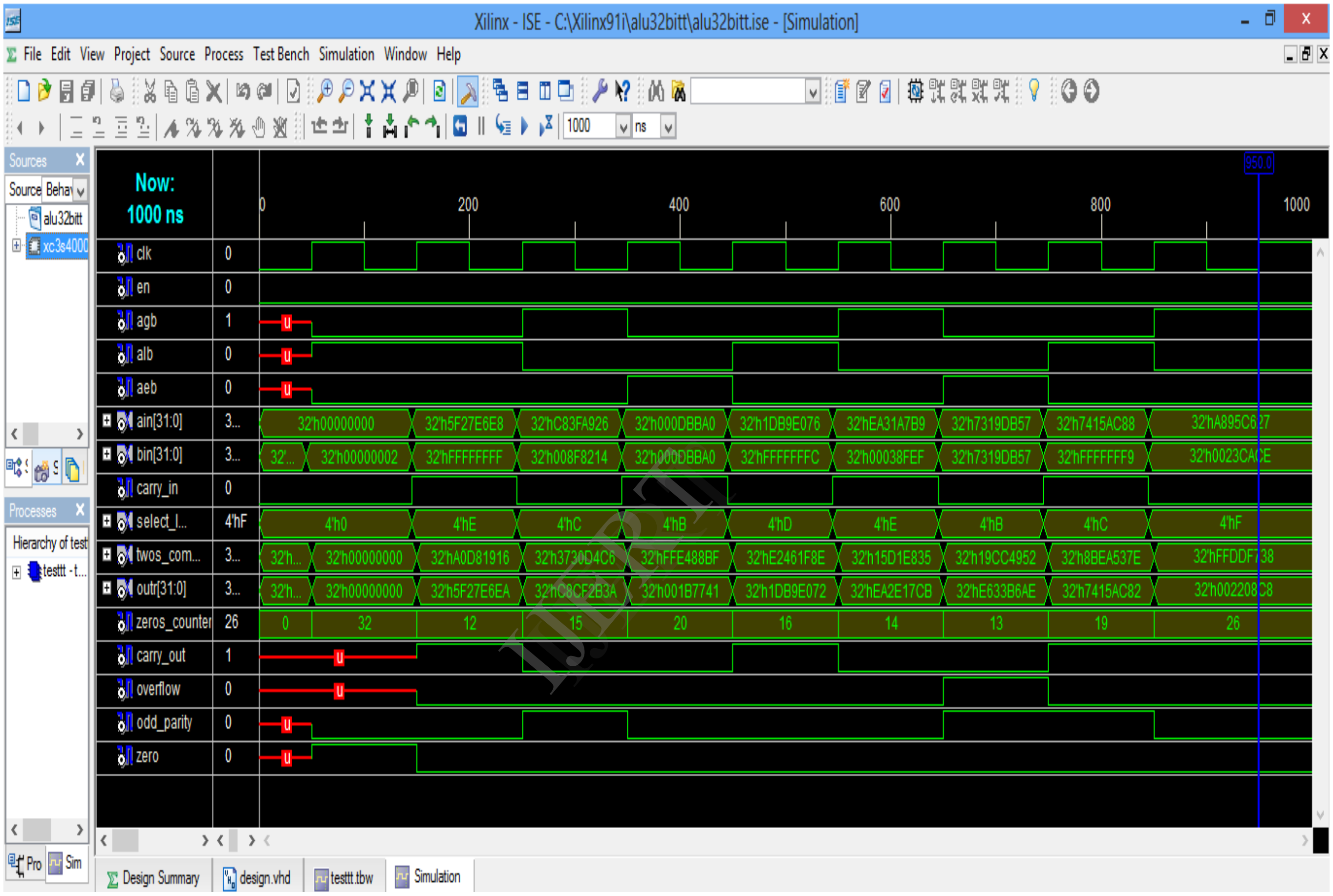
Xilinx - ISE - C:\Xilinx91i\alu32bitt\alu32bitt.ise - [Simulation]
File Edit View Project Source Process Test Bench Simulation Window Help
1000 ns
Sources
alu32bitt
xc3s4000
Processes
Hierarchy of testt
testtt
Now: 1000 ns
0 200 400 600 800 1000
950.0
clk 0
en 0
agb 1
alb 0
aeb 0
ain[31:0] 3... 32'h00000000 32'h5F27E6E8 32'hC83FA926 32'h000DBBA0 32'h1DB9E076 32'hEA31A7B9 32'h7319DB57 32'h7415AC88 32'hA895C627
bin[31:0] 3... 32'... 32'h00000002 32'hFFFFFFFF 32'h008F8214 32'h000DBBA0 32'hFFFFFFFC 32'h00038FEF 32'h7319DB57 32'hFFFFFFF9 32'h0023CACE
carry_in 0
select_l... 4'hF 4'h0 4'hE 4'hC 4'hB 4'hD 4'hE 4'hB 4'hC 4'hF
twos_com... 3... 32'h... 32'h00000000 32'hA0D81916 32'h3730D4C6 32'hFFE488BF 32'hE2461F8E 32'h15D1E835 32'h19CC4952 32'h8BEA537E 32'hFFDDF738
outr[31:0] 3... 32'h... 32'h00000000 32'h5F27E6EA 32'hC8CF2B3A 32'h001B7741 32'h1DB9E072 32'hEA2E17CB 32'hE633B6AE 32'h7415AC82 32'h002208C8
zeros_counter 26 0 32 12 15 20 16 14 13 19 26
carry_out 1
overflow 0
odd_parity 0
zero 0
Design Summary
design.vhd
testtt.tbw
Simulation

Fig.2. Testbench Simulation

3.Synthesis and Implementation Report (XILINX ISE v9.1i):

The Synthesis and Implimentation Reports have been generated by XILINX ISE v9.1i for the Behavioral model of 32 BIT ALU are given below:

3.1 Advanced HDL Synthesis:

Macro Statistics

# Adders/Subtractors: 35

1-bit adder carry out	: 1
2-bit adder	: 1
2-bit adder carry out	: 1
3-bit adder	: 3
3-bit adder carry out	: 1
32-bit adder	: 1
33-bit adder	: 1
33-bit adder carry in	: 1
33-bit subtractor	: 1
4-bit adder	: 7
4-bit adder carry out	: 1
5-bit adder	: 15
5-bit adder carry out	: 1

# Registers: 44	
Flip-Flops	: 44
# Comparators	**: 2**
32-bit comparator greater	: 1
32-bit comparator less	: 1
# Multiplexers	**: 3**
1-bit 16-to-1 multiplexer	: 2
32-bit 16-to-1 multiplexer	: 1
# Xors	**: 38**
1-bit xor2	: 3
1-bit xor3	: 33
1-bit xor32	: 1
32-bit xor2	: 1

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3.2 Timing Summary:

Speed Grade: -4
Minimum period: 2.377ns (Maximum Frequency: 420.698MHz)
Minimum input arrival time before clock: 62.522ns
Maximum output required time after clock: 12.314ns

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3.3 The Delay Summary Report:

The NUMBER OF SIGNALS NOT COMPLETELY ROUTED for this design is: 0
The AVERAGE CONNECTION DELAY for this design is: 3.480 nano-seconds
The MAXIMUM PIN DELAY IS: 11.932 nano-seconds
The AVERAGE CONNECTION DELAY on the 10 WORST NETS is: 7.830 nano-seconds

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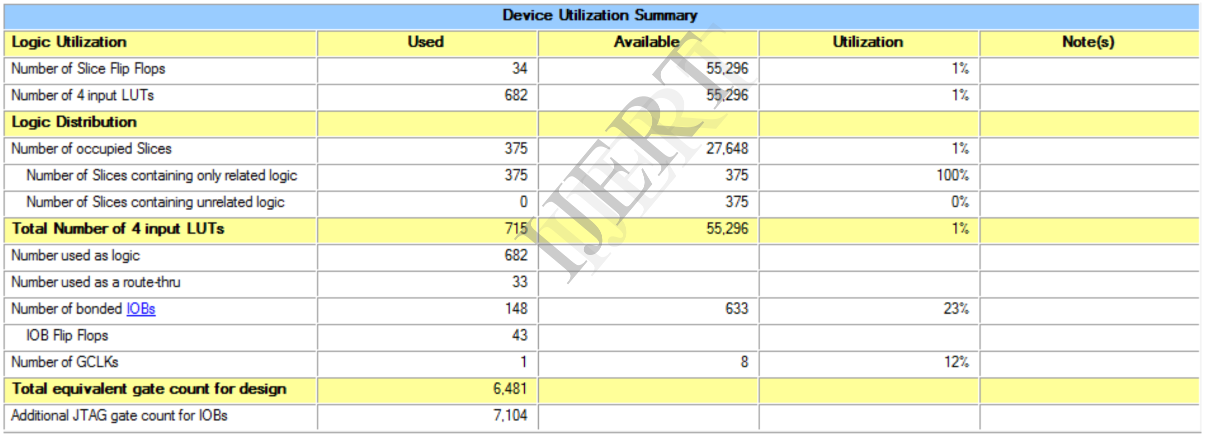

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	34	55,296	1%	
Number of 4 input LUTs	682	55,296	1%	
Logic Distribution				
Number of occupied Slices	375	27,648	1%	
Number of Slices containing only related logic	375	375	100%	
Number of Slices containing unrelated logic	0	375	0%	
Total Number of 4 input LUTs	715	55,296	1%	
Number used as logic	682			
Number used as a route-thru	33			
Number of bonded IOBs	148	633	23%	
IOB Flip Flops	43			
Number of GCLKs	1	8	12%	
Total equivalent gate count for design	6,481			
Additional JTAG gate count for IOBs	7,104			

Fig.3. Design Utilization Summary

Conclusion:

The paper "Design and Synthesis of 32 BIT ALU using Xilinx ISE Design Suite v9.1i" we have designed and implemented a 32 bit ALU. Arithmetic Logic Unit is a part of digital system that performs arithmetic computations, such as Addition and Subtraction, Parity, Comparator, Overflow and all sorts of basic logical operations(NAND,NOR,XOR,AND,OR). The ALU is one component of the CPU (Central Processing Unit) and used in various work. Here all the above mentioned operations are then verified by Xilinx IES Design Suitev9.1i to see whether they match theoretically or not. The above given waveforms show that they match completely thereby verifying our results.

Acknowledgement

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