Design and Verification Eight Port Router for Network on Chip

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ABSTRACT`: Multiprocessor system on chip is emerging as a new trend for System on chip design but the wire and power design constraints are forcing adoption of new design methodologies. Researchers pursued a scalable solution to this problem i.e. Network on Chip (NOC). Network on chip architecture better supports the integration of SOC consists of on chip packet switched network. Thus the idea is borrowed from large scale multiprocessors and wide area network domain and envisions on chip routers based network. Cores access the network by means of proper interfaces and have their packets forwarded to destination through multichip routing path. In order to implement a competitive NOC architecture, the router should be efficiently design as it is the central component of NOC architecture. Design And Verify the functionality of the "Design and Verification Eight Port Router for Network on Chip" IP core using the latest verification methodologies, Hardware Verification Languages and EDA tools and qualify the IP for Synthesis an implementation.

Introduction

My research is based on the paper" **router design for network on chip".** Now in this paper I have designed a eight port router which is the advancement for the previous four port router network.But in the four port network we have the ability to connect a network of four systems which is limited.Now I extended this network upto 8 ports and I observed the results using verilog HDL.

The challenge of the verifying a large design is growing exponentially. There is a need to define new methods that makes functional verification easy. Several strategies in the recent years have been proposed to achieve good functional verification with less effort. Recent advancement towards this goal is methodologies. The methodology defines a skeleton over which one can add flesh and skin to their requirements to achieve functional verification. OVM (open verification methodology) is one such efficient methodology and best thing about it is, it is free. This ovm is built on system Verilog and used effectively to achieve maintainability, reusability, speed of verification etc. This project is aimed at building a reusable test bench for verifying 8 Port Router Protocol Bridge by using system Verilog and ovm

In this document the use of vmm and system Verilog to verify a design and to develop a reusable test bench is explained in step by step as defined by verification principles and methodology. The test bench contains different components and each component is again composed of subcomponents, these components and subcomponents can be reused for the future projects as long as the interface is same.

Router:

System on chip is a complex interconnection of various functional elements. It creates communication bottleneck in the gigabit communication due to its bus based architecture. Thus there was need of system that explicit modularity and parallelism, network on chip possess many such attractive properties and solve the problem of communication bottleneck. It basically works on the idea of interconnection of cores using on chip network.

The communication on network on chip is carried out by means of router, so for implementing better NOC , the router should be efficiently design. This router supports four parallel connections at the same time. It uses store and forward type of flow control and Fsm Controller deterministic routing which improves the performance of router. The

switching mechanism used here is packet switching which is generally used on network on chip.

In packet switching the data the data transfers in the form of packets between cooperating routers and independent routing decision is taken. The store and forward flow mechanism is best because it does not reserve channels and thus does not lead to idle physical channels. The arbiter is of rotating priority scheme so that every channel once get chance to transfer its data. In this router both input and output buffering is used so that congestion can be avoided at both sides.

A router is a device that forwards data packets across computer networks. Routers perform the data "traffic direction" functions on the Internet. A router is a microprocessor-controlled device that is connected to two or more data lines from different networks. When a data packet comes in on one of the lines.the router reads the address information in the packet to determine its ultimate destination. Then, using information in its routing table, it directs the packet to the next network on its journey.

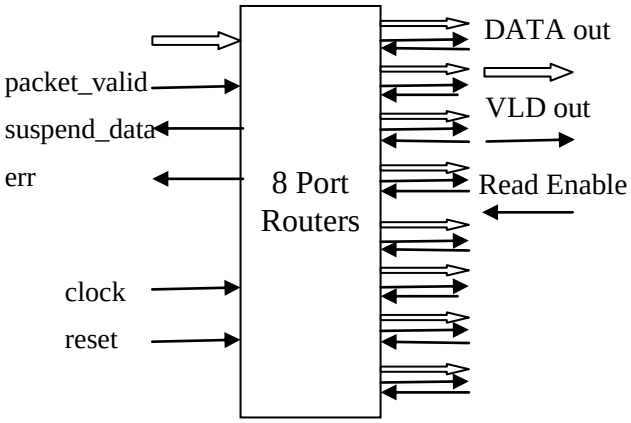
The router is a ” **Eight Port Network Router**” has a one input port from which the packet enters. It has seven output ports where the packet is driven out. Packet contains 3 parts. They are Header, data and frame check sequence. Packet width is 8 bits and the length of the packet can be between 1 bytes to 64 bytes. Packet header contains three fields DAand length.Destination address(DA) of the packet is of 8 bits. The switch drives the packet to respective ports based on this destination address of the packets. Each output port has 8-bit unique port address. If the destination address of the packet matches the port address, then switch drives the packet to the output port, Length of the data is of 8 bits and from 0 to 63. Length is measured in terms of bytes. Data should be in terms of bytes and can take anything. Frame check sequence contains the security check of the packet. It is calculated over the header and data.

Router is a packet based protocol. Router drives the incoming packet which comes from the input port to output ports based on the address contained in the packet

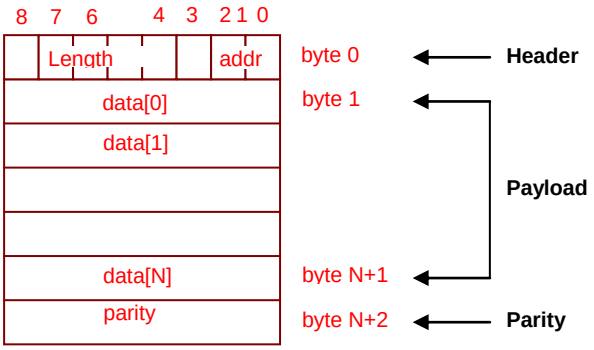
The router has a one input port from which the packet enters. It has three output ports where the packet is driven out. The router has an active low synchronous input resetn which resets the router.

.Data packet moves in to the input channel of one port of router by which it is forwarded to the output channel of other port. Each input channel and output channel has its own decoding logic which increases the performance of the router. Buffers are present at all ports to store the data temporarily.

The buffering method used here is store and forward. Control logic is present to make arbitration decisions. Thus communication is established between input and output ports.. According to the destination path of data packet, control bit lines of FSM are set. The movement of data from source to destination is called switching mechanism The packet switching mechanism is used here, in which the flit size is 8 bits .Thus the packet size varies from 0 bits to 8 bits. A detailed explanation of Design is as follow

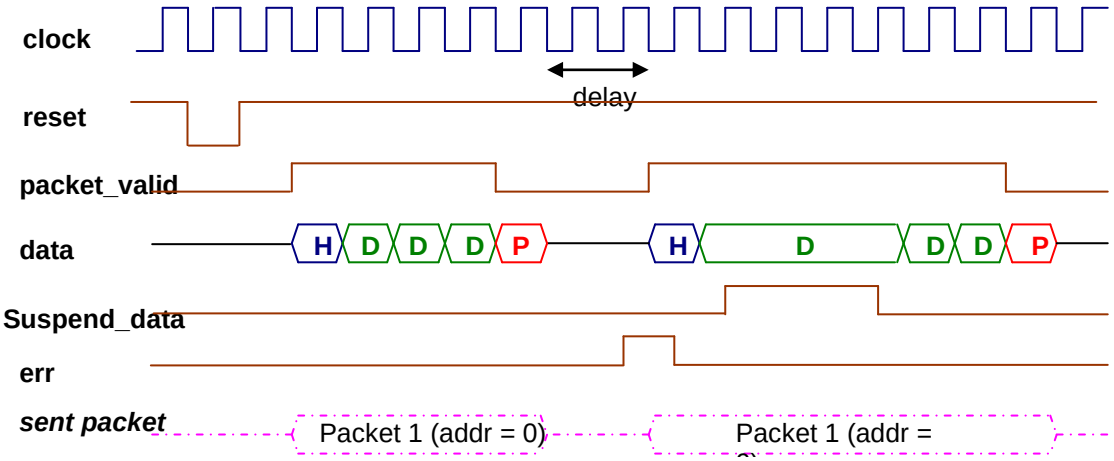


Block Diagram Of Eight Port Router



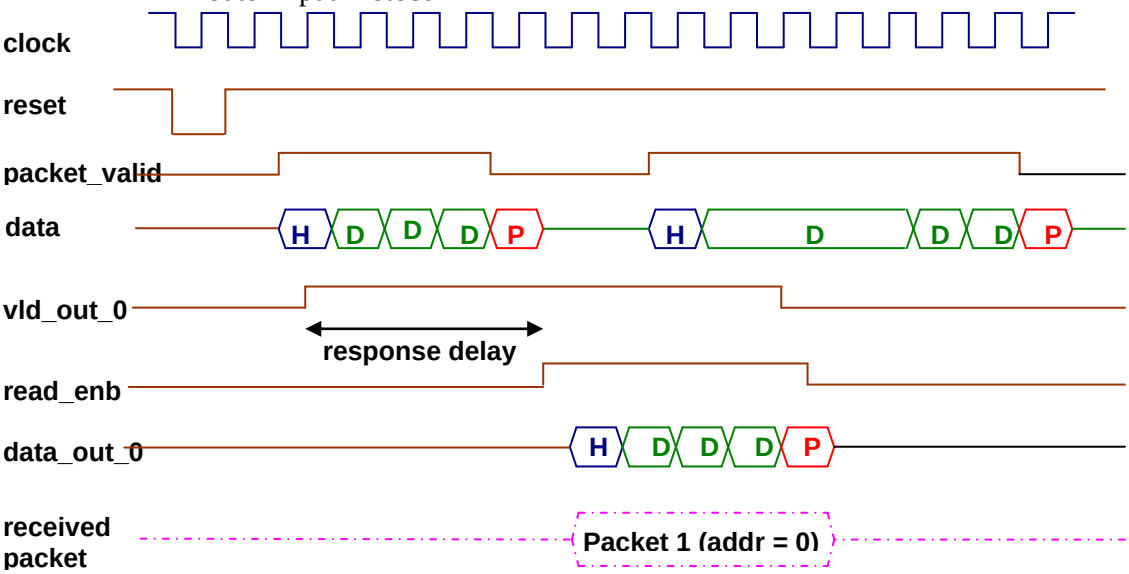
Data Packet Format

Data registers latches the data from data input based on state and status control signals, and this latched data is sent to the fifo for storage. Apart from it, data is also latched into the parity registers for parity calculation and it is compared with the parity byte of the packet. An error signal is generated if packet parity is not equal to the calculated parity



H = **H**eader, D = **D**ata, P = **P**arity

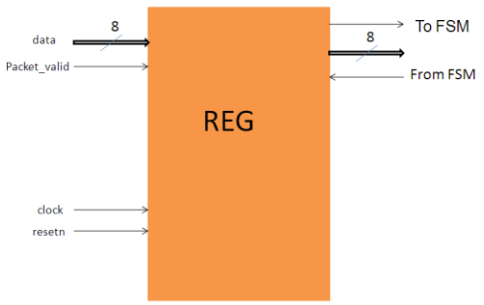
Router Input Protocol



Router output Protocol

Register Block:

This module contains status, data and parity registers required by router. All the registers in this module are latched on rising edge of the clock.



Router Output Block

There are 7 fifos used in the router design. Each fifo is of 8 bit width and 16 bit depth.

The fifo works on system clock. It has synchronous input signal reset.

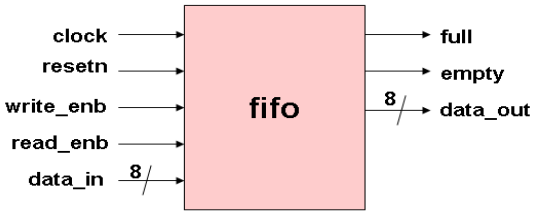
If resetn is low then full =0, empty = 1 and data_out = 0

The FIFO has doing 7 deferent operations

- Write Operation
- Read operation

Read and Write Operation

The functionality of FIFO explain Below



Four port Router FIFO

Write operation:

The FIFO write operation is done by when the data from input data_in is sampled at rising edge of the clock when input write_enb is high and fifo is not full.in this condition onaly FIFO Write operation is done.

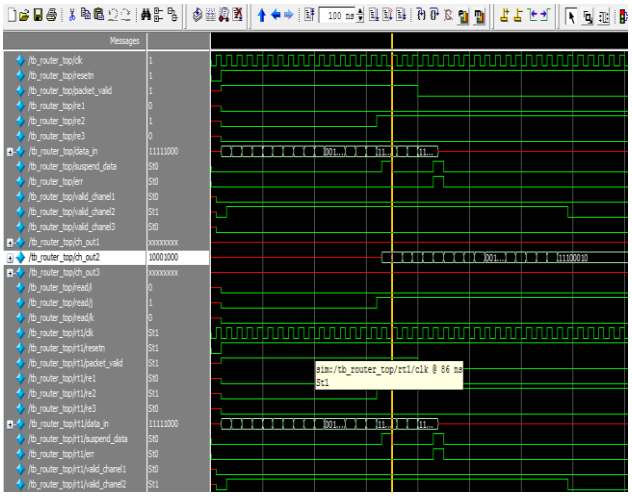
Read Operation:

The FIFO Read Operation is The data is read from output data_out at rising edge of the clock, when read_enb is high and fifo is not empty.

Read and Write operation can be done simultaneously.

Full – it indicates that all the locations inside fifo has been written.

Empty – it indicates that all the locations of fifo are empty.



8 Port Router Output

Conclusion

As the functional verification decides the quality of the silicon, we spend 60% of the design cycle time only for the verification/simulation. In order to avoid the delay and meet the TTM, we use the latest verification methodologies and technologies and accelerate the verification process. This project helps one to understand the complete functional verification process of complex ASICs an SoC's and it gives opportunity to try the latest verification methodologies, programming concepts like Object Oriented Programming of Hardware Verification Languages and sophisticated EDA tools, for the high quality verification.

In this Four Port Router project I Design and verified the functionality of Router with the latest Verification methodology i.e.,System Verilog and observed the code coverage and functional coverage of Router by using coverpoints ,cross and different test cases like constrained, weighted and directed testcases.By using these testcases I improved the functional coverage of Router. In this I used one master and eight slaves to monitor the Router.Thus the functional coverage of Router was improved.

The results shows that System Verilog methodology can be used to make reusable test benches successfully. Large part of the test bench is made reusable over multiple projects.even though this reusablity is limited to the interfaces. A large class of devices that are build on these inerfaces can be verified successfully. Once these components are

made the amount of time required to build test benches for other projects can be reduced a lot.

References

- Verilog HDL- Digital Design and Synthesis, by Samir Palnitkar
- Open Cores project site http://www.opencores.org..
- CISCO Integrated Services Router –SRND(Solution Reference Network Design) document
- NORTEL ISP Router Design document.
- VMM User guide
- VMM Reference manual
- System Verilog for verification by Chris Spear
- Router for NOC by Michael K. Papamichael
- Writing test benches using system Verilog by Janick Bergeron
- OVM Cook book
- OVM Reference manual

Websites

- www.testbench.in
- www.ovmworld.org
- www.systemverilog.org
- www.cisco.com/go/isr
- www.vmmcentral.com