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Design & Implementation of Embedded Logic Flip-Flop in 180nm Technology

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***Abstract*—This paper introduces a novel high performance flip-flop capable of incorporating logic functions. The proposed Embedded Logic flip-flop (ELFF) has a hybrid flip-flop architecture that combines the merits of both static and dynamic flip-flop structures. Incorporating logic function with-in flip-flop will reduce layout area, delay and power dissipation. Merging of logic functions with flip-flop allows the elimination of one gate delay from a critical path in sequential circuit design. ELFF is provided with an asynchronous reset, which can capable in easy implementation of counters and registers. The proposed ELFF has 20% better performance in terms of power dissipation and delay compared to existing DDFF-ELM. This Flip-flop will be a good component to include in standard cell library for designing VLSI chips for high performance and low power applications. The performance comparisons and analysis are done with Mentor Graphics EDA tool in the TSMC 180nm process.**

***Index Terms*—flip-flop, low power, high speed, embedded logic, ELFF, hybrid**

I. INTRODUCTION

The trend in VLSI technology scaling in the last few years shows the number of on-chip transistors increasing in every year. Although the supply voltage is scaled down, meanwhile the power consumption of VLSI chips is increasing continuously. The deep sub-micron CMOS technology has evolved during the past few years. For the design of high performance VLSI systems, the choice of backend methodology has huge importance in optimization of various design matrices. Standard cell libraries are so useful in the design of high performance VLSI chips. The standard cell library consists of several individual cells, which can capable of performing different logic functionality. These standard cells are different in size and performance. Flip-flop is an important component in every standard cell library. It is because of its importance in the synchronous circuit design. Flip-flops and latches are basic elements in the design of VLSI circuits. One flip-flop can store one bit of data.

In synchronous systems, high speed processing is achieved through deep pipelining. Flip-flops are an important component for achieving this. The latency associated with the pipelining is based on the Data to Output (D to Q) delay in a flip-flop. CMOS flip-flop can be of static or dynamic design styles, depending on how it retains its values against charge leakage. Several researches are going on for the improvement in the speed of operation of flip-flops. The primary difference between latches and flip-flops is that, for latches, their content changes continuously as long as they are enabled. On the other hand, for flip-flops, their content changes only either at rising or falling edge of enable signal. In flip-flop the controlling signal is used as the enable signal. After the rising or falling edge of the clock flip-flop content remains constant even if the input changes. According to the requirement of the system, the designer has to consider all the parameters such as speed, power consumption, area and noise stability, while choosing a flip-flop structure. What makes the decision harder is that, none of these parameters are independent from each other. Multidimensional optimization should be required in the design of high performance systems.

In the design of sequential circuit, a major challenge is to design a D flip-flop. A large number of various flip-flop architectures are published in the past few years. This study is to explore the performance comparison on various D flip-flops. The flip-flops considered for analysis are Hybrid-Latch flip-flop (HLFF), Semi-dynamic flip-flop (SDFF), conditional data mapping flip-flop (CDMFF), Cross charge control flip-flop (XCFF) and Dual Dynamic pulsed flip-flop (DDFF). The DDFF have the lowest number of transistors (18 transistors), which is 10% lesser compared to other hybrid structures. The DDFF have better Power-Delay-Area Product (PDAP). Compared to HLFF, DDFF has 45% better PDAP [8]. DDFF has the capability of incorporating logic functions and lower Power-Delay-Area product. So this flip-flop structure is a good component for the designing of a flip-flop featuring embedded logic functions. The main motivation for this paper is to incorporating logic function with-in flip-flop will reduce layout area; delay and power dissipation. It will be a good component to include in standard cell library. A revised structure of DDFF is used to design the proposed ELFF.

The details of the flip-flop architectures used for this study are given in the Section II. The existing Flip-flop designs capable of logic functions are given in the Section III, Details of the Proposed ELFF is given in Section IV and Performance Analysis is given in section V.

II. FLIP-FLOP TOPOLOGIES

CMOS flip-flop can be of static or dynamic design styles, depending on how it retains its values against charge leakage. A static flip-flop retains its value using positive feedback, while dynamic flip-flop requires continuous refreshment of charges. Static flip-flops can preserve their stored value even if the clock is stopped. While in dynamic flip-flop, the stored value will be lost even if it is not refreshed for a while. Static design style includes master slave designs such as TGMS flip-flop, PowerPC 603 MS latch Flip-flop etc... Static flip-flop requires large and positive setup time.

A second category of the flip-flop is a dynamic flip-flop. Basically, dynamic flip-flops can achieve high speed and low power dissipation. But they suffer from serious potential failures. Due to higher leakage current and power supply noise, the stored charge may lose. In dynamic flip-flops, the setup time is negative. So it has a lower D to Q delay. The sum of clock to Q delay and set up time comprises of the D to Q delay. Semi-dynamic and purely dynamic flip-flops come under this. TSPC latch flip-flop is purely dynamic flip-flop. The hybrid flip-flops come under semi-dynamic design style. Semi dynamic flip-flops have combined the advantages of both static and dynamic flip-flop architectures. The discharge of dynamic node is due to reverse leakage current in NP junctions and sub-threshold leakage in MOS transistors. The sub- threshold voltage varies exponentially with gate-source outages in pass gate transistors. Most dynamic flip-flops can be converted into static flip-flops by using keeper transistors at the dynamic nodes. The flip-flop circuits extracted from references were built using mentor graphics EDA tool. The following is a short description of the flip-flop circuits.

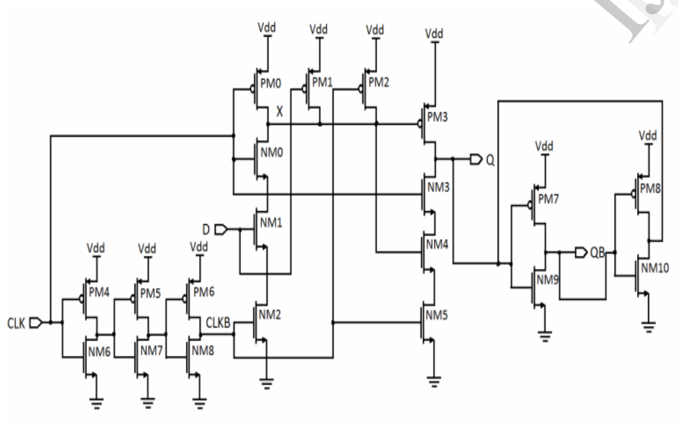

Fig 1: Hybrid Latch Flip-flop

Hybrid Latch Flip-flop (Fig 1) is a classic high performance flip-flop with hybrid architecture [2]. This hybrid structure combines advantages of both static and dynamic design styles. It has a dynamic front end and static output. An internally generated pulse signal is used for clocking this flip-flop. The pulse is generated from a clock and delayed clock using three cascaded inverters. Patrovi et al. implemented HLFF which has a large stack of NMOS transistors, makes operation slower. Klass et al. implemented Semi dynamic flip-flop (Fig 2), which is also a classic high performance flip-flop with hybrid architecture [3]. This flip-flop is also called fast flip-flop. This structure doesn't have a stack with large number of NMOS transistors, so it will be faster than HLFF. SDFF is capable of incorporating logic functions within the flip-flop. Unnecessary internal node transitions are present in SDFF. 1-1 glitch created due to the short circuit path from Q to ground at rising edge of clock will consumes more power.

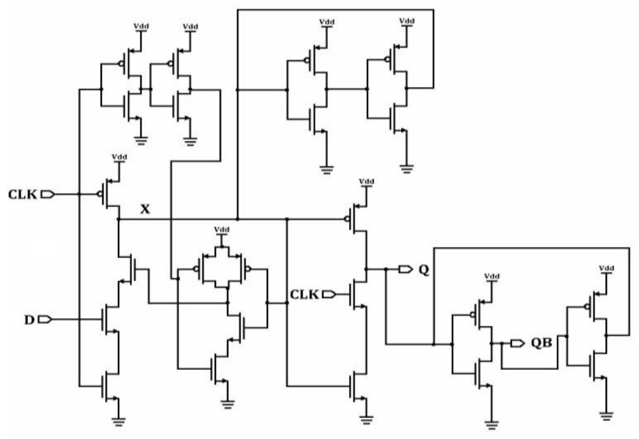

Fig 2: Semi dynamic flip-flop

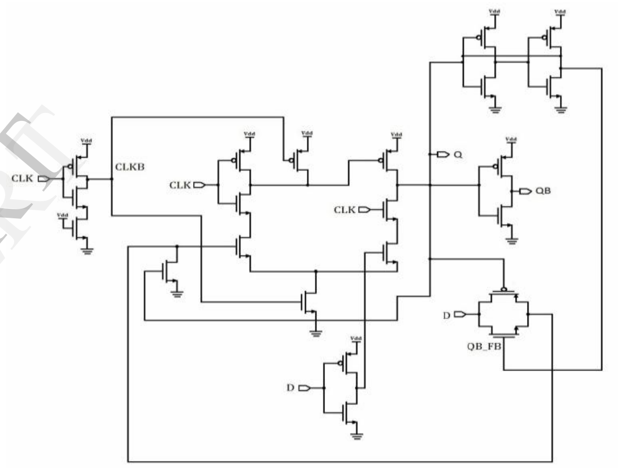

Fig 3: Conditional Data Mapping flip-flop

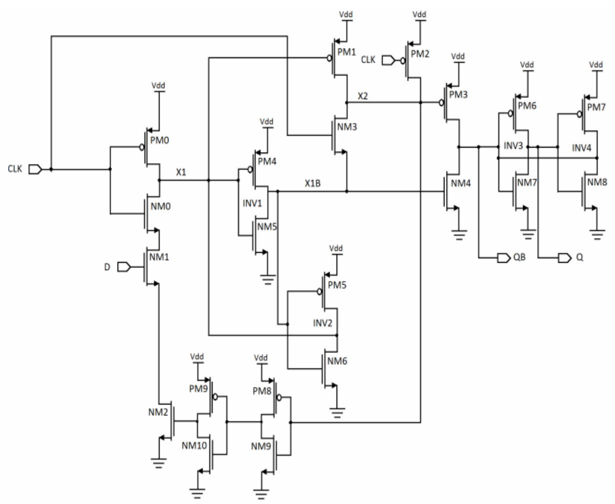

Fig 4: Cross Charge Control Flip-flop

The major sources of power consumption in flip-flop in hybrid designs are due to redundant data transitions and large pre-charge capacitance. Many attempts are made to reduce these problems. The Conditional Data Mapping flip-flop (Fig 3) is one of the most efficient flip-flops which reduce the data transitions. It uses an output feedback data to the flip-flop [4], [5], [6]. So the data transitions are reduced. Thereby the power consumption is reduced. The presence of a stack of 3 nMOS transistors at the output node and presence of conditional logic structure will increase the hold time. So the D to Q delay gets increased. Also, this CDMFF has a bulky structure due to the presence of conditional elements. The Cross Charge Control Flip-flop (Fig 4) is implemented in Hirata et al., which reduces the pre-charge capacitance problem in hybrid flip-flop architectures [7]. The output pull-up and pull-down nodes are driven by the pre-charge node. These transistors drive large output loads, which contribute the most of the capacitance at the output node. Through splitting this node into two dynamic nodes will reduce the pre-charge capacitance. Here the power dissipation is reduced. One of the disadvantages of this design is the redundant pre-charge capacitance at dynamic nodes.

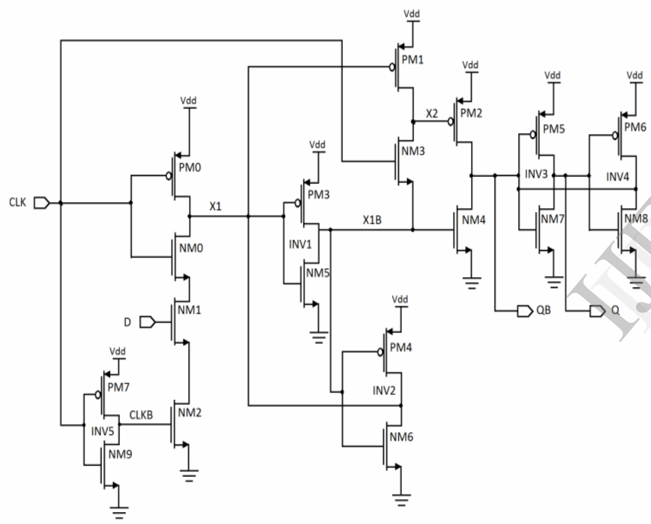

Fig 5: Dual Dynamic Node Hybrid Flip-flop

The Dual Dynamic Node Hybrid Flip-flop (Fig 5) is implemented in Absel et al. which is similar to XCFF, which have two dynamic internal nodes. These nodes drive the output pull-up and pull-down nodes separately. Since one of the dynamic nodes is switched on during one clock cycle. So the power consumption gets reduced. This flip-flop is capable of embedding logic functions with-in the flip-flop. An unconditional shut-off mechanism is provided at the dynamic front-end.

III. EXISTING DESIGNS

Not too many attempts have been made to design a flip-flop with logic capability. SDFF is the classical hybrid flip-flop which can capable of incorporating logic functions within the flip-flop. The logic functions are incorporated in the dynamic front-end. The discrete arrangement of a flip-flop and MUX logic is shown in fig 6. Merging of logic functions allows the elimination of one gate delay from the critical path. Thereby the entire delay will be reduced. Also the transistor count gets reduced. ELFF is a fast and small implementation compared to discrete combination of static logic and a flip-flop. The SDFF with embedded logic capability (SDFF-ELM) is shown in fig 7. The DDFF-ELM without reset logic is shown in fig 8. ELFF has better performance in terms of power dissipation and delay compared to existing DDFF-ELM structure. This Flip-flop will be a good component to include in standard cell library for designing VLSI chips for high performance applications.

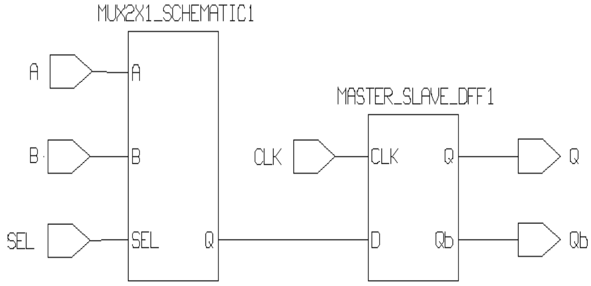

Fig 6: Discrete Combination of Logic and Flip-flop

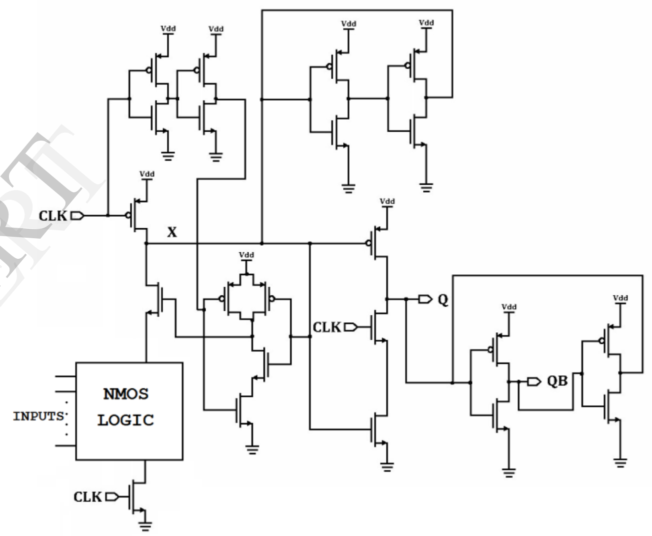

Fig 7: SDFF with embedded logic

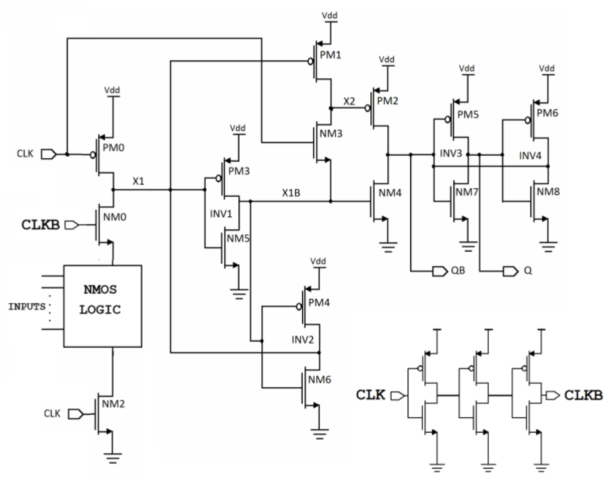

Fig 8: DDFF – ELM

IV. PROPOSED ELFF

The structure of the proposed Embedded Logic Flip-flop (ELFF) is given in Fig 9. It is a revised structure of DDFF-ELM. The inverter pairs of DDFF-ELM are replaced with a NAND based reset-circuit. When "rst" signal is held low for a particular period of time, then the node X1 is pulled high and output Q is pulled low by the respective reset circuits. The proposed ELFF design has the ability to incorporate logic functions within the flip-flop. The circuit for ELFF 2×1 MUX is shown in Fig 10.

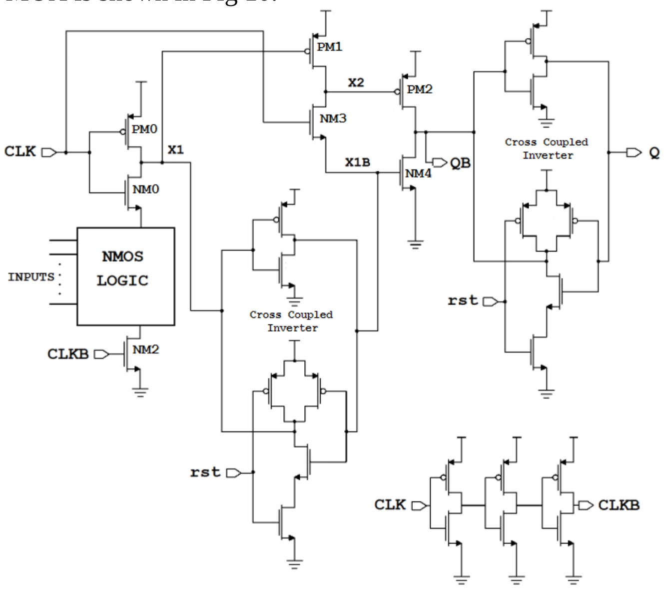

Fig 9: Proposed ELFF with asynchronous reset

The operation of the ELFF can be divided into two phases: evaluation phase and pre-charge phase. CLK is high at evaluation phase and low at the pre-charge phase. The actual latching occurs during the CLK and CLKB's 1–1 overlap during the evaluation phase. If nMOS logic provides a discharge path for node X1 to ground through NM2 prior to this overlap period, this changes the state of the first cross coupled inverter with reset logic. This causes node X1B to go high. Then the output QB is discharged through NM4. The first cross coupled inverter with reset logic keeps the low level at the node X1 for the rest of the evaluation phase. Thus the node X2 is held high during the entire evaluation period by the pMOS transistor PM1. When the CLK becomes low, the circuit enters to pre-charge phase. Then the node X1 is pulled high through PM0, switching the state of first cross coupled inverter with reset logic. During this time, node X2 is not driven by any transistor, and then it holds the charge dynamically. The outputs at node QB maintains their voltage level through second cross coupled inverter with reset logic. If nMOS logic will not give a discharge path to ground, node X1 remains high and node X2 is pulled low through NM3 as the CLK goes high. Thus, node QB is charged high through PM2 and NM4 is held off. At the end of the evaluation phase, as the CLK signal falls low, node X1 remains high and node X2 holds the charge dynamically.

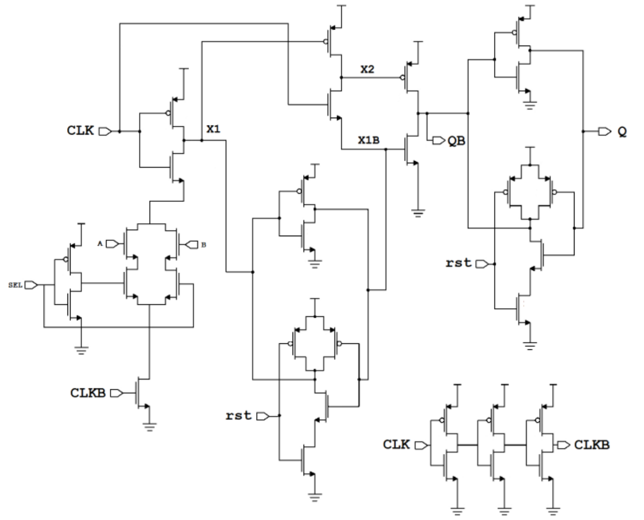

Fig 10: ELFF 2×1 MUX

V. PERFORMANCE ANALYSIS

Schematic design of the circuits was done using Mentor graphics Design Architect tool. The schematic design is followed by the circuit simulation and circuit verification with the help of simulation tool Mentor graphics ELDO using TSMC 0.18µm technology. The simulation results are viewed with the help of EZviewer and the results are documented. Input signals are provided with a rise-time and fall-time of 100ps using ELDO simulator. The obtained results are tabulated. The power dissipation for various flip-flop are measured at a V_{DD} of 1.5 V. From table I, CDMFF consumes lower power. It is due to reduction in redundant data transitions. The structures with dual dynamic nodes have lower power consumption. It is due to reduction of pre-charge capacitance due to split nodes. The D to Q delay is measured from EZviewer of ELDO simulator. The comparison results were extracted using PDAP (Power Delay Area Product) value. PDAP Comparison chart of Hybrid flip-flops is given in fig 11.

TABLE I. PERFORMANCE COMPARISON HYBRID FLIP-FLOPS AT 1.5V VDD

Flip-flop	*No. of transistors*	*Power Dissipated (pW)*	*D to Q Delay (ns)*	*PDAP*
HLFF	20	272.2	0.271	1475
SDFF	23	277.4	0.224	1429
CDMFF	22	204.8	0.240	1081
XCFF	21	224.5	0.154	726
DDFF	18	201.4	0.186	674

A discrete combination of logic and Flip-flop combination is compared with proposed ELFF at 1.8V V_{DD}. The obtained results are tabulated in Table II. The performance of embedding various logic functions like AND and OR are compared. It shows ELFF has better performance compared to discrete combination and DDFF-ELM. Comparison Chart showing the No. of Transistors in discrete mode and embedded mode is given in fig 12. PDAP Comparison chart of discrete mode and embedded logic flip-flop is given in fig 13.

Fig 11: PDAP Comparison Chart of Hybrid flip-flops

TABLE II. PERFORMANCE COMPARISON OF DISCRETE COMBINATION AND ELFF WITH EMBEDDED LOGIC AT 1.8V VDD WITHOUT RESET LOGIC

Function	*No. of transistors*	*Power Dissipated (pW)*	*D to Q delay (ns)*	*PDAP*
Discrete NAND + MSFF	48	289.0	0.476	6603
Discrete NOR + MSFF	48	415.7	0.478	9537
Discrete 2×1 MUX+ MSFF	52	441.4	0.477	10938
DDFF-ELM NAND Logic	23	424.2	0.182	1775
DDFF-ELM NOR Logic	23	471.9	0.167	1812
DDFF-ELM 2×1 MUX Logic	27	511.2	0.244	3366
ELFF NAND logic	23	411.1	0.156	1474
ELFF NOR logic	23	426.0	0.145	1420
ELFF 2×1 MUX logic	27	472.8	0.212	2701

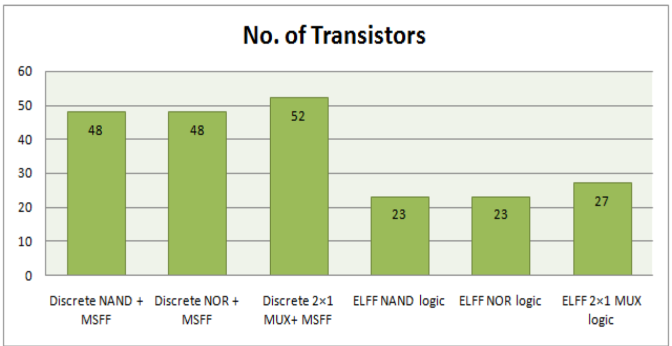

Fig 12: Comparison Chart of No. of Transistors in discrete mode and embedded logic flip-flop

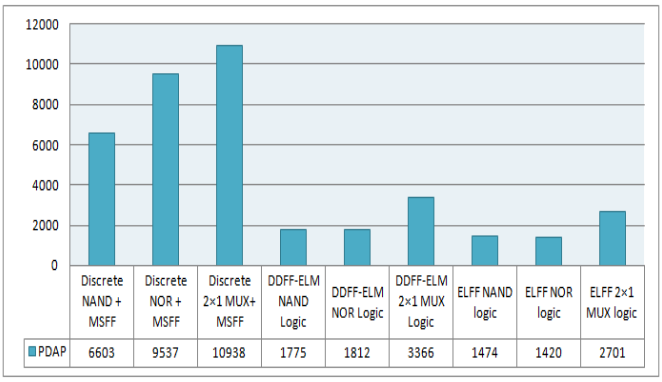

Fig 13: PDAP Comparison chart of discrete mode and embedded mode

The performance details of ELFF 2×1 MUX at different operating voltages are given Table III. It is found the ELFF can operate in a voltage range of 1.2 V to 2.1 V. PDAP Variation Chart of ELFF 2×1 MUX at Different Operating Voltages is given in fig 14. Simulation waveforms of ELFF 2×1 MUX is given in fig 15. The proposed ELFF uses same reset logic in both cross-coupled inverters, compared to existing DDFF-ELM. It is found the proposed ELFF have 20% better performance compared to DDFF-ELM.

TABLE III. ELFF 2×1 MUX AT DIFFERENT OPERATING VOLTAGES

V_{DD}	*No. of transistors*	*Power Dissipated (pW)*	*D to Q delay (ns)*	*PDAP*
1.2	31	185.3	0.378	2171
1.5	31	303.4	0.255	2398
1.8	31	472.8	0.212	3107
2.1	31	694.2	0.189	4067

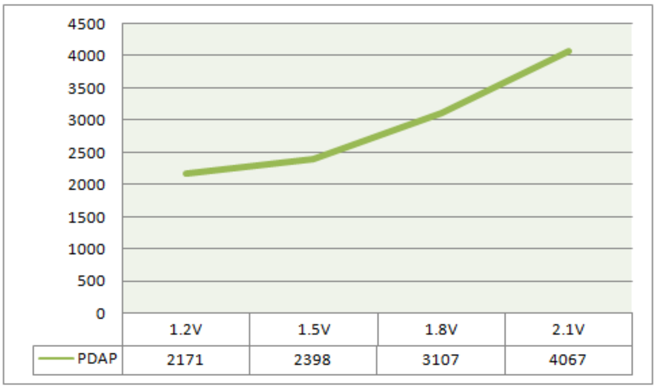

Fig 14: PDAP Variation Chart of ELFF 2×1 MUX at Different Operating Voltages

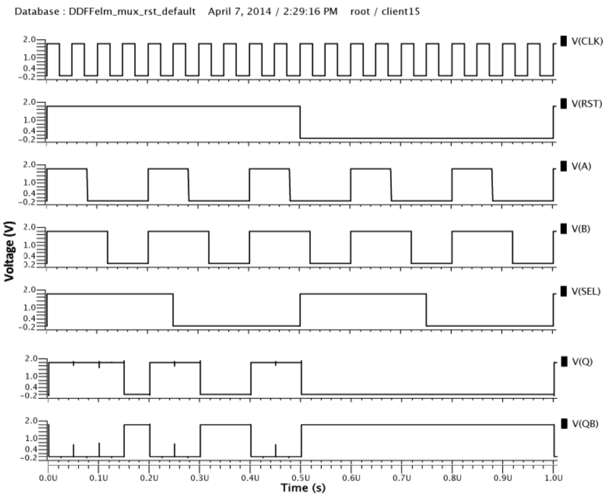

Fig 15: Simulation waveforms of ELFF 2×1 MUX

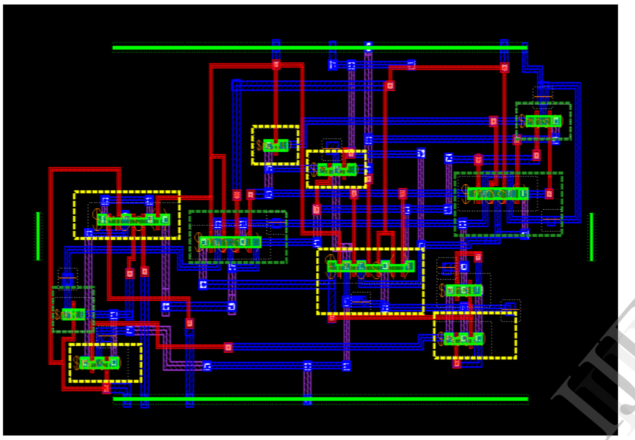

Fig 16: Layout of ELFF 2×1 MUX

After the schematic entry and design verification, we proceed with the layout for the ELFF. Mentor graphics Pyxis Layout Editor (IC station) is used for Schematic Driven Layout (SDL), as the name suggests the layout is drawn with the help of schematic, where in the devices and ports are instantiated from the schematic. The Layout of ELFF 2×1 MUX is shown in Fig 16. After laying out the layout in the Layout Editor, we performed physical verification which includes DRC, LVS. The DRC tool of Mentor Graphics IC station checks whether the layout conforms to the design rules. DRC can be run on the entire layout. For this we had selected the TSMC 180nm rules. The LVS tool of Mentor Graphics IC station checks if the layout matches to the schematic in various aspects. Finally we extracted parasitic capacitance for the ELFF. The post layout simulations are done using netlist extracted from layout.

VI. CONCLUSION AND FUTURE SCOPE

The proposed Embedded Logic flip-flop (ELFF) has a hybrid flip-flop architecture that combines the merits of dynamic and static structures. ELFF is provided with an asynchronous output reset, which can capable of easy implementation of counters and registers. ELFF has better performance in terms of power dissipation and delay compared to existing DDFF-ELM structure. This Flip-flop will be a good component to include in standard cell library for designing high performance VLSI chips.

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