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Design of 3 Bit MDAC for Pipeline ADC

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Abstract

A 3-bit MADC is designed in a 0.25-µm CMOS technology. Latched comparators (positive feedback) are used inside flash ADC for faster response. The ADC is designed according to thermometer coding. DC analysis of ADC & DAC are represented in the results. For residue the sweep voltage is from -1 to +1 which is 2 volts.

Index Terms- Analog-to-digital converter (ADC), Digital-to-Analog converter (DAC), pipeline ADC, Multiplying DAC (MDAC).

1. INTRODUCTION

High performance and low power consumption ADCs are generally required in the communication systems and image processing systems. For these systems the conversion speed of analog signal to digital should be high with high accuracy. The power consumption of these ADC should be low. Flash converters are extremely fast compared to many other types of ADCs with high accuracy over a series of stages. But a Flash converter requires a huge number of comparators as compared to other ADCs. In the section II the architecture of pipeline ADC is presented. In section III the design of MDAC is presented. Section IV represents the simulation results. In section V and VI conclusion and references are presented.

2. PIPELINE ARCHITECTURE

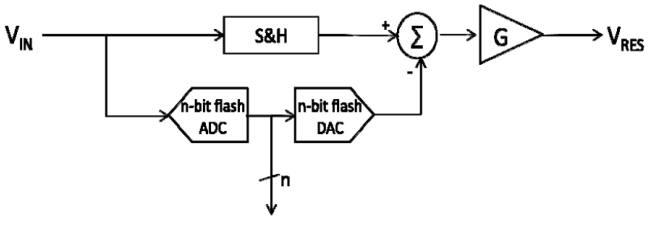

Figure 1: Pipeline ADC stage block diagram.

Figure 1 shows the pipeline ADC [8] each stage block diagram [4]. In each stage there is a sample and hold (S&H) block, a sub digital-to-analog (sub-DAC), a sub-ADC which is a flash type ADC [3], a subtractor and an inter-stage gain amplifier [5]. The sampled and hold takes the samples and apply to the sub-ADC which produces the output for this stage. The output of sub-ADC is again converted back to analog signal by sub-DAC. This quantized analog signal is subtracted from input signal.

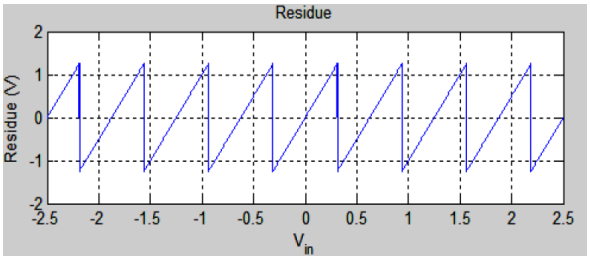

Figure 2: Residue voltage.

As a result of subtractor the residue voltage is generated. Figure 2 shows the residue voltage of MDAC. This residue is amplified and applied to the next stage. A binary bit searching scheme is used in the operation of pipeline ADC.

3. MDAC DESIGN

The first block of MDAC is sample and hold circuit [6]. The design of sample and hold circuit is as shown in figure 3.

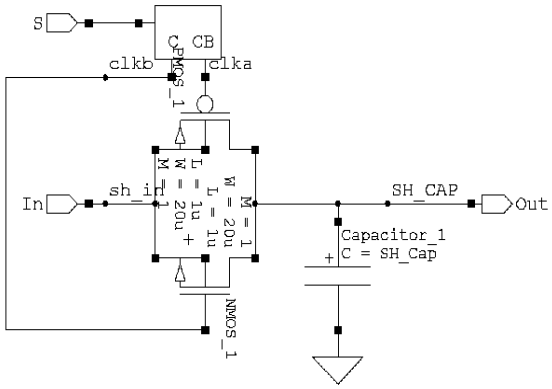

Figure 3: Sample and Hold circuit.

In S&H circuit the Pmos and Nmos are used. At the input a clock box is used to give the balance clock at the output.

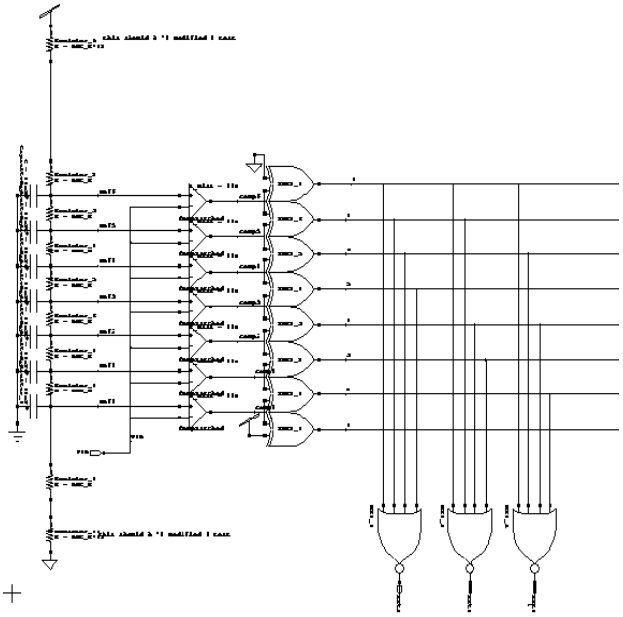

Figure 4: ADC circuit.

Figure 4 shows the ADC circuit. Here the series resistors are used to generate the binary output. The resistors used here are of 5K. These are applied to the opamp. The opamp act as a comparator. The comparator output is the thermometer coding. The code generated by converter is applied to the EX-OR gate which gives the binary output. This output is then connected to the NOR gate to produce 3 bit output. The EX-OR gate use the thermometer coding [7] to generate the desired output from circuit. The capacitors are used to reduce the kick back effect. The ADC circuit shown in figure 5 is a simple 3 bit flash adc.

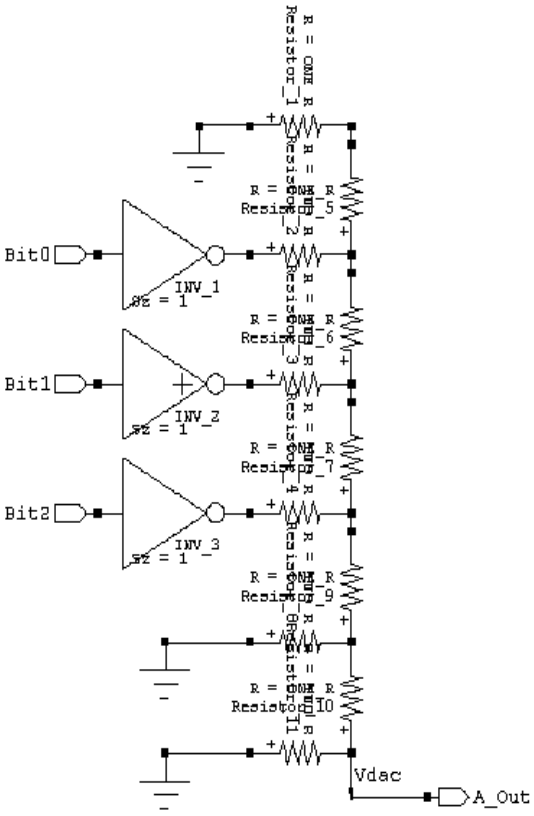

Figure 5: DAC circuit.

Figure 5 shows the DAC circuit. The output of ADC is converted into analog signal to obtain the residue voltage. To obtain this voltage the R-2R ladder circuit [6] is designed. Here before the R-2R circuit inverter is used because the output bits of ADC are opposite due to the use of universal NOR gate. The value of R is 100k and the value of 2R is 200k.

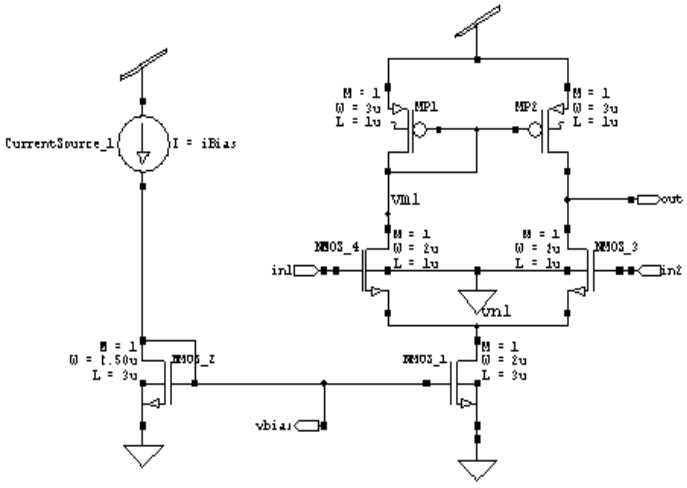

Figure 6: Differential amplifier.

Figure 6 shows the last stage is the differential stage output or gain stage. The gain of this amplifier is 8. The input

for the differential amplifier [7] is one analog signal from the input and other from the DAC [9] which is the residue voltage.

4. SIMULATION RESULTS

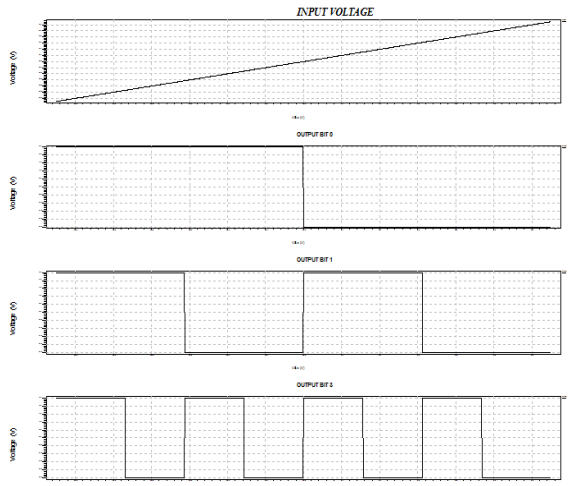

Figure 7: Input and output of ADC.

Figure 7 shows the result of ADC. As shown in figure the analog voltage is applied to the ADC and output is obtained in terms of three bits bit0, bit1, bit2. Due to the implementation of universal nor gate the output is inverted. Therefore at the peak level output bits are 000 and at the starting point the output is 111.

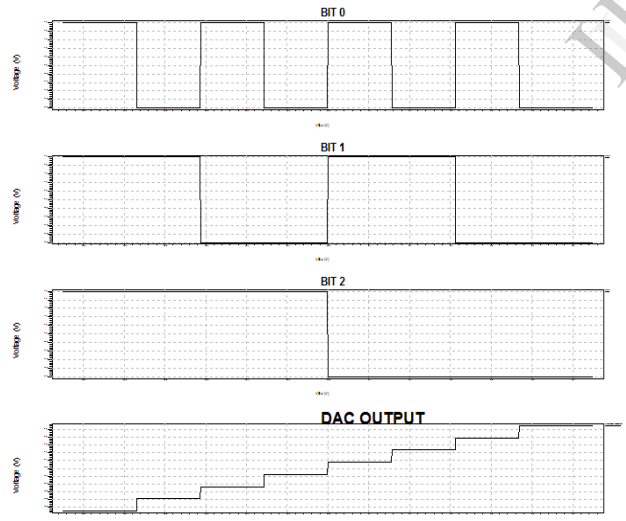

Figure 8: DAC input and output.

As shown in figure 8 the input and output of DAC are shown. The input for the DAC is digital voltage and at the output the analog output is obtained. Note that the analog output obtained at the output of DAC is quantized analog signal.

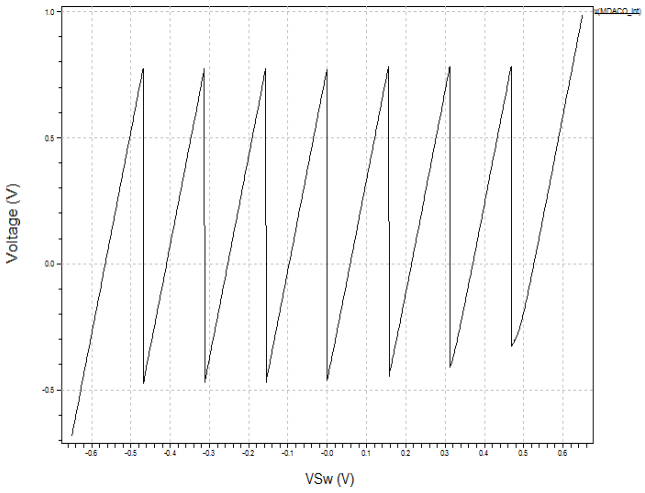

Figure 9: Residue voltage.

Figure 9 shows residue voltage. The residue represents the amplified remainder from the subtraction of the DAC output voltage from the stage input voltage. The residue is swept from -1 to +1. For the generalized pipeline ADC described previously, each stage is responsible for quantizing n bits of the input sample.

5. CONCLUSIONS

In this paper a method for design knowledge on design of 3-bit MDAC has been developed. It consists of design of ADC, DAC, S&H, differential amplifier design and their DC analysis.

From the simulation results it can be concluded that the final ADC output consists of a weighted sum of each stage's digital decision. The weightings are determined by the interstage gain or the gains of the residue amplifiers within each stage [7].

6. REFERENCES

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