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Design of 45 nm Fully Depleted Double Gate SOI MOSFET

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***Abstract*— Advanced MOSFETS such as Fully Depleted Double Gate (FD-DG)SOI MOSFET have gained popularity in the nanometer regime due to their inherent properties to suppress short channel effects and provide high drive current over a wide range of channel lengths. This paper presents the design of a 45nm FD-DG SOI MOSFET and studies the effect of variation of channel doping and gate oxide thickness (T_{OX}) on various device parameters. Characteristics for the proposed MOSFET have been obtained by considering optimum values of channel doping and T_{OX}. Cogenda's Visual TCAD tool has been used for the device simulation and parameter extraction.**

I. INTRODUCTION

First stated in 1965, Moore's law has allowed the number of transistors on a chip to double every sixteen months [1]. This progress has been made possible by continuous scaling down of the metal-oxide-semiconductor field-effect transistor (MOSFET) to smaller physical dimensions. MOSFETs have become cheaper, faster, consume less power and provide more functions per unit area of silicon as they become smaller. As a result, the chip density increases and there is improvement in the performance. As the gate length of a MOSFET is scaled down, the capacitive coupling of the channel potential to the source and the drain is more than the capacitive coupling to the gate,resulting in short channel effects (SCE), such as threshold voltage (V_{TH}) roll-off i.e. reduction in thresholdvoltage with a reduction in channel length[2] and drain- induced barrier lowering (DIBL) i.e. reduction in V_{TH}at higher drain voltage (V_{DS}) due to reduction of the source-channel potential barrier by the drain voltage. V_{TH}roll-off and DIBL result in increased off-state transistor leakage (I_{OFF}). Increase in I_{OFF}may hinder CMOS scaling because of significant power consumption and isthus becoming a serious concern for high-performance circuits. The practical
limits imposed by scaling the Bulk MOSFETs into nanometer regime necessitates the need to look for advanced device structures .The Double Gate fully depleted SOIMOSFET is a good technology choice for nanoscale technologies. With one extra gate, the gate to channel coupling is doubled and the influence of source and drain on the channel becomes small. This gives the DGFD SOI MOSFET an inherent capability to suppress short channel effects. Moreover, due to the presence of two channels the DGFD structure exhibits an improved current drive capability. DGFD structures with thin body thickness can suppress the leakage current by eliminating the part of channel that is not effectively modulated by the gate. These structures do not need high channel doping as it is defined by the body thickness. As a result mobility degradation and statistical dopant fluctuation problems can be eliminated. The junction depth is also defined by the body thickness. Thus, shallow junctions can be realized easily without developing complicated ion implantation techniques.

II. DOUBLE GATE SOI MOSFET

The Double Gate SOI MOSFET has two gates simultaneously controlling the charge in the thin silicon body, allowing two channels for conduction as shown in Fig.1. A direct charge coupling existsbetween the front and back gate due to the thin SOI film [3].This influences the terminal characteristics of the device. The main objective of designing a Double Gate MOSFET is to suppress the Short channel effects to a large extent and maintain good electrical characteristics in terms of a high I_{ON}/I_{OFF}ratio and sharp I-V slope[4]. The threshold voltage can be controlled by front and back gates simultaneously. Hence, the transistor threshold voltage can be changed dynamically according to the circuit's operating state. In the standby mode, a high threshold voltage gives a low leakage current, while a low threshold voltage gives a higher drive current in the active mode [5].

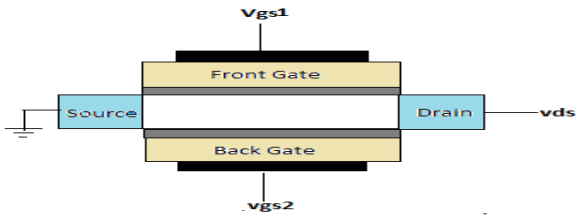

Fig.1. General Double Gate MOSFET Structure

A. *Types of Double Gate MOSFET*

Double Gate MOSFETs are characterized as follows:

- *Symmetric Double Gate MOSFET:*

A Double Gate MOSFET is said to be symmetric [6] if both thegates have identical work functions as shown in Fig.2.

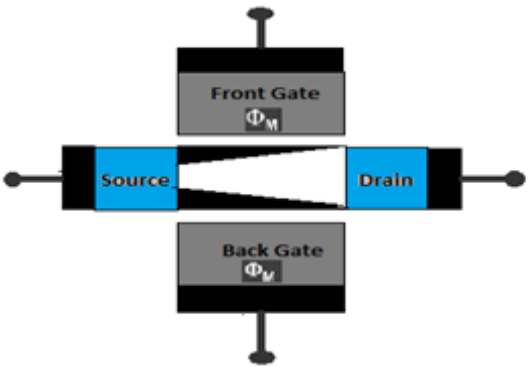

Fig.2. Symmetric Double Gate MOSFET structure

- Asymmetric Double Gate MOSFET:

A Double Gate MOSFET is said to be asymmetric if both the gates have different work functions as shown in Fig.3.

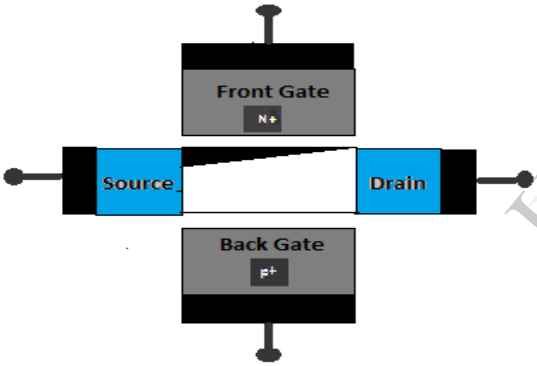

Fig.3. Asymmetric Double Gate MOSFET structure

B. *Double Gate MOSFET operation*

The voltage applied on the gate terminals controls theelectric field, determining the amount of current
flow through the channel. Double gate MOSFET has two modes of operation as shown in Fig.4.
The most common mode of operation is to switch both channels simultaneously.

Another mode is to switch only one gate and apply a bias to the second gate. This is called ground plane (GP) or back gate (BG).

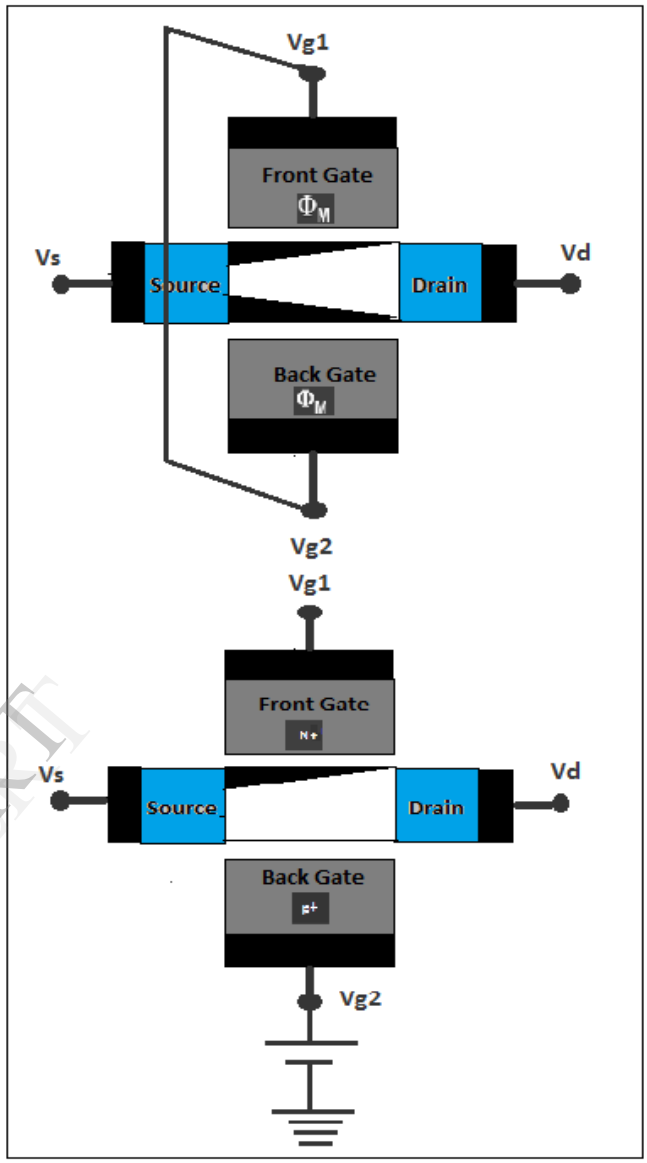

Fig.4. Modes of Operation of Double Gate MOSFET

III. RESULTS AND DISCUSSION

In this work, a 45 nm Double Gate Fully Depleted SOI MOSFET has been designed. SiO_2 has been used as the gate oxide.

A. Impact of channel doping on I_{OFF}, I_{ON} and V_{TH}

- Impact of channel doping on I_{OFF}:

$I_{OFF}$is defined as the current flowing from Drain to source when V_{GS}=0 and V_{DS}=V_{DD}. This current is affected by a number of parameters such as channel physical dimensions, channel doping profile, source/drain junction depth, gate oxide thickness and supply voltage. As channel doping increases the value of I_{OFF}decreases as shown in Fig.5.

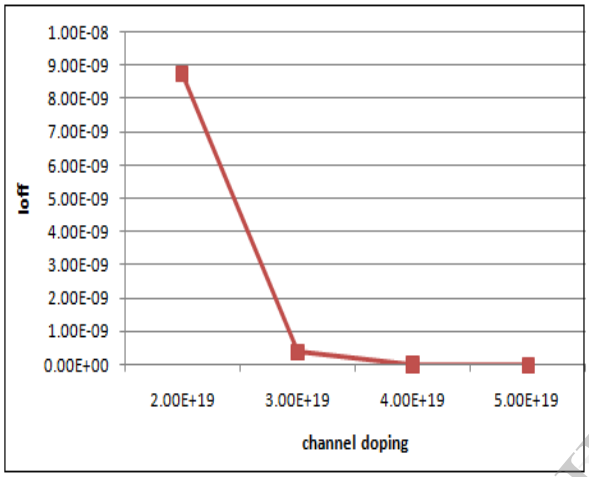

Fig.5. Impact of Channel Doping on I_{OFF}

- Impact of channel doping on I_{ON}:

I_{ON} is defined as the current flowing from Drain to source when V_{GS}=V_{DD} and V_{DS} =V_{DD}. The current driving capability of a MOSFET is decided by its on-state current. As channel doping increases the value of I_{ON}decreasesas shown in Fig.6.

- Impact of channel doping on V_{TH}:

Threshold voltage is defined as the gate voltage at which the drain current i.e. I_D=10^{-7}(W/L_{EFF}) where W is the width of the device and L_{EFF} is the effective channel length. As channel doping increases the value ofV_{TH} increases as shown in Fig.7.

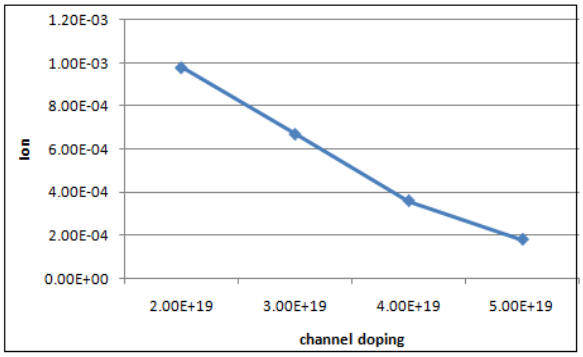

Fig.6. Impact of Channel Doping on I_{ON}

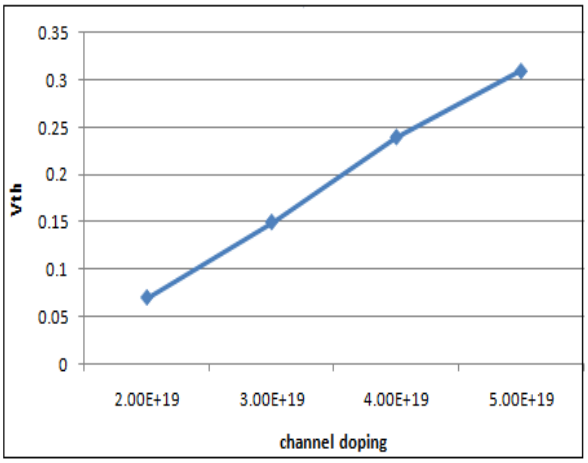

Fig.7. Impact of Channel Doping on V_{TH}

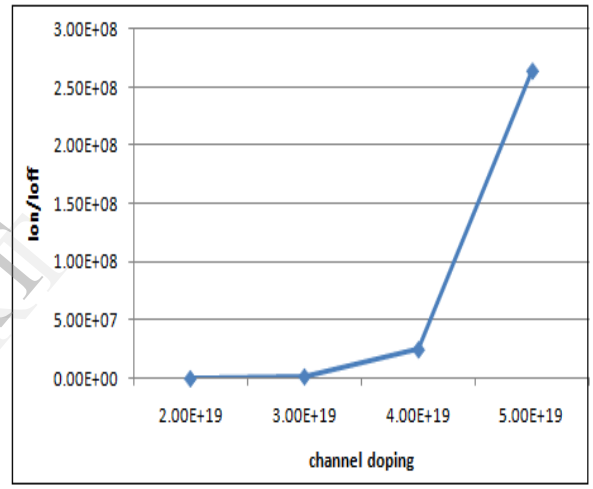

Fig.8. Impact of Channel Doping on I_{ON}/I_{OFF}

- Impact of channel doping on I_{ON}/I_{OFF}:

As the channel doping increases, there is an improvement in the I_{ON}/I_{OFF} ratio as shown in Fig.8.

B. Impact of Oxide thickness on I_{OFF}, I_{ON}, V_{TH}

- Impact of oxide thickness on I_{OFF}:

As oxide thickness decreases I_{OFF}increasesas shown in Fig.9.This increase in I_{OFF} is due to Tunnelling effect.

- Impact of oxide thickness on I_{ON}:

As the oxide thickness decreases Ion increases as shown in Fig.10.This increase in I_{ON} is due to an increase in the gate to channel coupling.

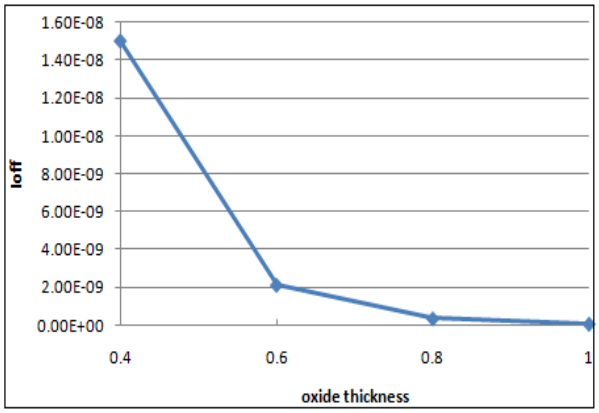

Fig.9. Impact of Oxide Thickness on I_{OFF}

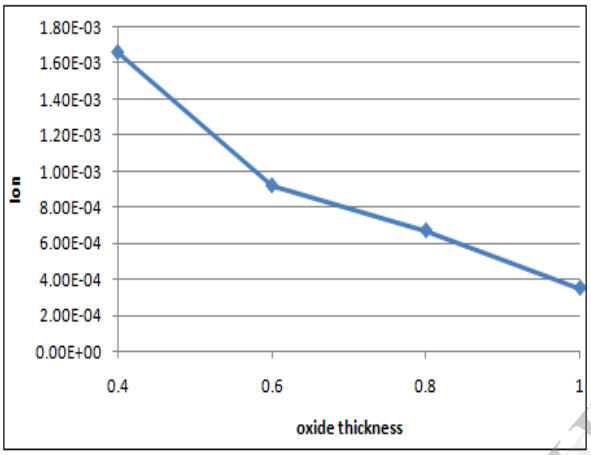

Fig.10. Impact of Oxide Thickness on I_{ON}

- Impact of oxide thickness on V_{TH}:

As the oxide thickness decreases, V_{TH}decreases as shown in Fig.11.This decrease in V_{TH} is due to the increase in attraction of the gate on the channel.

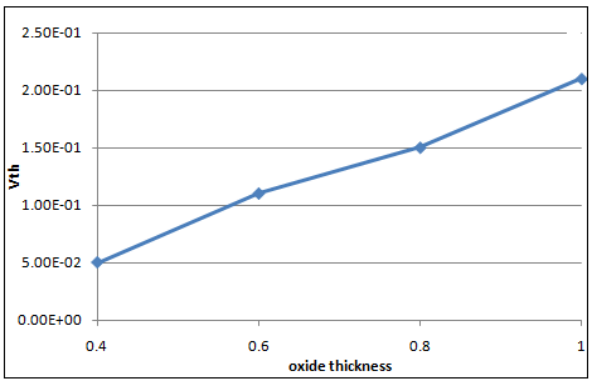

Fig.11. Impact of Oxide Thickness on V_{TH}

- Impact of oxide thickness on I_{ON}/I_{OFF}:

As the channel doping increases, there is an improvement in the I_{ON}/I_{OFF} ratio as shown in Fig.12.

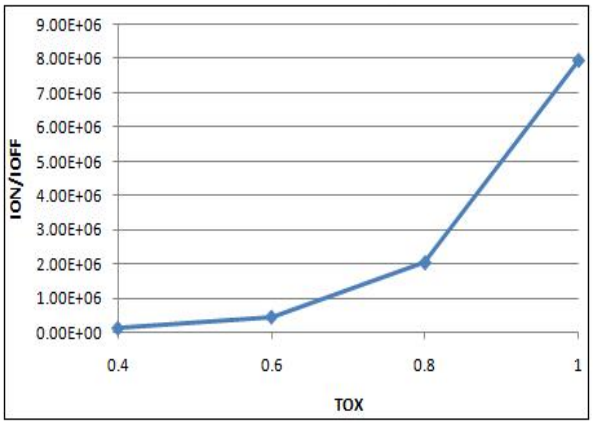

Fig.12. Impact of Oxide Thickness onI_{ON}/I_{OFF}

C. *Characteristics Based On Above Analysis*

- ID-VGS Characteristics:

Transfer characteristics determining the values of $I_D$with variation in V_{GS} keeping V_{DS} constant at 0.6V have been plotted,for the proposed 45nm DG MOSFET with Table I parameters as shown in Fig.13. These parameters have been obtained from above analysis of T_{OX} and Channel Doping variation.

- I_D-V_{DS} Characteristics:

Output characteristics determining the values of $I_D$with variation in V_{DS} keeping V_{GS} constant at 0.6V have been plottedfor proposed 45nm DG MOSFET with Table I parameters as shown in Fig.14.

Table I. Prameters for 45nm DG MOSFET from above analysis

S.No.	Parameter	Value
1.	Gate length	45nm
2.	Gate oxide thickness	0.8nm
3.	Silicon film thickness	4nm
4.	Body doping	3e19

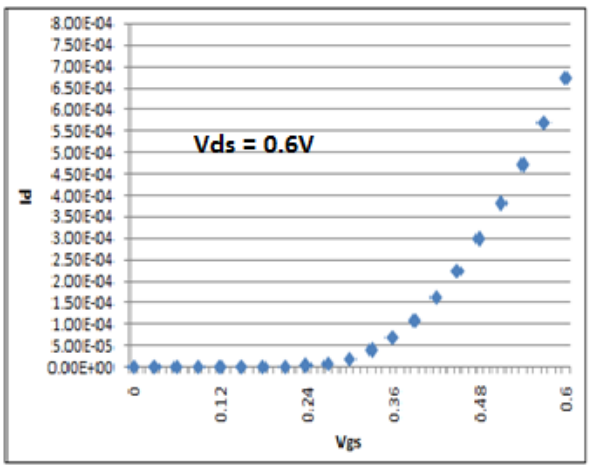

Fig.13. I_D-V_{GS} Characteristics

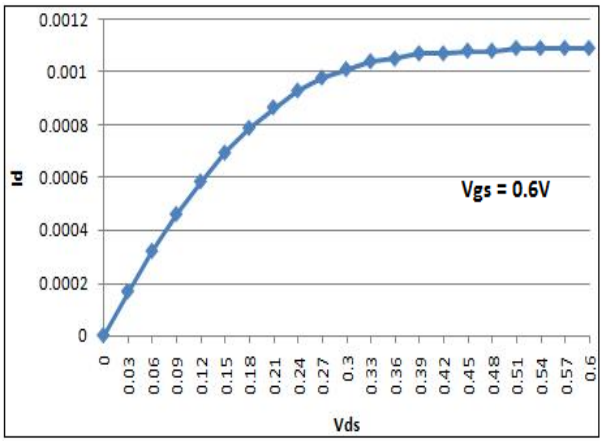

Fig.14. I_D-V_{DS} Characteristics

IV. CONCLUSION

From the above analysis, we can conclude that as the devices are scaled down, the off-current becomes a major concern due to short channel effects that creep in at shorter gate lengths. Channel engineering can be used to control the leakage within permissible limits but the channel doping cannot be increased beyond a certain point as it is necessary to maintain a trade-off between I_{ON} and I_{OFF}. Very high doping levels can lead to mobility degradation of carriers in the channel. Optimum device parameters were found by simultaneously optimizing the channel doping and gate oxide thickness.

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