Design of 6T- SRAM Cell Using Dual Threshold Voltage Transistor

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Abstract

Most microprocessors use large on-chip SRAM caches to bridge he performance gap between the processor and the main memory. Due to their growing embedded applications coupled with the technology scaling challenges, considerable attention is given to the design of low-power and high-performance SRAMs. Static random access memories (SRAM) are widely used in computer systems and lots of portable devices. In this paper, we proposed 6T-SRAM cell with dual threshold voltage transistors. Low threshold voltage transistors are mainly used in driving bit lines while high threshold voltage transistors are used in latching data voltages. The advantages of dual threshold voltage transistors can be used to reduce the access time and maintain data retention at the same time.

Hence, high-speed and low-power 6T-SRAM cell operations of the SRAMs are feasible. This paper presents a 5-transistor dual voltage SRAM cell intended for the advanced microprocessor cache market using 1.8v/0.18um cmos technology. The goal is to reduce the power of the cache memory array while maintaining competitive performance

1.Introduction

Semiconductor memories are most important subsystem of modern digital systems. In new era the scaling of silicon technology has been ongoing, due to scaling large memory can be fabricated on a single chip as results memories are capable to store and retrieve large amount of information at high speed. But due to high density, power dissipiation gets increases and speed decreases. So there is need for the design of low power and high speed circuit in memory. A memory in terms of computer hardware is a storage unit. There are many different types of hardware used for storage, such as magnetic hard drives and tapes, optical discs such as CDs and DVDs, and electronic memory in form of integrated memory or stand-alone chips.[6]

The main focus of this paper is the SRAM. There are some very important requirements for a memory when it is to be embedded as on-chip cache. First and foremost it has to be reliable and stable. This is of course true for all memories, but is especially important for cache due to the more extreme performance requirements and area limitations. Secondly the memory has to have high performance. The sole purpose of cache is to speed up the operation of the CPU by bridging over the performance gap between main memory and the CPU. Another most important requirement is low power consumption. Today's advanced microprocessors use a lot of power and get very hot as a result. With increasing memory sizes these contribute with more and more power loss. This is especially important in mobile applications where

prolonging battery life strongly depend on minimizing power loss.

2.Problem associated with single – vth SRAM cell

There are many techniques which reduces power dissipiation and wake low power SRAM cell divided word line architecture, memory banking architecture, pulsed world line and reduced voltage swing techniques are used to reduce only active power dissipitation. On the other hand during standby mode, there is leakage power disspitation due to presence of sub threshold and gate tunneling leakage currents

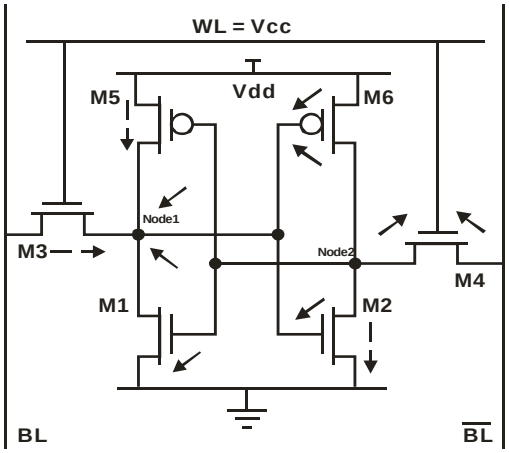

Figure-1 Subthreshold and Tunneling Gate Leakage of SRAM Circuit [2]

To avoid these leakage, Dual therehold (dual Vth) techniques applied on Conventional SRAM cell.

3. Dual – vth 6T SRAM cell

A typical dual Vth 6T-Cell is shown in fig-4.3. The access transistors M3 and M6 are controlled by the world line (WL).It threshold voltage of N3 and N4 is low , the switching time of N3 and N4 will be reduced, which will be reduced, which will in turns shorten the access time of the 6T- SRAM cell

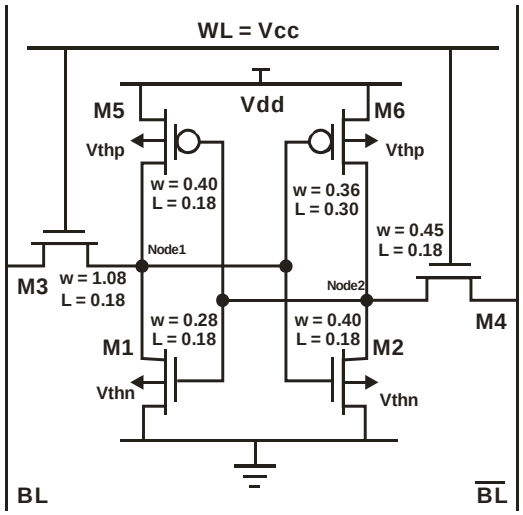

Figure-2 Schematic of Dual – Vth 6 -SRAM Cell with Final Sizes [1]

Hence we use the low-Vth transistors to implement the driving transistors. It will produce a large driving current than normal or high-vth transistors By contrast, transistors with high – Vth possess low leakage current and sub threshold current. Thus, they are very good to be cross coupled as a data latch. Thick channel transistors are showing high threshold voltage (high Vth), while thin channel transistors are showing low threshold voltage (low Vth) in fig shown below. [7]

Design of 6T-SRAM Cell is started with making Schematic after that optimization of 6T-SRAM Cell is done is done in such a way that it meets the required objectives. Write operation is possible for dual Vth 6T-SRAM cell with transistors sized for a 0.18um CMOS technology for proper write operation simulations are done for different width of transistor. The simulation results show a significant amount of average power reduction.

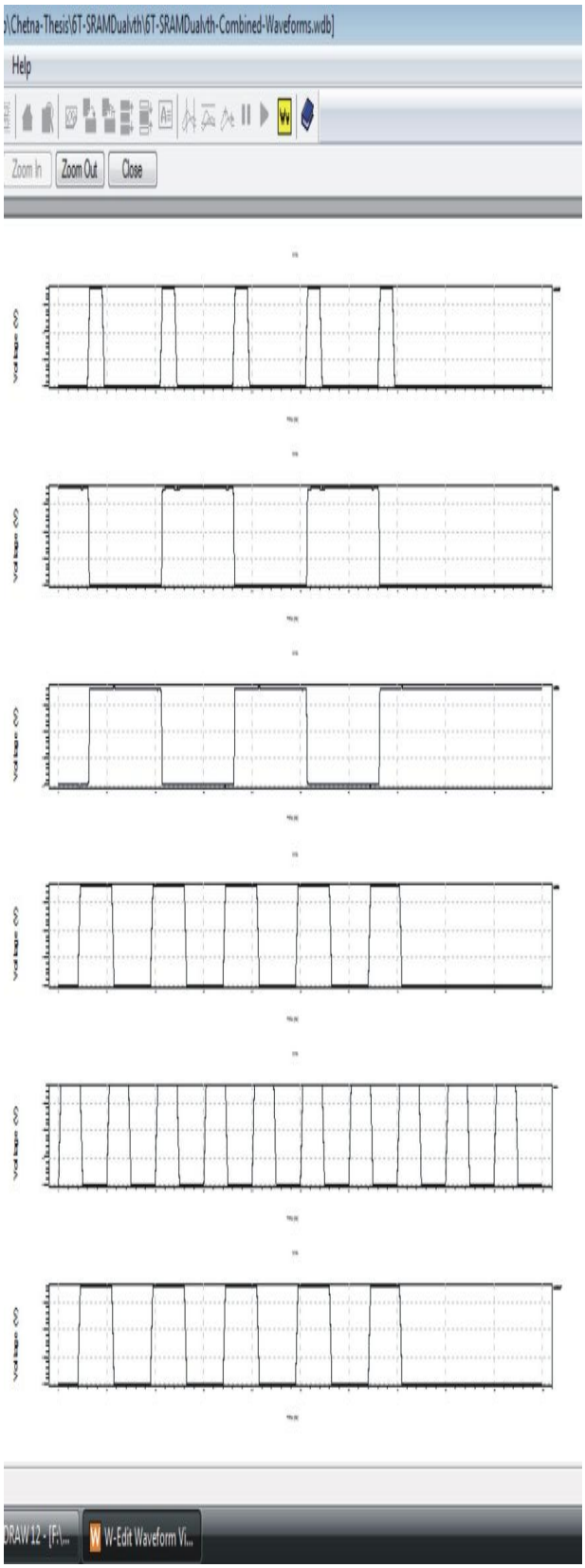

Figure-3 Voltage waveforms of Dual – Vth 6T-SRAM

4. Simulation wave forms of dual – Vth 6T-SRAM cell

Non-distractive write operation is possible for dual Vth 6T-SRAM cell with transistors sized for a 0.18um CMOS technology for proper write operation simulations are done for different width of transistor. The width is varied in steps of 0.04 um. The results of these simulations are shown in fig-4.

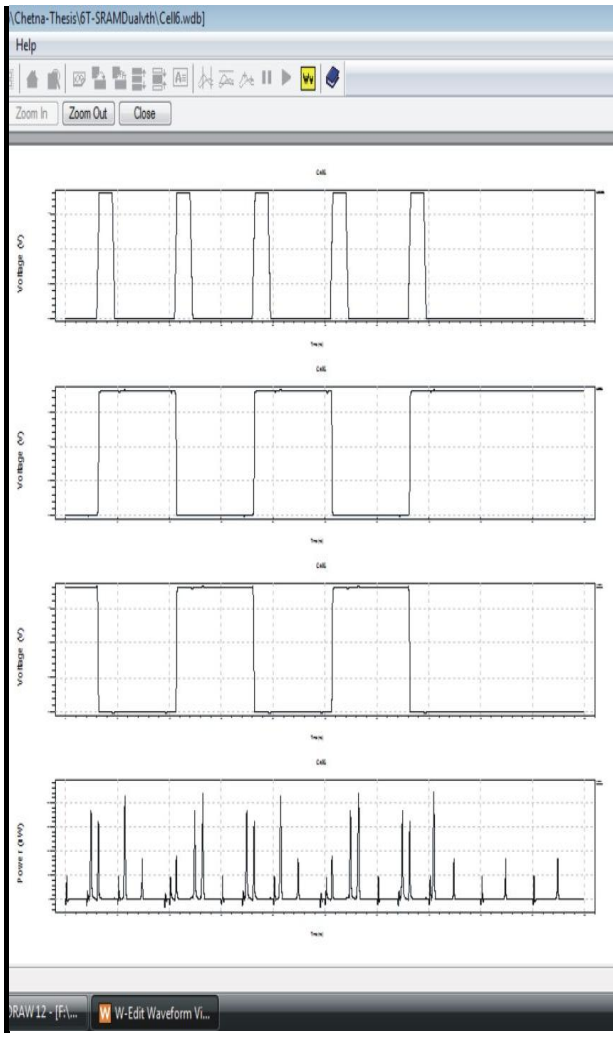

Figure-4 Simulation wave forms of dual – vth 6T-SRAM

The simulation results show a significant amount of average power reduction by Dual - Vth 6T-SRAM Cell.

4. Conclusion

In this paper, the analysis and simulation is done for Dual - Vth 5T- SRAM Cell as compared with Dual - Vth 6T-SRAM Cell using 1.8v/0.18um cmos technology. The values of sensing delays and average power consumption are calculated for different sizes of CMOS-Transistors.

Table-1 Write delay in dual vth 6T-SRAM Cell

Operation	6T-SRAM Cell Writ Delay(ns)
Write'0'	3.0518e-08
Write'1'	1.5143e-08

Table-2 Write power consumption in dual Vth 6T-SRAM

Operation Write Delay(ns)	6T-SRAM Cell Write Power Consumption (µw))
0	50
2.5	180
3.0	160
Average Power Consumption	390(µw)

Hence all of these parameters have adjusted together until a satisfactory result is achieved. For instance sizing of transistors have been done in such a way that 6T-SRAM cell can reduce power consumptions and delay shown in above tables.

REFERENCES

[1] Stefan Adersson, Sreedhar Natarajan "A High Density, Low Leakage, 5T-SRAM For embded Caches" *2004 IEEE Department of Electrical Engg Linkoping University, SWEDEN*

[2] Shilpi Birla, Neeraj Kr. Shukla, Debasis Mukherjee and R.K. Singh**, "**Leakage Current Reduction in 6T Single Cell SRAM at 90nm Technology" *IEEE international Conference on Advances in Computer engineering* 2010, 978-07695-0.—13

[3] Shilpi Birla, Née raj Kr. Shukla , Debasis Mukherjee and R.K. Singh ," Leakage Current Reduction in 6T Single Cell SRAM at 90nm Technology" *IEEE international Conference on Advances in Computer engineering* 2010 ,978-07695-0.—13

[4]Hooman Jarollahi and Richard F. Hobson**,** "Power and Area Efficient 5T-SRAM with Improved Performance for Low-Power SoC in 65nm CMOS" 978-1-4244-7773-9/10/-2010 *IEEE* 121

[5] David Hentrich, Erdal Oruklu, and Jafar Saniie,"Performance Evaluation of SRAM Cells in 22nm Predictive CMOS Technology" *IEEE International Conference on Electro/Information Technology*, 978-1-4244-3355-1 *IEEE*-2009.--14

[6] Jawar Singh, Jimson Mathew, Dhiraj K. Pradhan and Saraju P. Mohanty , " Low power CMOS VLSI Circuit design" John Wiley and Sons, *IEEE International Conference on Electro/Information Technology*,978-1-4244-2596-9 *IEEE*-2008.—5

[7] Sung-MO Kang, Yusuf Lablebci," CMOS Digital integrated circuits: Analysis and Design" *Tata McGraw Hill Third edition, 2003.*