Design of a Frequency Synthesizer for WiMAX Applications

Samarth S. Pai
Department of Telecommunication
R. V. College of Engineering
Bangalore, India

Abstract

Implementation of frequency synthesizers based on phase-lock-loops (PLL) is one of the most challenging blocks of the wireless communication systems such as WiMAX. This paper reviews the requirements set for the frequency synthesizer by the wireless standards, and how these requirements are derived from the system specifications. These requirements apply to both integer-N and fractional-N synthesizers. In this paper we discuss one of the design and architecture of frequency synthesizer used in WiMAX applications with description of each block that is required for building of the frequency synthesizer.

1. Introduction

WiMAX, or Worldwide Interoperability of Microwave Access, is a wireless Internet service designed to cover wide geographical areas serving large numbers of users at low cost. WiMAX is the synonym given to the IEEE 802.16 standard defining wide area wireless data networking. As the wireless transceivers systems getting growth in the worldwide, improving of the resolution, speed and lowering the power and area of the circuits, are of the most important issues. Thus one of the most challenging blocks of the wireless communication systems such as WiMAX are frequency synthesizers that can be implemented based on phase-lock-loops (PLL).

An Integer-N structure is the simplest structure for a PLL-based synthesizer. This type of synthesizer suffers from many problems. In this structure channel spacing should be the same as reference frequency (fref). So in applications with many channels and low channel spacing (fs), such as WiMAX, the above criteria forces fref to be as low as fs. According to Gardner stability criteria lower fref results in a lower loop BW, which in turn leads to a lower switching speed, a higher in band noise and a large module for counter (MIT open courseware). So we choose a Fractional-N structure for our design. In this structure, the value of fref is independent of fs, and we can set a higher fref to achieve a wider loop BW while having lower fs to gain a fine resolution.

In this paper a frequency synthesizer is designed with a small filter capacitance which results in a lower charge-pump current while having a good phase margin and a small settling time. Further reduction in the area of the circuit is achieved by not implementing a inductor in the design. Also TSPC logic is employed in the counter for reduced area and more power as TSPC is compatible with CMOS logic.

2. Structure of Frequency Synthesizer

Fig. 1 illustrates a fractional-N PLL-based frequency synthesizer (Eldon Staggs, 2005). Here, we employ a Ring oscillator-based VCO. To cover the WiMAX band from 2.3GHz to 2.7GHz, we only need to generate 1.5GHz~1.8GHz, with the frequency step of 20MHz. The number of the channels is 15. Using a div-2 divider and two mixers, the I and Q frequency components from 2.3GHz to 2.7GHz for a quadrature OFDM system is generated. Using this technique allows us to design a counter with lower division factor. This saves the power, because much of the system power is consumed in the high frequency counter (Eldon Staggs, 2005). The detailed description of each block is as follows,

2.1 Phase/Frequency Detector (PFD)

To design a PFD we use the common structure shown in Fig. 2 (R. Jacob Baker, 1996). To reduce the power we employ CMOS logic to implement the D-Flip Flops and the logic gates. For WiMAX standards (Eldon Staggs, 2005), the frequency lower than 35MHz is proposed for fref.

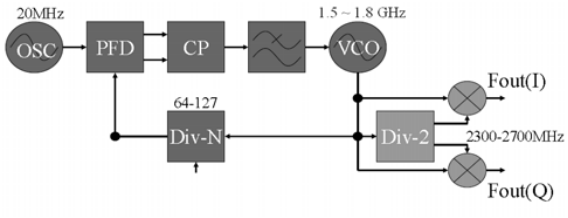

Fig.1. Proposed frequency synthesizer structure

On the other hand, as fref increases, the jitter and noise problems get worse. So we select fref to be 20MHz in order to have a relatively low jitter noise. The crystals which generate this value of fref are easily available and also having fref value of 20MHz is a good compromise to have a reasonable counter division factor. In the feedback path of this PFD a delay about 200psec~300psec is contrived to compensate the dead zone in the PFD characteristic. This dead zone may cause the PLL to be unlocked or have an incorrect performance.

2.2 Charge Pump (CP)

The output of the PFD is a digital signal. So before applying this signal to a LPF we should convert it to a related analogue voltage/current signal. This is accomplished by a charge-pump, which operates as a digital to analogue converter Fig. 3.

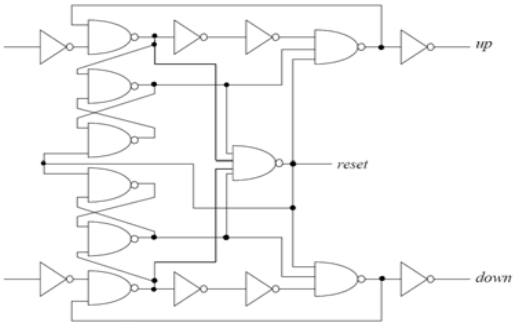

Fig.2. PFD structure

2.3 Low Pass Filter (LPF)

Charge-pump output current passes through the sampling capacitor (C1) and gets converted to a voltage level. We use another capacitor parallel with C1 to eliminate the voltage ripple. To increase the phase margin of the filter we employ a resistor (R1) to move the zero to the left hand plane (LHP).

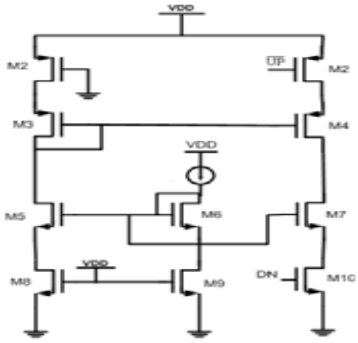

Fig. 3: Charge pump circuit

By adding R2-C3 in parallel, a very far pole is generated which leads to a much more ripple reduction. This results the filter to be of order three. Since the third pole is set to be very far from the second pole in the filter, we can approximate the 3rd order filter with a 2nd–order one to alleviate the complexity of the calculations. The final filter topology is shown in Fig. 4. The following steps show the filter design calculations in brief.

$$\omega_c = \frac{1}{10}\omega_{ref} = 12.5\times10^6 \, rad/\sec$$

Using the below definitions:

$$b = 1+\frac{C_1}{C_2} \quad , \quad \omega_Z = \frac{1}{R_1 C_1}$$

$$\omega_{P2} \approx b\omega_Z$$

$$\omega_C \approx \sqrt{\omega_{P2}.\omega_Z} = \sqrt{b}.\omega_Z$$

That wZ is the filter zero and the wC is the loop BW. So the phase margin can be found by using the following equation,

$$PM = tg^{-1}\left(\frac{\omega_C}{\omega_Z}\right) - tg^{-1}\left(\frac{\omega_C}{\omega_{P2}}\right) = tg^{-1}\left(\frac{b-1}{2\sqrt{b}}\right)$$

We can find the values of the filter elements:

$C_1 = 25pF,\ C_2 = 1pF,\ C_3 = 2PF$
$R_1 = 20k\Omega,\quad R_2 \approx 1K\Omega$

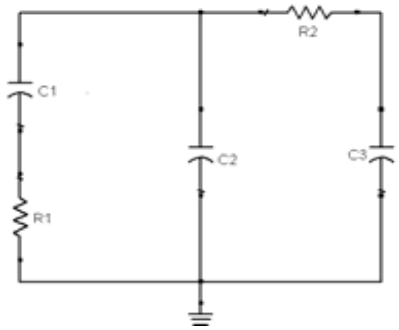

Fig. 4: Proposed low pass filter

2.4 Voltage Controlled Oscillator (VCO)

We select Ring oscillator-based VCO instead of LC-tank based VCO in our design to have more area and power saving. The topology of this circuit is shown in Fig. 5. The tuning range of the input control voltage from -0.2V to 1.2V is sufficient to cover the desired frequency band. We find that the desired VCO gain to generate the in-band frequencies is 200MHz/V, but the VCO in Fig.5 have much higher gain than this one, which leads to a very low resolution output and may drop some channels because of the sensitivity reduction. To overcome this significant problem we should reduce the gain of the VCO. To accomplish this, we place a gain-linearizer just before the VCO. By this technique, VCO gain of almost 200MHz/V can be achieved. The VCO output frequency versus the input control voltage of the VCO after using the gain-linearizer block is shown in Fig. 6. This structure of the VCO, have a low power. The power consumptions of the VCO with gain-linearizer for the lowest and highest frequencies are:

$$\begin{cases} f_{VCO} = 1.5GHz \\ P_{diss} = 3.46mW \end{cases}$$

$$\begin{cases} f_{VCO} = 1.8GHz \\ P_{diss} = 4.2mW \end{cases}$$

2.5 Counter

One of the essential blocks of the system is a programmable counter which is able to produce fractional division factors (N). To have a flexible programming in the counter we use a multi-modulus counter. A simple 3-modulus counter is shown in Fig. 7. Multi-modulus allows us to use small division factor counter, say N=2~3, to implement a counter with a very big division factor instead of designing one counter with a large division factor. This saves the power and area, while the design complexity is reduced. Since the input frequency of the counter is very high, so CMOS logic can't be used to implement this counter. Thus, we use a well-known logic named TSPC, Fig. 8 in this structure. This logic has been proved to have almost 1mW in 2GHz. The division factor should be from N=76 to N=90, in order to support the PLL output range with fref=20MHZ. By considering this range, a 6-modulus counter is selected for this counter.

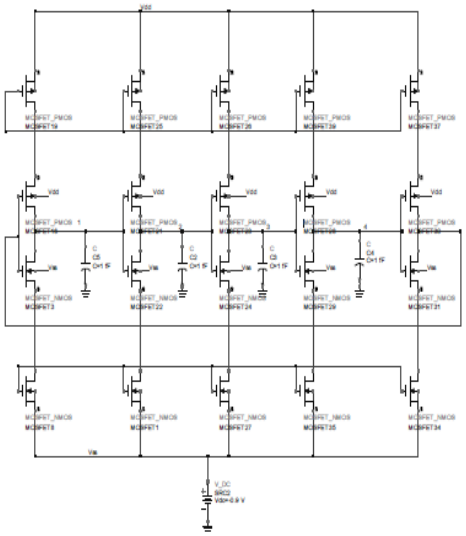

Fig.5. Ring Oscillator Circuit

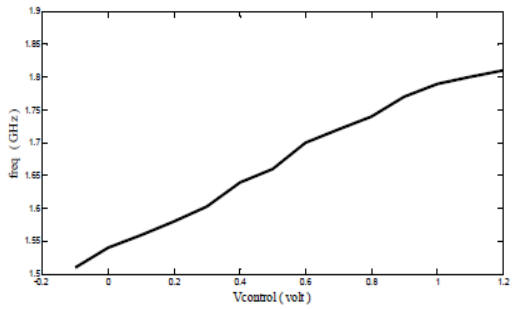

Fig.6. Frequency variation of VCO Vs. control voltage

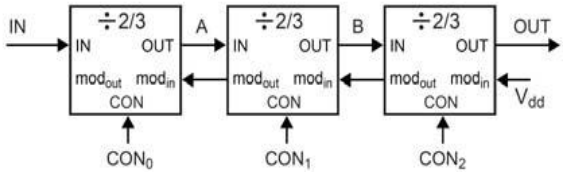

Fig.7. Three Modules Implementation for Counter

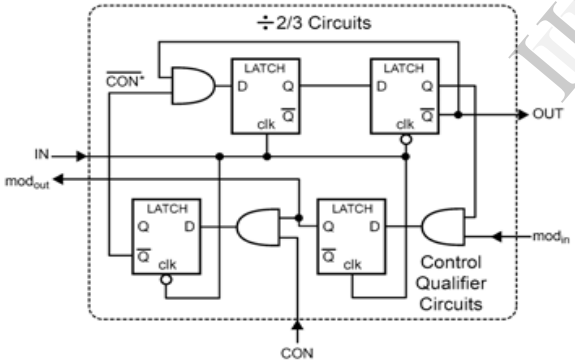

Fig.8. Schematic of Each Counter Module

3. Conclusion

In this paper a PLL-based frequency synthesizer for WiMAX application is designed. For better results, certain improved techniques are applied to the design. To reduce the gain of the VCO, a gain-linearizer block is used just before the VCO. TSPC logic is employed to implement the high frequency counter and to lessen the power consumption. To increase the integration capability of the circuit as a whole, the capacitors of the filter are designed to be as small as possible without compromising on the performance of the system.

4. References

[1] M. Mohammad Abadi, M. Tamaddon, R. Jahani and H. Chahkandi Nejad, "Design of a PLL Based Frequency Synthesizer for WiMAX Applications", *Australian Journal of Basic and Applied Sciences*, 5(9): 844-853, 2011, ISSN 1991-8178.

[2] Eldon Staggs 2005, "Mobile Wi-Max Radio Phase Locked Loop Design", an *Applications workshop for High-performance design*, Ansoft.

[3] Gardner, F.M., "*Phase lock Techniques*", 2nd ed., 1979, New York, John Wiley.

[4] Jacob Baker, R., W. Harry Li and E. David Boyce, "CMOS Circuit Design, Layout, and Simulation", *Series on Microelectronic Systems*, IEEE Press, 1999.

[5] Perrot, M.H., "*High Speed Communication Circuits lecture notes*", MIT open courseware.

[6] Ziboon, H.T., H.M. Azawi, "Design and Simulation of Sigma-Delta Fractional-N Frequency Synthesizer for WiMAX", Eng. & Tech magazine, 26(9), 2008.