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Design of a Low Power Current Steering Digital to Analog Converter in CMOS

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***Abstract*— In this paper it deals with the design & analysis of a 16-bit current steering digital-to-analog converter. The digital-to-analog converter contained eight sets of current mirrors with different weight. The digital-to-analog converter was implemented using *GDI Technology (Gate Diffusion Input)* in CMOS process. The average INL and DNL are 0.27 LSB and 0.32 LSB, respectively. At the sample rate of 350 MHz and supply voltage of 3.5 V, the DAC consumed about 66.903 nW. The SFDR was -37 dB. The digital-to-analog converter of this construction consumed less power and chip area. It is suitable for portable device application. . The proposed circuit design simulation can be done using NI-Multisim 13.0 software.**

Keywords: - DAC, SDFR, INL, DNL

I. INTRODUCTION

Our world is not a digital environment of absolutes. The signals of the real world are not made of logical highs and lows, or zeroes and ones. These signals are analog and they meander within a range of voltages or currents. The purpose of the Digital to Analog Converter (DAC) is to convert digital data into an analog signal where the 'real world' exists. The digital data may originate from a microprocessor, ASIC, or FPGA, but at some point it requires conversion to an analog signal to have impact on the real world. Whether the system uses an audio amplifier, or an LED indicator, or a motor driver, the final signal will be analog in nature. The DAC serves as that bridge to transfer a digital signal into the analog domain and hopefully ends with an accurate output signal.

In recent years, the current steering converter is the dominant construction for very high speed Digital to Analog Converters (DAC). The current steering DAC has the advantages of being quite small for resolution below 14 bits, being very fast, and being more cost effective. However, the major drawback is its sensitivity to device mismatch, glitches, and current source output impedance for higher number of bits. For example, its integral non-linearity (INL) and differential non-linearity (DNL) are vulnerable to the accuracy of current sources. Generally, a self-calibrated circuit can be designed to solve these problems, but the circuit will consume more power and require a large chip area.

Current steering DAC has three main designs: Binary Weighted Current Steering DAC Thermometer Coded Current Steering DAC and Segmented Current Steering DAC. In a binary implementation, one bit in the digital input word directly turns a relative current source on or off, and the output sums up all the current sources that are turned on. The current value is proportional to the input binary word. The binary structure is simple and requires less area and less power, as no decoding logic is required. However, its major drawback is its down-graded performance mainly due to glitches at middle code transitions and stringent matching requirement of the current sources.

For example, when the digital input code changes from 0111. . .1 to 1000. . .0, one MSB turn on and all the other LSB's turn off. Glitch will be induced during the switching of input code. It is a limitation of high-speed operation of DAC. Although the die size of a binary weighted converter might be relatively small, its specifications for dynamic performance are stringent. Therefore binary weighting is not suitable for high-speed digital-to-analog conversion.

The thermometer-coded DAC, also called unary DAC, utilizes a number of equally weighted elements. Thermometer-coded DAC is invariably monotonic. When the digital input increases by 1 LSB, one current source is switched from negative to positive, and the analog output always increases with input signal. In comparison, the binary-weighted type manifests poorer dynamic performance than the thermometer-coded type. For a large number of bits, the digital circuits converting the binary code into thermometer code and the number of interconnecting wires become large. This implies a more complex circuit layout. Therefore, the disadvantages of the thermometer-coded DAC are its complexity, consumption of a large area and the larger power requirement of the binary-to thermometer decoders.

The segmented current steering is a very popular approach for designing digital-to-analog converters because it combines the advantages of binary-weighted and thermometer-coded designs. The segmented DAC is commonly to use a thermometer-coded approach for the top few MSB's while using a binary-weighted approach for the

lower LSB's. In this way, the glitch is significantly reduced and accuracy is high for the MSBs. Subsequently, the circuit area is minimized with the segmented DAC (Fig. 1).

II. CONSTRUCTION

The proposed differential mode DAC was formed by two single-ended DAC circuits. The single-ended DAC contained binary-to-thermometer (BT) decoders and current mirror circuits, as shown in Fig. 4. The current mirror circuit contained eight current mirrors of different weighting. Each current mirror is controlled by a 2-bit binary to thermometer code decoder, as shown in Fig. 2. The proposed DAC has the advantage of low chip area. It is owing to low transistor count of this construction. The MOS transistor has larger capacitances in its gate oxide, source and drain. Moreover, less number of transistors has the possibility of less interconnection than those of more transistors. Dynamic power consumption of MOS circuits is proportional to the total capacitances of load and internal node. Low transistor count DAC has the chance for low total capacitances. Therefore, the proposed DAC has more possibility to consume low power.

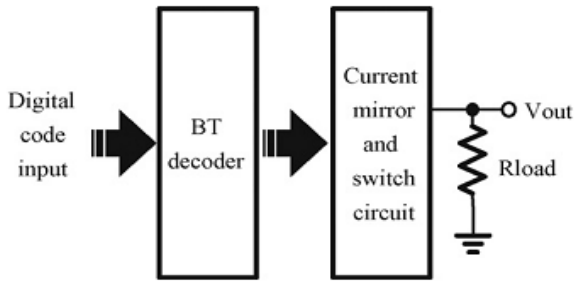

Fig. 1. Single-ended DAC construction

2.1. Binary to thermometer (BT) decoder

Fig. 2 shows the constitution circuit of one 2-bit binary to thermometer decoder. It consisted of one AND gate and one OR gate. S0, S1, and S2 were the control signals for current mirrors. The 16-bit DAC decoder of differential mode required only eight AND gates and eight OR gates.

2.2. Current mirror construction

Fig. 4 shows a single-ended 16-bit DAC. It contained eight BT decoders and eight current mirrors. Each current mirror generated 2-bit DAC.

Fig. 3 depicts the circuit of one 2-bit DAC. The three NMOS transistors, M_2~M_4, were switches that turned on the current path. The three signals, S_0~S_2, were generated by the previous BT decoder stage. I_0 were the drain current of M_0 mirrored from I_1, the drain current of M_1. Transistors M_2, M_3 and M_4 acted as switches. When they were turned on, effective resistance appeared between the drain of M_1 and ground. For example, when the switch was turned on via S_0, the effective resistance of M_2 appeared between the drain of M1and the ground.

There were four thermometric configurations of (S2 S1 S0), namely (111), (011) (001) and (000). For example, if (S2 S1 S0) = (011), then I_1 was the total current drawn by M_2 and M_3. The relationship between I_0 and $I_1$was derived as follows:

$$I_0 = I_1^* \frac{\left(W/L\right)_{M0}}{\left(W/L\right)_{M1}} = \left[\left(S_1 \wedge S_0\right) + \left(S_1\right) + \left(S_1 \wedge S_0\right)\right]\left(I_{unit}\right) \quad (1)$$

Where I_{unit} was the unit output current of the 2-bit DAC when (S2 S1 S0) = (001). The operators ∧, ∨ were the Boolean AND, and Boolean OR, respectively. The I_1, shown in Fig.3, was determined by the parallel resistance of M2, M3 and M_4

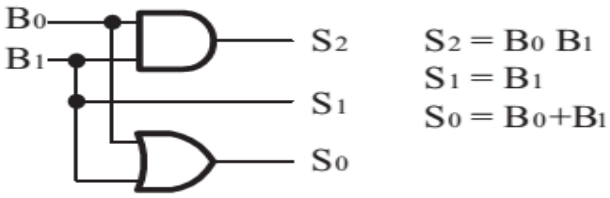

Fig. 2 Two-Bit BT decoder.

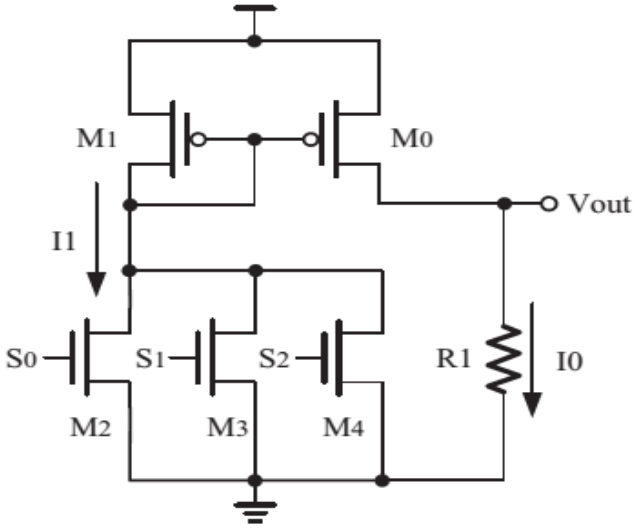

Fig. 3 Current mirror circuits of 2-bit DAC

The current mirrors of the 16-bit single-sided DAC needed 24 NMOS transistors as switches to turn the current on or off. I_{out} collected all the current from current mirrors.

The output I_{out} can be described as follows:

I_{out} = [(B1∧ B0) + (B1) + (B1∧ B0)] (I_{unit})
+ [(B3∧ B2) + (B3) + (B3∧ B2)] (4 I_{unit})
+ [(B5∧ B4) + (B5) + (B5∧ B4)] (16 I_{unit})
+ [(B7∧ B6) + (B7) + (B7∧ B6)] (64 I_{unit})
+ [(B9∧ B8) + (B9) + (B9∧ B8)] (265 I_{unit})
+ [(B11∧ B12) + (B11) + (B11∧ B12)] (1024 I_{unit})
+ [(B14∧ B13) + (B14) + (B14∧ B13)] (4096 I_{unit})
+ [(B16∧ B15) + (B16) + (B16∧ B15)] (16384 I_{unit})

For example, $I_{out} = 3\ I_{unit}$ for $(B1\ B0)_2 = (11)_2$, and $I_{out} = I_{unit}$ for $(B1\ B0)_2 = (01)_2$.

In Fig. 3, the PMOS transistors M_0 and M_1 were used as a basic current mirror. The width of the $M_2 \sim M_4$ transistors were adjusted to obtain a suitable current on M_1.

Different currents were obtained by changing the width of the PMOS M_0. Fig.4 depicts the single-side 16-bit DAC. The DAC required eight different current sources, namely I_{unit}, $4I_{unit}$, $16I_{unit}$, $64I_{unit}$ $256I_{unit}$, $1024I_{unit}$, $4096I_{unit}$, and $16384I_{unit}$. The conventional N-bit thermometer-coded type DAC required at least 2^{N-1} current sources.

The conventional N-bit binary weighted DAC required N current sources. It is the reason of smaller area for the proposed DAC.

The aspect ratio of M_0–M_1 were adjusted to obtain the unit current I_{unit}. $4I_{unit}$, 16Iunit, 64Iunit $256I_{unit}$, $1024I_{unit}$, $4096I_{unit}$, and $16384I_{unit}$ were also determined by adjusting the aspect ratio of M_5/M_6, M_{10}/M_{11}, M_{15}/M_{16}, M_{20}/M_{21}, M_{25}/M_{26}, M_{30}/M_{31} and M_{35}/M_{36}.

Last, a differential 16-bit current mirror DAC were constructed using two 16-bit single-ended current mirror DACs.

Differential mode DAC can increase the linear performance of the proposed construction. Compared to the binary weighted DAC, the construction partially used thermometric code, and slightly decreased the glitch.

III. SIMULATION RESULTS

The differential mode DAC was implemented using CMOS process. The voltage of the circuit was 3.5 V. Which was feed by Agilent pattern generator. Therefore, the sampling rate was set at 350 MHz the output was measured using Agilent oscilloscope. The average INL and DNL were about +0.27/−0.17 LSB and +0.32/−0.1 LSB, as shown in Figs.5 and 6, respectively.

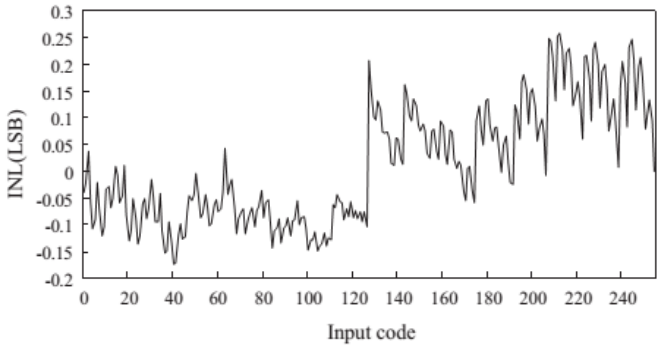

Fig. 5 INL of 16-bit DAC

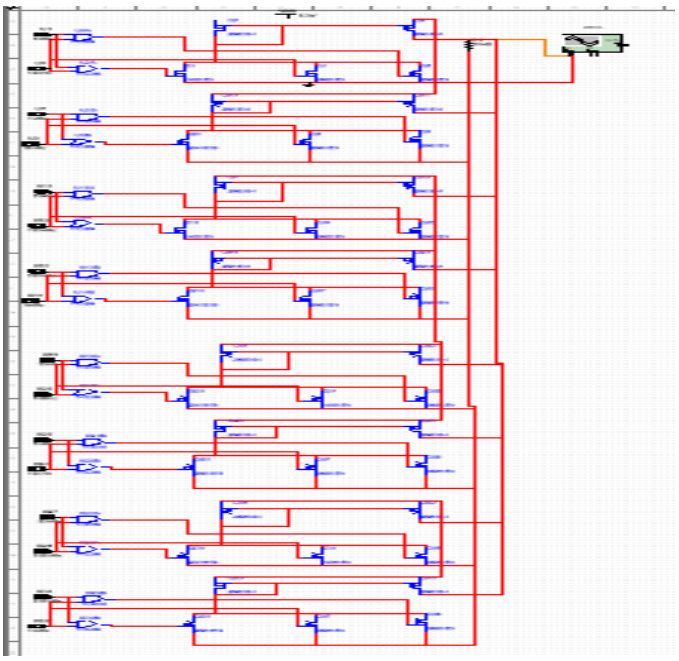

Fig. 4 A 16 bit single-ended current mirror DAC

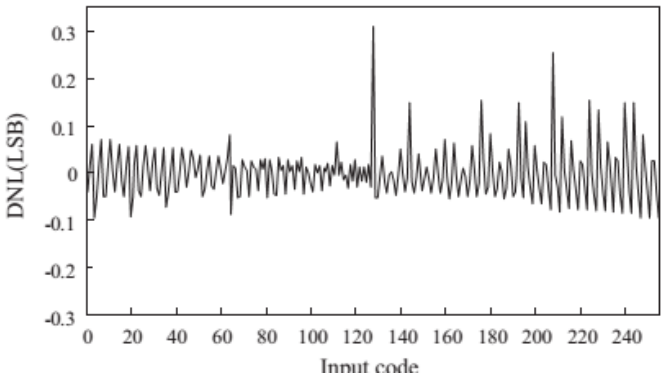

Fig. 6 DNL of 16-bit DAC

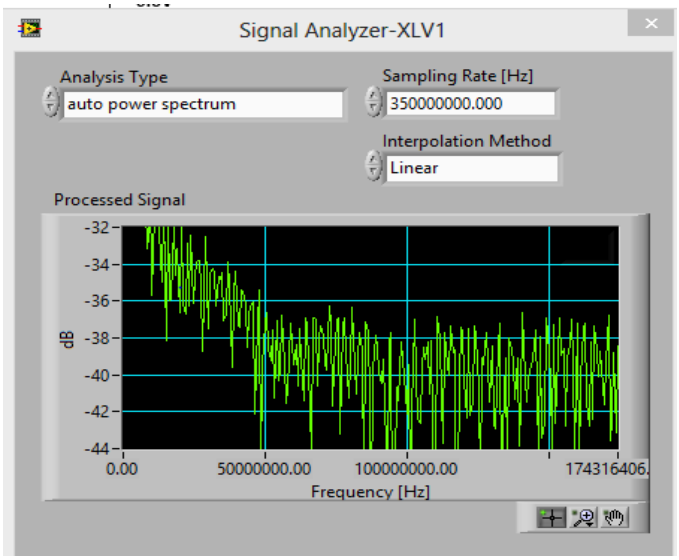

Fig. 7 SFDR (Spurious-Free Dynamic Range)

Spurious-Free Dynamic Range (SFDR) is the strength ratio of the fundamental signal to the strongest spurious signal in the output. It is also defined as a measure used to specify analog-to-digital and digital-to-analog converters (ADCs and DACs, respectively) and radio receivers. SFDR is defined as the ratio of the RMS value of the carrier frequency (maximum signal component) at the input of the ADC or DAC to the RMS value of the next largest noise or harmonic distortion component at its output.

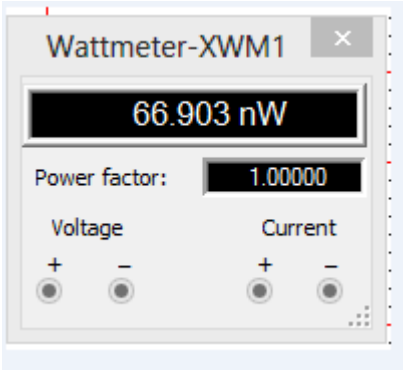

Fig.8 Power

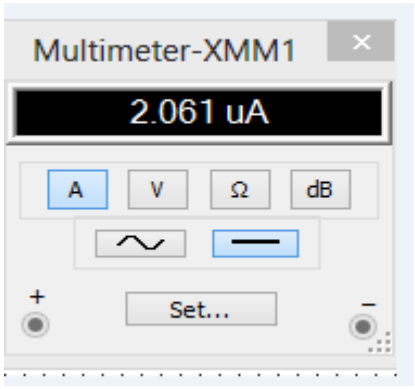

Fig. 9 Current

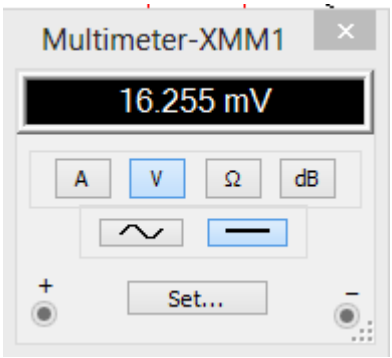

Fig.10 Voltage

Under the sampling rate of 350 MHz, the 2.7 MHz digitized sine waveform was feed into the chip. The SFDR was about -37 dB, as shown in Fig.7 The full-scale output was 16.255 mV. The power consumption was 66.903 nW at the sample rate of 350 MS/s.

VI. PERFORMANCE SUMMARY

Table. 1

Resolution	16 bits
Supply voltage	3.5V
Sample rate	350 MHz
INL	+0.27/−0.17 LSB
DNL	+0.32/−0.1 LSB
SFDR	-37 dB (2.23 MHz@350 MS/s)
Power consumption	66.903 nW
Full scale of output	16.255mV (R_L=1kΩ)
Technology	GDI Logic in CMOS Technology

Table. 1 summarized the specifications averaged of all the DAC chips. The power efficiency is 66.903 nW/ 350MHz It is also the smallest among for CMOS technology.

The core size of the chip is also the smallest one. The reason is that the DAC requires only one current mirror for 2-bit conversion. It is suitable for low power and small-area DAC applications, especially for portable device.

The 16-bit proposed DAC has some interesting characteristics. It requires eight current sources of different weight, i.e., 2^0*Iunit*, 2^2*Iunit*, 2^4*Iunit*, 2^6*Iunit*. 2^8*Iunit*, 2^{10}*Iunit*, 2^{12}*Iunit*, and 2^{14}*Iunit*. However, conventional 16-bit binary-weighted DAC requires 16 current sources of different weight, i.e., 2^0*Iunit*,2^1*Iunit*,….. 2^{14}*Iunit*, and 2^{15}*Iunit*. Therefore, the proposed approach meets less mismatch problem of current sources compared with binary weighted DAC. The conventional 16-bit thermometer-coded type DAC required at least 2^{15} current sources. The proposed 16-bit DAC required only 8 current sources. It is the reason of smaller area for the proposed DAC.

The approach uses thermometric code in 2-bit DAC. It slightly decreases the glitch during digital code switching compared with binary weighted DAC.

The proposed DAC was sensitive to the resistances of M2, M3, and M4 in Fig. 3 The sensitivity of the resistance would degrade the performance of linearity. It is possible the only disadvantage.

V. CONCLUSION

Most physical variables are analog in nature. Quantities such as temperature, pressure and weight can have an infinite number or values. Converting an analog value to a digital equivalent (binary number) is called digitizing the value. Such operation is performed by an Analog-to-Digital Converter (ADC). After processing the digital data, it is often necessary to convert the results of such operation back to analog values; this function is performed by a Digital-to-Analog converter (DAC). The Multiuse simulator is a useful tool to perform theoretical and practical experiments to

improve understanding of the various electronic concepts. It is also helpful to design and program embedded system applications in our further research work. It also can debug, execute verify results before real time implementation. Experiments were performed on A 16-bit differential mode current steering DAC is proposed in this paper. The DAC was implemented using GDI Logic in CMOS Technology. Eight different unit current mirrors were used to form the 16-bit DAC. The full-scale output was 16.255 mV. The DAC consumed 66.903 nW for 2.23 MHz analog signal at 350 MS/s. The INL and DNL were +0.26/−0.17 LSB and +0.31/−0.09 LSB, respectively. Therefore, the circuit was found to consume less power and core area. It is suitable for low power and small-area DAC applications, especially for portable device.

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