International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 1 Issue 8, October - 2012

Design of a Low Power Four-Bit Binary Counter Using Enhancement Type Mosfet

Praween Sinha
Department of Electronics & Communication Engineering
Maharaja Agrasen Institute Of Technology, Rohini sector -22, Delhi 110085, India

Shreyaansh Srivastava
Department of Electronics & Communication Engineering
Northern India Engineering College, FC-26, Shastri Park, New Delhi 110053, India

Abstract

Digital positioning systems often require a down counter for their operation. Due to the necessity of particular logic sequences and control of individual terminals, the design of counters for particular use is very essential. In this paper the design procedure and logic diagram for a synchronous binary counter is presented. The main objective of this paper is to provide new low power solution for Very Large Scale Integration (VLSI) designers. Especially, this work provides a challenge to exploit the topological features of MOSFET. Various techniques at the different levels of the design process have been implemented to reduce the power dissipation at the circuit, architectural and system level.
Furthermore, the number of gates per chip area is constantly increasing, while the gate switching energy does not decrease at the same rate, the power dissipation rises and heat removal becomes more difficult and expensive. To limit the power dissipation, alternative solutions at each level of abstraction are used.
The dynamic power requirement of CMOS circuits is rapidly becoming a major concern in the design of personal information systems and large computers. In this project work, a new CMOS logic style called Gate Diffusion Input (GDI) is discussed. GDI's basic cell is very similar to basic CMOS logic style but it enables us to design complex functions with fewer gates as compared to CMOS, further reducing the power consumption of/by the circuit.

***Keywords*-Gate Diffusion Input (GDI), AND Gate, Binary Counter, T flip-flop, XOR Gate**

1. INTRODUCTION

Circuit design plays an important role in the design of digital circuits like counters. First, to guarantee the counter to work at the desired clock rate, the designer has to know the delay of critical path and the required time of inserting a pipeline stage. Second, to reduce the area of the counter, several architectures of counter are investigated [1]. Circuit analysis helps the designer verify the functions and performances of the counters. The architecture of the counter has to be determined first. Thereafter, the number of the pipeline stages can be decided by the speed of the counter. The size of the circuit should be as small as possible if all the requirements can be met [5].

Fast airthmetic requires fast circuits. Fast circuits require small size to minimize the delay effects of the wires. Small size implies a single chip system to minimize input/output delays [2]. The increasing demand for low-power VLSI asks among other, for power efficient logic styles. Performance criteria for logic style are circuit speed, circuit size, power dissipation, and wiring complexity as well as ease-of-use and generality of gates in cell-based design techniques. Dynamic logic styles are often a good choice for high speed, but not for low-power circuit implementations due to the high node activity and large clock loads.

After guaranteeing correct digital functionality, the primary consideration for system designers has always been speed. A circuit is specified to operate at a particular delay, otherwise the entire system may not work; further reduction is beneficial but not strictly necessary. Other factors may have equal or greater importance than power dissipation; area of implementation and reliability issues are subjects which designer must take into account. It's worth to note that power reduction techniques are not necessarily negatively corrected to delay reduction.

For example, one method to reduce delay in a circuit's critical path is to upsize the driving strength of gates, which results in increased power reduction. However, reducing interconnect capacitance, which is another way to lower delay, reduces both power and delay. Generally, great power savings can be achieved if delay is not an issue, but optimizing power without delay consideration is insignificant [3].

A Flip-flop is the name given to two-state devices which offer basic memory for sequential logic operations. Flip-flops are synchronous bi-stable devices that operate as memory elements [6]. A flip-flop circuit contains two outputs, one is for the normal value and the other is for the complement value of the stored bit. Flip-flops are used for digital data storage and transfer and are commonly used in banks called "registers" for the storage of binary numerical data [4].

Counters are designed using flip-flops. Counters can be classified as synchronous and asynchronous counters based on the application of clock to the flip-flops. A synchronous counter is clocked by a single clock for all the stages and the output for each stage changes at the same time. In an asynchronous counter the output from the previous stage is given as the clock for the next stage so that the output ripples across each stage to reach the final count [4].

A.4 BIT BINARY COUNTER

A 4-bit binary counter has 16 possible states, in other words it counts from 0 to 15 up/down [4]. That is, it counts from 0000 through 1111 and again rolls over to 0000 again**.**

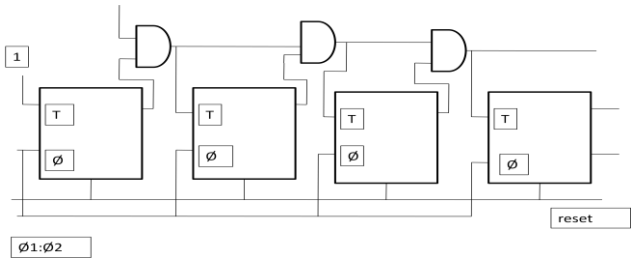

Fig. 1. 4-bit binary counter.

TABLE I
Font Sizes for Truth Table of the 4-bit Counter with Reset and Carry-out

RESET	States					Count
	CLA (carry-out)	F3	F2	F1	F0	
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
0	0	0	1	0	0	4
0	0	0	1	0	1	5
0	0	0	1	1	0	6
0	0	0	1	1	1	7
0	0	1	0	0	0	8
0	0	1	0	0	1	9
0	0	1	0	1	0	10
0	0	1	0	1	1	11
0	0	1	1	0	0	12
0	0	1	1	0	1	13
0	0	1	1	1	0	14
0	1	1	1	1	1	15
1	0	0	0	0	0	0

At circuit level, an optimized design is desirable having less numbers of transistors, small power consumption and adequate output voltage swing [7]. In the current work a 4-bit binary counter with D flip-flop and XOR gate using GDI technique has been proposed. The rest of paper is organized as follows: In section 2 three T flip-flops using D flip-flop and XOR gate using GDI technique have been reported. In section 3 results of proposed T flip-flop cell have been combined with AND gate and resulting counter is 4-bit binary counter. Section 4 concludes the work.

2. DESIGN OF PROPOSED T FLIP-FLOP

We have proposed a new design of the counter using the cells of T flip-flop. For T flip-flop we propose the use D-flip flop as a base. The D flip-flop here was formed by the combination of transmission gate and two inverters. The input to the transmission gate transfers logic 1 as a strong logic through NMOS and logic 0 as a strong logic through PMOS in the transmission gate. The output of the transmission gate is given into the inverter which results in an inverted output. The inverted output was again given to the inverter and the output of this inverter is said as the output of D flip-flop.

But here, the feedback is also provided through the transmission gate and the output of this transmission gate was given to the first inverter. This transmission network is known as feedback transmission gate. The D flip-flop passes the input as the output, but after some delay. The output of the D flip-flop is given as an input to the XOR Gate with another input and the output of XOR gate was given as an input to the D flip-flop. This whole arrangement acts as the T flip-flop.

A. LAYOUT DESIGN OF XOR GATE

The layout design of XOR Gate is designed using the TANNER TOOLS (L-Edit). Here the XOR Gate is designed using Gate Diffusion Input (GDI) technique of low-power digital combinatorial circuit design. This technique allows reducing power consumption, propagation delay, and area of digital circuits maintaining low complexity of logic design.

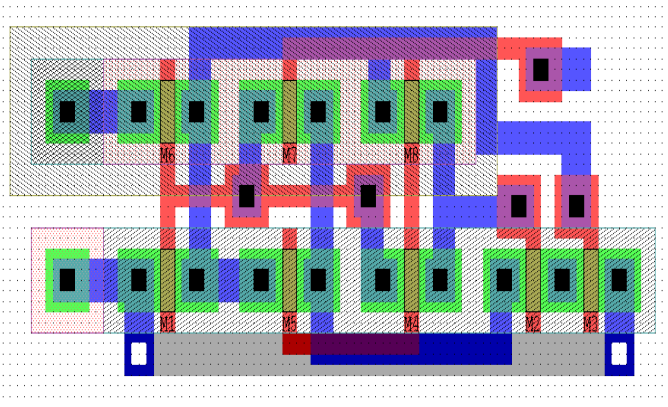

Fig. 2. Layout of the XOR Gate.

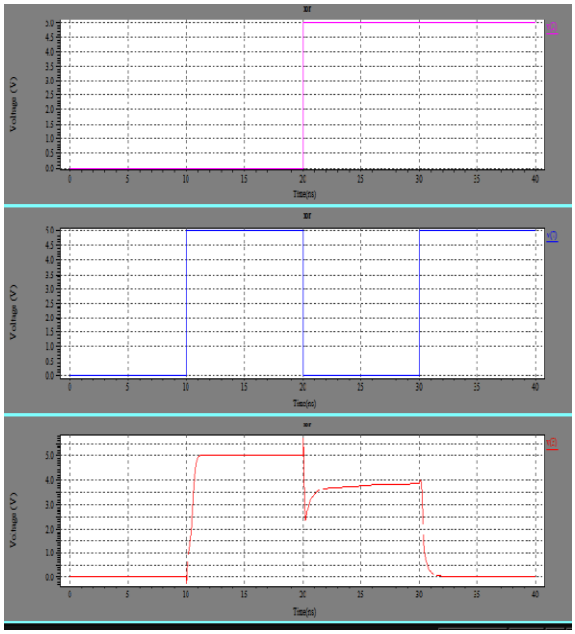

Fig.3. Simulation result for XOR Gate.

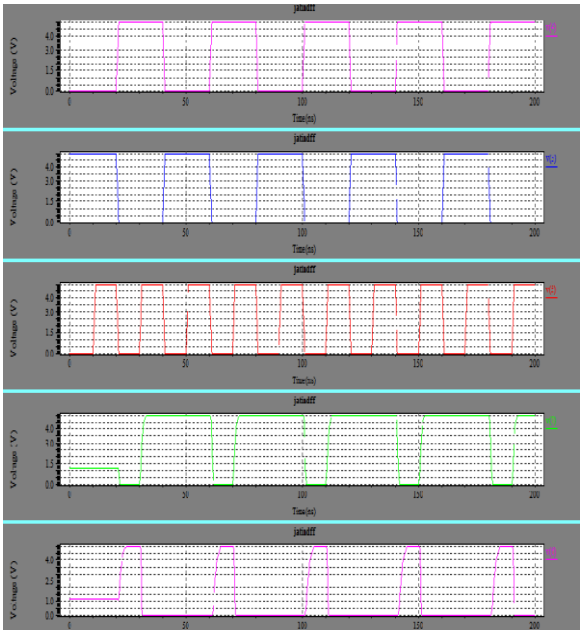

Fig.5. Simulation result for D flip-flop.

B. D FLIP-FLOP

The D flip-flop was formed by the combination of two transmission gates and two inverters. The input to the transmission gate & the output of the transmission gate is given into the inverter which gives an inverted output. The inverted output was again given to the other inverter and the output of this inverter is said to be the output of D flip-flop.

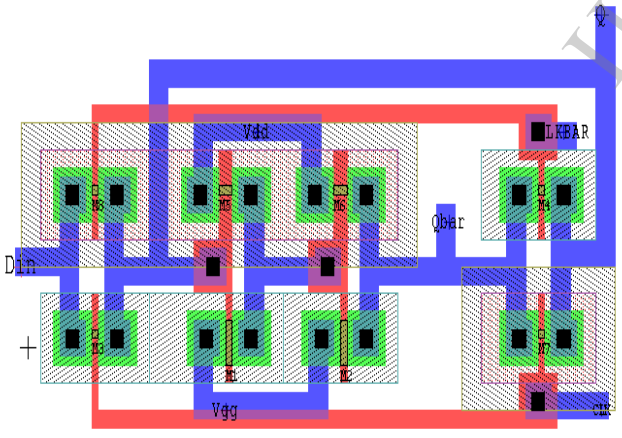

Fig. 4. Layout of the D flip-flop.

C. T FLIP-FLOP

The output of the D flip-flop is given as an input to the XOR gate with another input and the output of XOR gate was given as an input to the D flip-flop. This whole arrangement is the T flip-flop. We need to design the circuit to generate a triggering signal T as a function of D and Q: D = f (T, Q) Consider the excitation table:

Q_N	Q_{N+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Treating T as a function of D and current FF state Q(t), we have T =D Q' + QD'

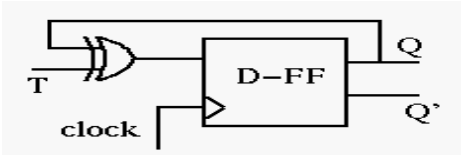

Fig.6. Toggle flip-flop.

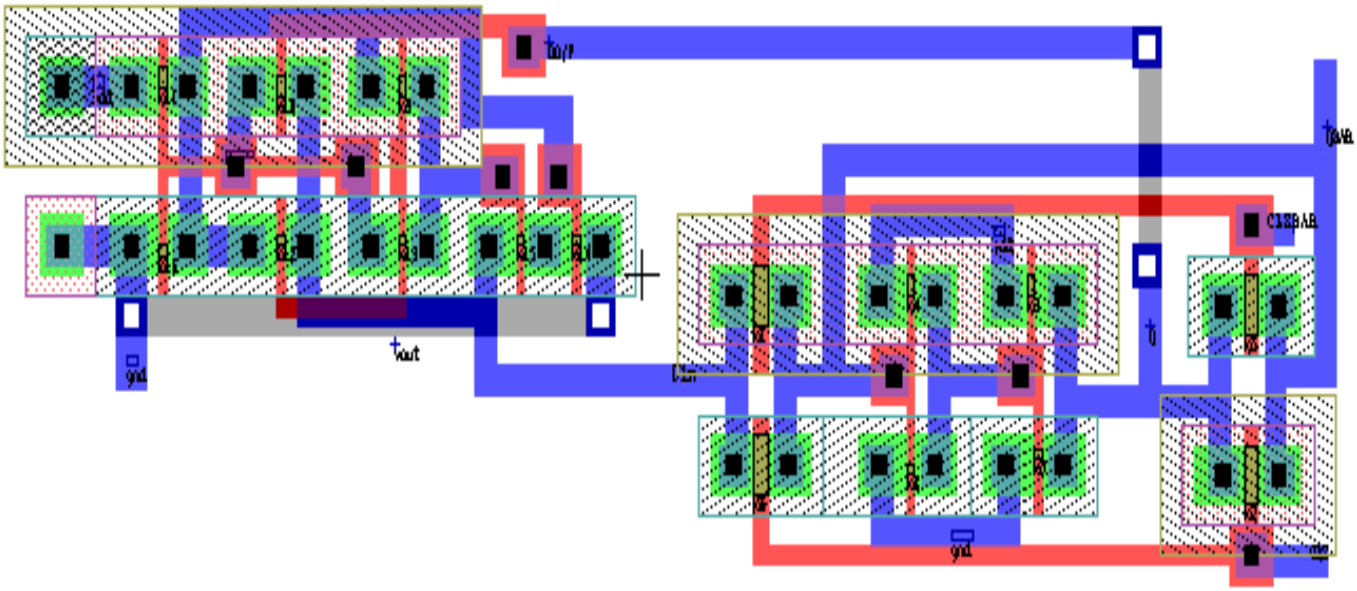

Fig.7. Layout of the T flip-flop.

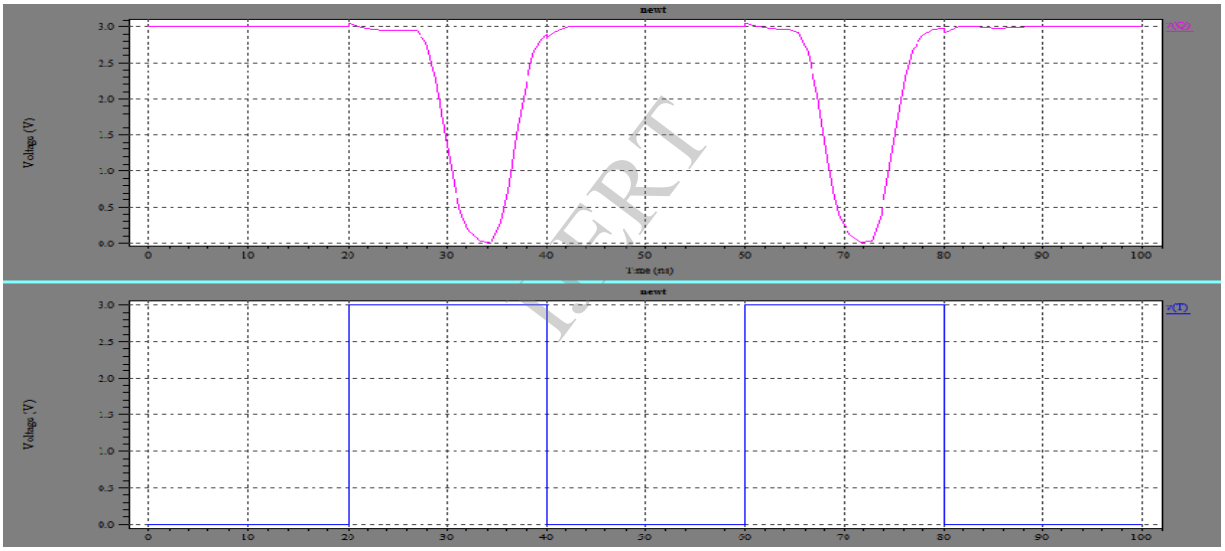

Fig.8. Simulation result for T flip-flop.

3. DESIGN OF THE PROPOSED 4-BIT BINARY COUNTER

In this section, the proposed counter is developed by combining the T flip-flop proposed above along with the gates mentioned at all states to form a 4-bit binary counter.

Following figures show the layout of the proposed 4-bit binary counter and its simulation results.

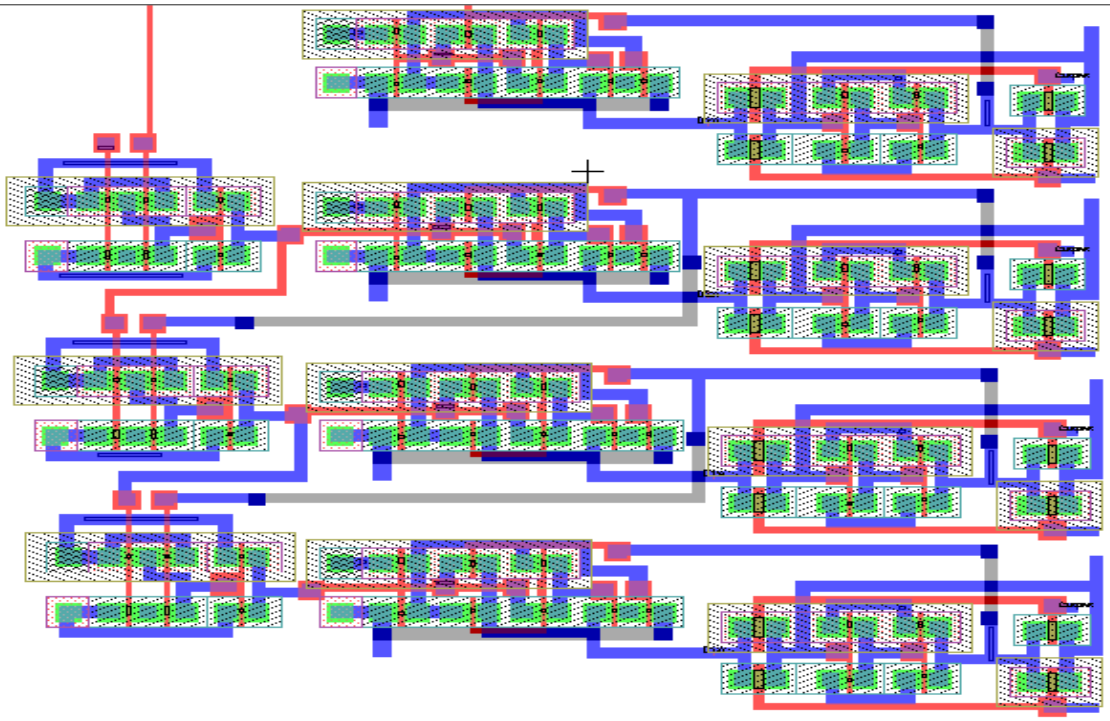

Fig. 9. Layout of the proposed 4-bit binary counter.

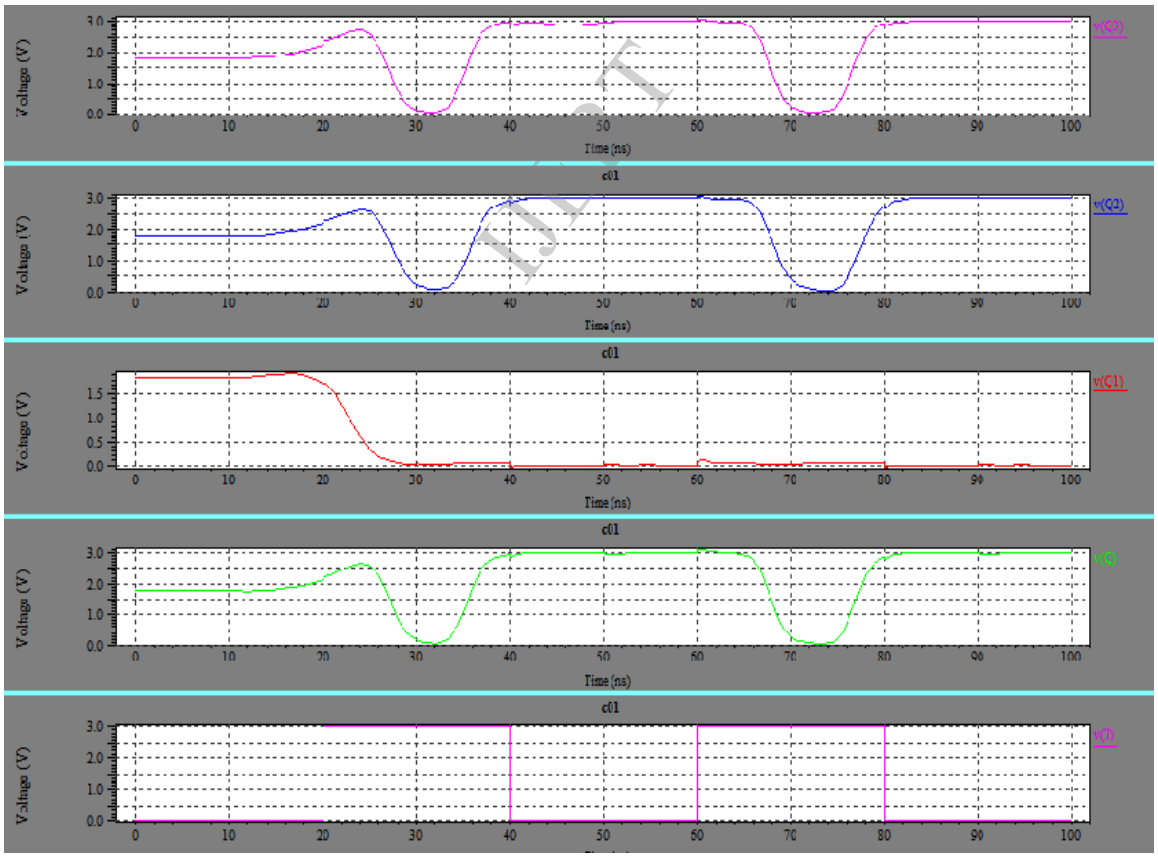

Fig.10. Simulation result for the proposed 4-bit binary counter.

TABLE II
SPECIFICATIONS OF THE PROPOSED 4-BIT BINARY COUNTER

SPECIFICATION	VALUE
Maximum clock frequency	476 MHz
Maximum rise time	2.1 ns
Maximum Fall Time	2ns
Maximum Propagation Delay without load	2.1ns
Maximum Capacitive load before Distortion	300x10-15 F
Technology Used	1um
Operating Voltage	3V

4. CONCLUSIONS

In the current work, a new low power 4-bit binary counter with three T flip-flops is developed using D flip-flop, XOR gate, AND gate and GDI technique. The reported counter works at a voltage of 3V. Compared to the earlier reported 4-bit binary counter, the proposed circuit clearly shows qualitative characteristics such as reduced power consumption and better output signal levels. Also, the new circuit design fairly reduces the transistor count in comparison to the earlier counter.

5. REFERENCES

[1] N.H.E. Weste, "Principle of CMOS VLSI Design" Addison-Wesely 1998.
[2] Neredimelli V V P Hide, Dr. I. Santi Prabha, "Design of Modulo 2n-1 based on Radix-8 Algorithm for RNS & MAC Applications, International Journal of Research in Computer and Communication Technology.
[3] Pascal Constantin Hans Meier, "Analysis and Design of Low Power Digital Multipliers".
[4] M.Moris Mano, "Digital Design", Prentice Hall, 1994.
[5] Phillip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford University Press, 2006.
[6] J.Rabaey and A.Nikolic and A. Chandrakasan, "Digital Integrated Circuits: A Design Perspective" Prentice Hall 2003.
[7] Sung-Mo Kang and Yusuf Leblebici, "CMOS Digital Integrated Circuits", McGraw-Hill, 2003.