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Design of a Low-Power Redundant-Transition-Free TSPC Dual-Edge-Triggering Flip-Flop with a Single-Transistor-Clocked Buffer Enhanced by LECTOR

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***Abstract*—In the current era dominated by graphics processing units (GPUs) and artificial intelligence (AI), the flip-flop (FF) has emerged as a significant consumer of power within processors. To tackle this challenge, a groundbreaking solution is introduced: a novel single phase-clock dual-edge-triggering (DET) FF utilizing a single-transistor clocked (STC) buffer (STCB). This innovative STCB employs a solitary clocked transistor in the data sampling pathway, effectively eliminating redundant clock transitions (RTs) and internal RTs inherent in conventional DET designs. Through rigorous post-layout simulations conducted on 22 nm fully depleted silicon on insulator (FD-SOI) CMOS technology, the proposed STC-DET demonstrates superior performance in power consumption compared to existing low-power DET designs, particularly under high switching activity. Additionally, it achieves the most favorable power-delay-product (PDP) among DET implementations. Leveraging the LECTOR Technique, this advancement significantly reduces power consumption while maintaining optimal functionality.**

***Keywords*—Dual edge triggering (DET),dynamic power , flipflop, LECTOR**

I. INTRODUCTION

In the realm of CMOS digital design, power consumption stands out as a critical concern, particularly given the increasing demands from GPUs and AI processors. With AI training processing power doubling approximately every 3.4 months, the pressure to address power dissipation is mounting. A significant portion, up to 50%, of a modern CPU's power is allocated to its clocking system, making power optimization a pivotal focus.

Within a processor's clocking system, flip-flops (FFs) and clock distribution networks play vital roles. Traditional single-phase clock FFs, by processing only one clock edge at a time, incur unnecessary power overhead, especially when the other clock edge remains active, a limitation stemming from insufficient data processing development. In contrast, dual-edge-triggering (DET) FFs capitalize on both clock edges to process data, thereby halving the clock frequency while maintaining throughput.

To further mitigate power consumption, a novel DET FF topology employing a true single-phase clock (TSPC) is proposed. Various low-power latches, flip-flops, and methodologies have been suggested. In DET FFs, a notable power consumption issue arises from clocked transistors causing redundant power overhead when input data remain static, yet certain transistors in the circuit remain active due to its topology.

Single Transistor Clock Dual Edge Triggering (STCDET) enhances clock signal efficiency and performance in digital circuits. By leveraging both rising and falling edges of the clock signal, STCDET doubles the effective clock frequency, thereby accelerating operations without requiring significant circuitry modifications. This technique finds applications across diverse digital systems, including high-speed processors and data communication systems, where maximizing clock frequency is paramount for efficiency.

II. LITERATURE REVIEW

Previous research has extensively explored the design and optimization of flip-flops and latches, critical components in microprocessor design, focusing on aspects of delay and energy efficiency.[1] Various studies have compared different flip-flop designs, highlighting trade-offs between speed and energy consumption. One study compared several single edge-triggered flip-flop (SET-FF) designs, showcasing the balance between speed and energy consumption.

Another proposed a novel fully static true-single-phase-clocked dual-edge-triggered flip-flop (DET-FF) for IoT applications, emphasizing its reliability and energy efficiency, particularly in low-voltage regimes. [2]Additionally, a study introduced a DET-FF with a true-single-phase clock, addressing clock overlap issues and achieving robust operation at low voltages. DET flip-flops have garnered attention for their potential in low-power, high-performance designs. Studies have shown promising results in energy efficiency with minimal complexity overhead compared to conventional single edge-triggered flip-flops. Researchers have proposed techniques such as clock branch-sharing schemes to reduce power consumption in DET-FFs, resulting in improvements in power efficiency and power-delay-product (PDP). Reduced implementation DET-FF circuits with fewer transistors have also been introduced, offering practical and economic advantages in VLSI system design. Continued advancements in DET flip-flop design have aimed at mitigating challenges such as clock overlap and glitch energy.

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Various techniques for low-power clocking systems, including clocked pair shared flip-flops, significantly reduce clock load and driving power. [3] Novel static DET flip-flops using C-elements have exhibited low energy dissipation and superior characteristics in power and PDP. These designs have been validated through simulation and demonstrate robustness under process, voltage, and temperature (PVT) variations. Overall, the literature underscores the importance of flip-flops and latches in microprocessor design, particularly in optimizing for speed, energy efficiency, and reliability. From single edge-triggered to dual edge-triggered flip-flops, researchers have explored various design strategies to address specific challenges such as clock overlap, glitch energy, and low-voltage operation. These advancements offer promising avenues for improving the performance and energy efficiency of microprocessors, essential for meeting the demands of modern computing systems

III. DESIGN METHODOLOGY

In CMOS circuits, the reduction of the threshold voltage due to voltage scaling results in an increase in subthreshold leakage current, leading to higher static power dissipation. Our proposed technique, called LECTOR, offers a novel approach to designing CMOS gates, significantly reducing leakage current without increasing dynamic power dissipation. The core of this method involves integrating two leakage control transistors (one p-type and one n-type) within the logic gate, where each transistor's gate terminal is controlled by the source of the other. This configuration ensures that one of the transistors is consistently "near its cutoff voltage" for any input combination, thereby increasing the resistance along the path from V/sub dd/ to ground and resulting in a significant decrease in leakage currents. The process involves converting the gate-level netlist of the given circuit into a static CMOS complex gate implementation, followed by the introduction of leakage control transistors to achieve a leakage-controlled circuit. Notably, LECTOR operates effectively in both active and idle states of the circuit, offering superior leakage reduction compared to alternative techniques.

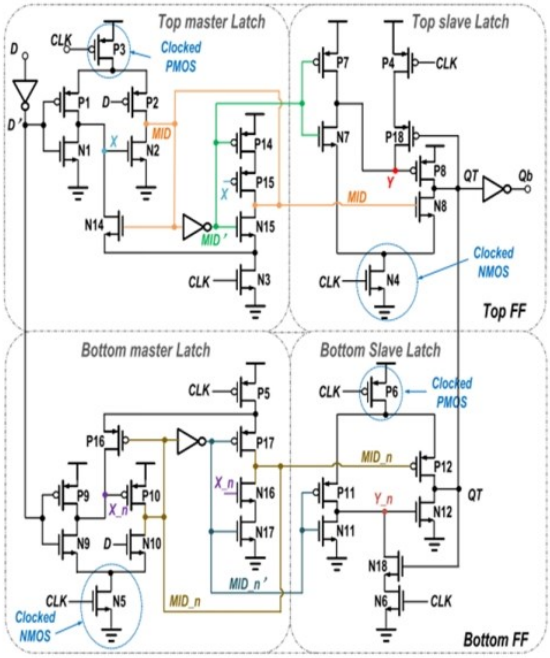

Fig.1 TSPC single transistor clocked DET, STC-DET.

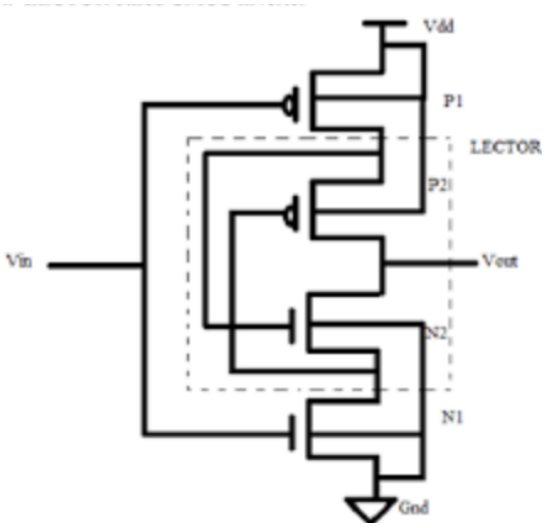

Fig.2 Lector Schematic

In the operation of the Top FF in STC-DET, when CLK is low, transistors P2 and N2 act as a virtual inverter. During this time, the clocked PMOS P3 in the top master latch turns on, changing node X to D". However, in the top slave latch, NMOS N4 remains off due to the low CLK, keeping node Y high, thus keeping PMOS P8 off. Consequently, the input proceeds to MID in the top master latch. As a result, the QT of the top FF remains floating.

A negative-triggered STCB is constructed using transistors N1, N2, P1, P2, and P3, with the sole timed transistor P3 serving as the signal sampling channel. Unlike FN_C DET and FS-TSPC, STCDET lacks the RT between a clocking PMOS and a clocking NMOS. Additionally, a clock-driven NMOS transistor, N3, is present in the top master latch, serving as a keeper rather than part of the data sampling path. Transistors P3, N4, N5, and P6 form the clocking path and are all on the data sampling path.

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Another positive-triggered STCB is constructed in the top FF using transistors N4, N7, N8, P7, and P8.
When CLK is high, the routes connected to P1 and N2 in the top master latch are off because clocked PMOS P3 is off. The logic state of MID is maintained by the keeper. Keeper transistors maintain X while it is low. However, in the top slave latch, the timed NMOS N4 turns on, making Y equal to MID", which is essentially MID. As a result, the signal from MID travels to QT due to transistors N8 and P8 acting as a virtual inverter, activating the top FF at the positive edge of the clock.
In the operation of the Bottom FF in STC-DET, the clock NMOS in the bottom master latch turns off when CLK is low. Consequently, the routes connected to N9 and P10 are inactive, and the keeper maintains the logic state of MID_n. Similarly, if X_n is high, the keeper maintains that state. However, in the bottom slave latch, when CLK is low, the timed PMOS turns on, transforming Y_n into MID_n", which is essentially MID_n. Therefore, P12 and N12 act as a virtual inverter, and the signal from MID_n appears at QT just before the clock's falling edge, engaging the bottom FF at the negative edge of the clock.
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IV.RESULTS AND DISCUSSION

The Figures shown below is the Output for STCDET Using LECTOR.

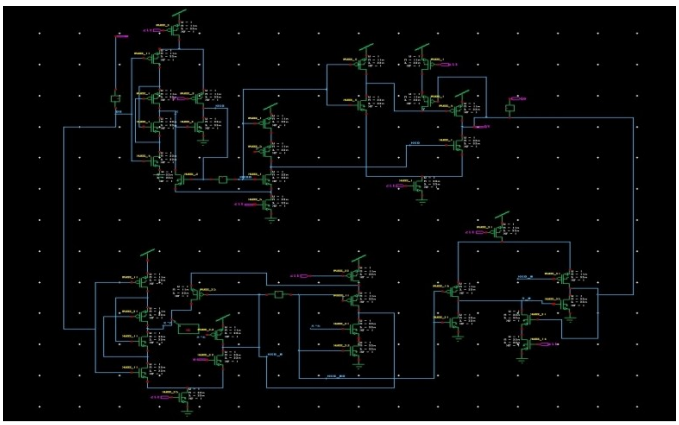

Fig.3 Schematic for STCDET Using LECTOR

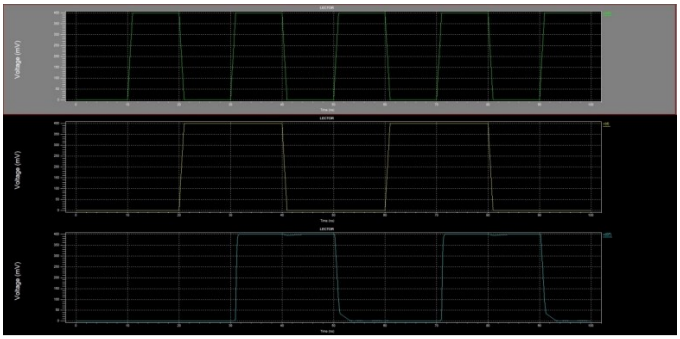

Fig.4 Waveform for STCDET Using LECTOR

```
*   Device and node counts:
*                MOSFETs - 54
*                   BJTs - 0
*                MESFETs - 0
```

Fig.5 Area of transistors in Lector method

```
Power Results
vl from time 0 to 1e-007
Average power consumed -> 1.206081e-007 watts
Max power 1.861622e-006 at time 3.1223e-008
Min power 1.793915e-008 at time 4e-008
```

Fig.6 Power Consumed in Lector method

```
delay = 2.0820e-008
   Trigger = 1.0250e-008
   Target  = 3.1070e-008
```

Fig.7 Delay in Lector method

COMPARISION TABLE :

Method	AREA	POWER	DELAY
Existing	42	1.886586e-007W	2.0205e-008
LECTOR	54	1.206081e-007W	2.0820e-008

V. CONCLUSION

A novel low-power redundant-transition-free dual-edge-triggered FF, named STC-DET, is introduced, utilizing STC buffers to completely eliminate RT in dual-edge-triggered FFs. The positive-triggered and negative-triggered STC buffers each incorporate only one timed transistor in the data sampling circuit, eliminating all clock redundant components and internal redundant transitions present in previous DET systems. Moreover, STC-DET exhibits no power dissipation controversy. Among all DET designs, STC-DET consumes the least amount of power across various voltages and process corners for switching activity. In summary, among state-of-the-art DET FFs, STC-DET achieves the lowest power consumption within the average switching activity range. Additionally, implementing the LECTOR approach in STCDET could further reduce power consumption.

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