International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 4 Issue 10, October-2015

Design of a Single Tail Comparator on a 90nm Technology

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Abstract: **Electronic devices such as mobile phones have found an increase in usage in day to day life due to their portable nature. Consumption of power is one of the problems faced by mobile phones that affect the battery life. This must be scaled down to obtain increase in functioning and extend their time of usage. Analog to digital conversion is done by the comparator in the circuit. In this paper, we present the functioning analyses of a single tail comparator on a 90 nm technology. Important parameters involved are speed and power consumption. Cadence design tools are used to perform simulation analyses on the comparator using 90nm technology.**

Keywords: ADC, Cadence, Spice, 90nm

I. INTRODUCTION

In a high speed Analog to Digital Conversions (ADC) comparators play a major role during the operation. An operational amplifier is one of the most commonly used devices in electronic circuits. An operational amplifier with open loop configuration is called as a comparator. Comparators are majorly used in open loop configurations without a feedback. A comparator is a device which performs comparison operation on the two given analog inputs and converts them into a single digital output. The obtained digital output depends on the equivalent value of the given analog input. Due to less power consumption and high speed performance, comparators have found majority of applications in ADC circuits. Most importantly is the use of one bit comparator. The overall performance of the ADC's depend on the speed of the circuit, less static power consumption and reduction of offset voltages. Pre-amplifiers were used in the circuits before which had high offset voltages. To eliminate this problem clock tail comparators are introduced which reduce the offset voltages, power consumption and increase the speed.

II. COMPARATOR OPERATION

A comparator takes two analog inputs and gives a single digital output. Suppose Vp and Vn are two analog inputs and Vo is the digital output.
VDD is the input dc voltage.

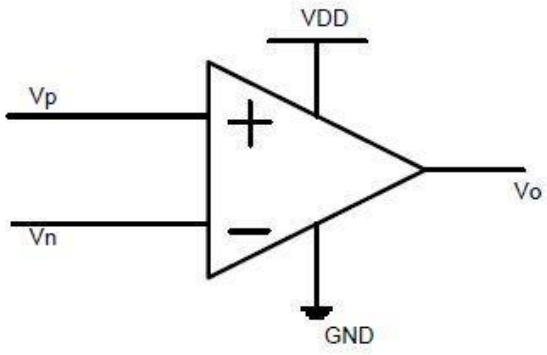

Fig 1 - Schematic of comparator [1]

If potential of Vp is greater than that of Vn then the output Vo has logic 1. If Vp potential is less than that of Vn then the output Vo has logic 0.The comparator used here works only on the difference in input voltages and does not function if the input voltages are equal. For this comparison a pulse voltage is applied at Vp and a reference dc voltage is applied at Vn. Vo has a value of logic 1 if the pulse voltage is greater than reference voltage. This can be observed from graph.

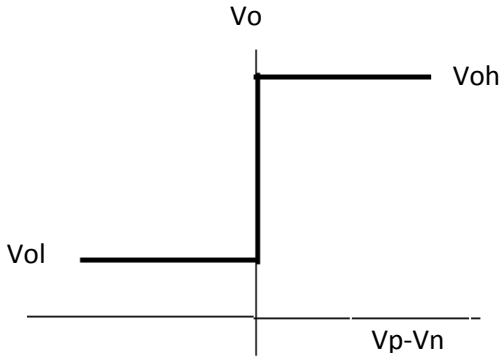

Fig 2 -Voltage transfer characteristics of ideal comparator

Most commonly used comparators are Op amps, Regenerative comparator, Single tail comparator etc. A comparator with no feedback which is called an Op Amp. A Regenerative comparator uses positive feedback to compare magnitude of two signals. A single tail comparator has a transistor tail attached to its circuit with clock input.

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III. TOOL DESCRIPTION

Cadence tools using full custom VLSI design is implemented. It starts with MOS transistor level design entry using Schematic/Symbol/Simulation. The simulation is done for transient analyses using SPICE model files. The following order is implemented:
Design entry – MOS transistor level design entry – Library – GPDK 90nm

A. Schematic Capture

The transistor level schematic is designed by using CMOS logic. This consists of pull up network with PMOS transistors connected between VDD and GND. The schematic design is entered by using Virtuoso(R) Schematic Editor- XL 6.1.6

B. Create Symbol

The symbol view of a circuit module is an icon that represents the collection. It is generated using Virtuoso(R) Symbol Editor – XL 6.1.6

C. Simulation using Test Bench

The simulation for any CMOS design can be designed by using schematic symbol with defined input voltage/current and sinusoidal/non sinusoidal sources based on type of output analyses. Test bench schematic entry is done using Virtuoso(R) Schematic Editor- XL 6.1.6. The simulation results can be analyzed using Transient and another responses based on selected design input. The design functionality is verified by sepetre SPICE simulation tool Virtuosos(R) Analog Design Environment – XL- 6.1.6

III. Single Tail comparator

A. Circuit design

The single tail comparator circuit diagram is shown below [2]

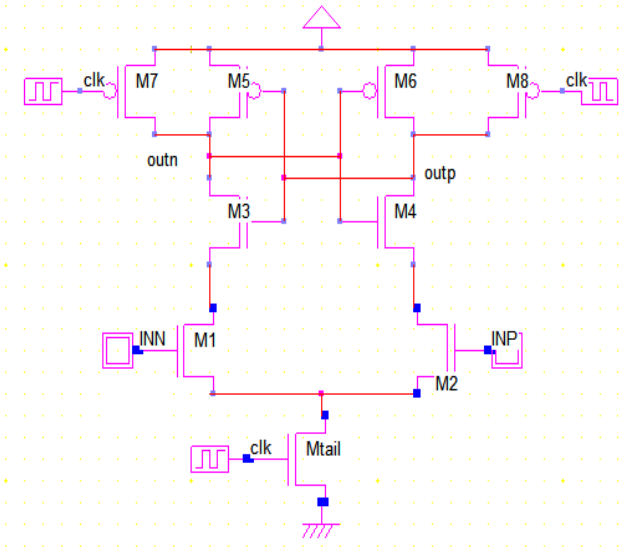

Fig 3 - Single tail comparator

The entire process of designing the circuit is done using the cadence software. The circuit uses four PMOS transistors and five NMOS transistors including the tail transistors. Transistors are placed and connections are made using the wires and respective inputs and outputs are given. The circuit consists of three inputs namely CLK, INN, INP and two output outp and outn where INN and INP are input at n and p nodes, and CLK is the input, outp and outn are outputs at n,p nodes.

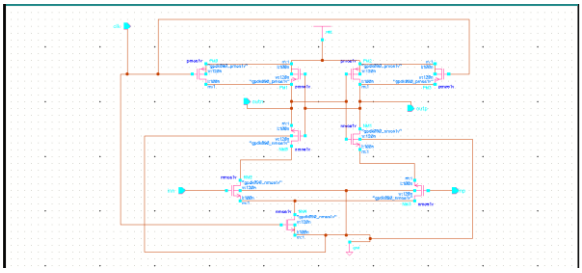

Fig 4 - Schematic of a single tail comparator

B. Symbol Creation

The entire schematic is converted into a symbol which represents the circuit diagram. Now this symbol is used in the test bench construction to generate the required waveforms.

Fig 4 - Symbol of a single tail comparator

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C. Test bench Design

The symbol is included in the test bench area and the required input and output pins are given. A 1v dc voltage is applied to the VDD and the other pin is grounded. Clock pulses are given to the inputs and the circuit is simulated to get the output waveforms.

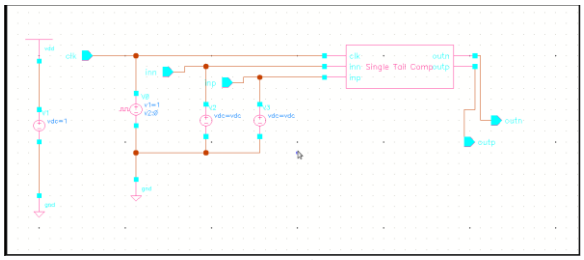

Fig 5 – Test Bench of a single tail comparator

D. Working

The tail transistor present controls the circuit functioning. The clock provided improves the functionality of the circuit as it controls the transistors switching them ON and OFF. The comparator circuit works in two phases namely comparison phase and reset phase. The comparison occurs only when clock value is one. The transistors M (3,4,5,6) work as a regenerative latch which provides feedback to the circuit. The outn node acts as as input to M6, M4 transistors and outp node acts as input to M5, M3.

Initially CLK=0 is given to the transistors. The M tail transistor gets OFF and the transistors M7, M8 are ON. The nodes outn and outp are charged to VDD and logic 1 occurs at both the nodes. This is called Reset phase. Here the output values do not depend on the INN and INP values.

Now CLK=1 is given to the transistors. M tail gets ON and corresponding M7 and M8 gets off. Input values INN=1 and INP=0 are given. Outn and outp start discharging to VDD-(PMOS threshold value). Hence M5 gets ON that results in latch generation of the inverters M3,M5;M4,M6. Since INN>INP that implies VINN>VINP and M1 gets ON, M2 gets OFF resulting in grounding of the voltage at outn and maximum voltage at outp. The reverse occurs when INN<INP i.e., outn>outp. This is called Comparison phase of the circuit.We can observe that outn= ~INN, outp= ~INP.

When both the input values are one, the output values become zero as the voltages at both the nodes is grounded.

E. Waveforms

The following waveforms are obtained after performing the simulation with various input values.

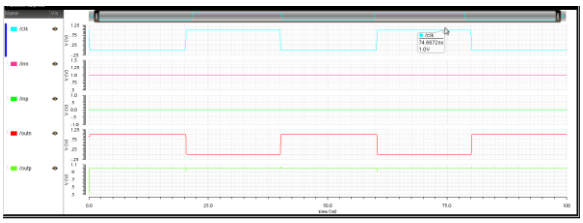

Fig 6.1 – INN>INP : Comparison phase outn<outp

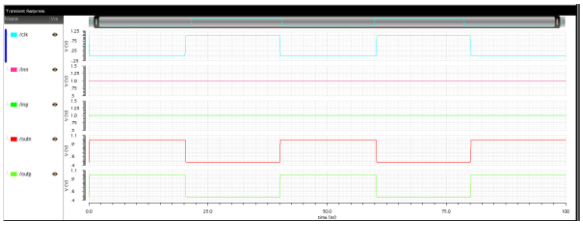

Fig 6.2 – INN=INP= 1 : No Comparison

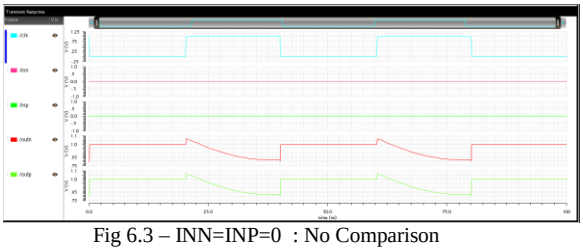

Fig 6.3 – INN=INP=0 : No Comparison

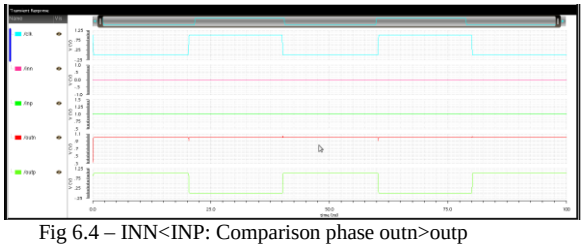

Fig 6.4 – INN<INP: Comparison phase outn>outp

F. Truth Table

CLK	INN	INP	OUTN	OUTP
0	X	X	1	1
1	0	0	0	0
1	0	1	1	0
1	1	0	0	1
1	1	1	0	0

IV ADVANTAGES

Higher input impedance is provided by did this circuit. Due to high input resistance, the power consumed is low which results in less static power consumption. There is no loss in voltage from VDD to ground which results in rail to rail output swing. Due to the tail transistor, the speed of the circuit is increased when compared to the pre amplifier circuit as fast switching of PMOS and NMOS occurs.

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V LIMITATIONS

There is only one path for the current to flow in the circuit. Due to more number of transistors present in the top half of the circuit which represents stacking and due to this high supply voltage is consumed for circuit operation.

VI CONCLUSION

The circuit is thus constructed on a 90nm technology using cadence software. The presence of single tail transistor improves the overall performance of the circuit as the switching of the PMOS and NMOS transistors occurs at a faster phase that depends on the input clock values of the tail transistor. The circuit only functions as a comparator when the input clock value is one.

VII FUTURE SCOPE

To overcome the limitations of single tail by reducing the stacking effect, delay and increasing the speed, another tail transistor may be introduced and stack transistors may be reduced by modifying the circuit.

IX REFERENCES

[1] Rameshkumar.R, Bharathiraja.S. , "A Comparative Analysis of High Speed Dynamic Comparator in 180nm and 90nm using H-spice," IJISER Vol 1 Issue 11 Dec 2014.
[2] Analysis and design of analog integrated circuit by Razavi.
[3] VLSI design by V.S Bagad.

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