Design of Compact and High Speed Baugh -Wooley Multiplier by CSA Using QCA

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Abstract: **While conventional CMOS digital circuits are limited by technology scaling researchers investigated various nano devices alternate to CMOS. In various nano devices Quantum-dot Cellular Automata (QCA) technology is a promising alternative to CMOS technology. It is attractive due to its fast speed, small area and low power consumption. This paper presents the design of compact and high speed Baugh Wooley Multiplier using Quantum Dot Cellular Automata. Multipliers are the basic building blocks of many computations in DSP processors. Earlier several adder and multiplier designs in QCA have been proposed, but limited work is done in signed multiplication. This paper utilizes the unique QCA characteristics to design a Baugh -Wooley Multiplier that is fast and efficient to implement both signed and unsigned multiplication and comparison will be done with present implemented multipliers. Simulation results were included using QCADesigner and shows that a factor of 12 smaller in terms of the area in this proposed Baugh -Wooley Multiplier design when compared with the CMOS 32nm implementation.**

Keywords: **Multiplier, Quantum-dot cellular automata, Nanotechnology, 1-bit full adder, Majority gate.**

I. INTRODUCTION

According to Moore's Law with growing number of devices on SOC as the CMOS scaling continues Short channel effects are predominant. To overcome this Research scholars concentrated on various alternative Technologies and techniques. Nanotechnology is a possible alternative to these problems and the ITRS report [1] explains several possible technology solutions. Quantum-dot cellular automata (QCA) an excellent possibility to construct digital circuits in Nanotechnology. Since QCAs were introduced in 1993 [2], several experimental devices have been developed [3], [4], [5], [6], [7]. Although they are certainly "not ready for prime time," recent papers show that QCAs may eventually achieve high density [8], fast switching speed [9], and room temperature operation [5], [10].

As an emerging alternative to CMOS technology in digital design it is necessary to explore the characteristics of QCA. Previously, several fundamental circuits designed in QCA have been proposed [11-15]. The research showed that, in the case of adder design, improved performance depends on minimizing the carry propagation delay [15]. Therefore, conventional high performance adder designs that require more wires than a slow adder design in CMOS technology could result in slower performance and difficulty in realization of QCA technology. It has been shown that due to these wire delays, most previous adder designs are limited in terms of speed [14].

A case study of a matrix multiplier is employed since it can be designed by using both systolic array and single processor architectures Multiplication involves 2 basic operations: the generation of the partial product and its accumulation. Therefore, there are possible ways to speed up the multiplication: reduces the complexity, and as a result reduces the time needed to accumulate the partial products. Both solutions can be applied simultaneously. Two's Compliment is the most popular method in representing signed integers in Digital Electronics..It is also an operation of negation(Converting positive to negative numbers or vice versa) in computers which represent negative numbers using two's compliment. Its use is so wide today because it does not require the addition and subtraction circuitry to examine the signs of the operands to determine whether to add or subtract. Two's compliment and one's compliment representations are commonly used since arithmetic units are simpler to design Baugh-Wooley Multiplier. Carry Save Adder is used in the implementation of Baugh-Wooley multiplier. Here by using one bit full adder in place of CSA(Carry Save Adder) and by using QCA(Quantum dot Cellular Automata) the Baugh-Wooley Multiplier was implemented.

QCA technology has significant advantages of fast speed, high density and low power consumption. Therefore, it is considered as attractive for the development of digital circuits. Sophisticated QCA circuits including binary arithmetic circuits memories and a simple processor have been designed and verified by simulation tools. Design methods for complex QCA circuits have also been explored to achieve more efficient designs. However, with the development of computer architecture, binary arithmetic was became the standard number system for electronic computers, and now dominates the modern computing world. While binary computer arithmetic design has been extensively investigated, limited attention has

been given for signed and unsigned multipliers. Hence, this paper explores the possibility of implementing Baugh-Wooley Multiplier in semiconductor QCA technology is investigated.

The paper is organized as follows: In Section 2, background information on QCA technology and design methods are presented. Section 3 outlines the algorithms and systolic structure of Baugh-Wooley Multiplier and with its respective QCA implementation. Section 4 explains about the design analysis with Simulation results and performance. Finally, conclusions are provided in Section5.

II **QCA basics:** QCA is based on electrons confining in dots and each cell has four quantum Dots [2]. The four dots are located in the corners of squares structure as shown in fig 1. The electrons tunnel through neighboring dots to the proper location during the clock transition.

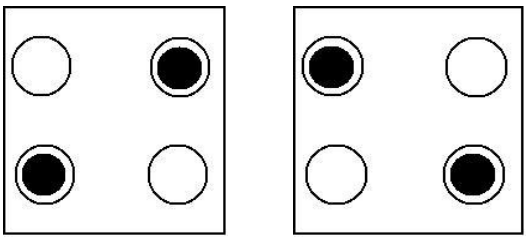


Fig1 Schematic of a QCA cell: (a): Logic '1'(b): Logic '0'.

Several approaches have been suggested for computation with an array of QCA cells. One approach is based on transferring the array to an excited state from a ground state by merely applying input data (without explicit clocking). The array is expected to settle to a new ground state. However, sometimes the transition may result in a metastable intermediate state. In QCA, the logic states are not stored as voltage levels. Instead, the location of individual electrons determines the binary state.

QCA Clock Zones: To facilitate transfer to a new ground state, another approach based on clocking has been suggested. Clocking (by application of an appropriate voltage to a cell) leads to adjustment of tunneling barriers between quantum dots [4]. Clocking is performed in one of two ways: zone clocking and continuous clocking. In each zone clocking, each QCA cell is clocked using a four-phase clocking scheme as shown in Fig 2(a). The four phases correspond to *switch*, *hold*, *release* and *relax*. In the switch phase, cells begin unpolarized and with low potential barriers but the barriers are raised during this phase. In the hold phase, the barriers are held high while in the release phase, the barriers are lowered. In the last phase, namely relax, the barriers remain lowered and keep the cells in an unpolarized state. An alternative to zone clocking, called continuous clocking, involves generation of a potential field by a system of submerged electrodes

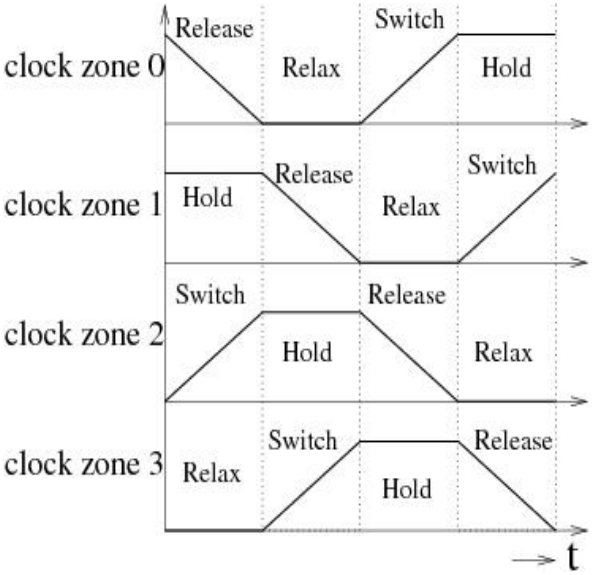


Fig 2(a): QCA clock zones

A (logic) wire is nothing but a series of QCA cells. Two types of crossovers are used to build various circuits they are 1). Coplanar crossover, 2).Multilayer crossover. Based on comparison Multilayer crossovers [9] are used to construct all designs in this paper.

QCA WIRE:

In a QCA wire, the binary signal propagates from input to output because of the Coulombic interactions between the cells[3]. This is a result of the system attempting to settle to a ground state. Any cells along the wire that are anti-polarized to the input would be at a higher energy level, and would soon settle to the correct ground state. The propagation in a 90-degree QCA wire is shown in Fig. 2. Other than the 90-degree QCA wire, a 45-dgree QCA wire can also be used. In this case, the propagation of the binary signal alternates between the two polarizations. Further, there exists a so-called non-linear QCA wire, in which cells with 90-degree orientation can be placed next to one another, but off center.

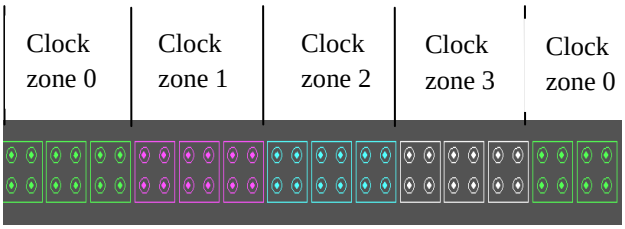


Fig 2(b): QCA wire

Majority Gate and Not gate:

Fig 2(c), (d) shows the majority gate and its layout, fig 2 (e), (f) shows NOT gate and its layout. By using these two gates various Boolean expression are realized. The majority gate performs a three-input logic function [12-15]

where M(A,B,C) = A.B+A.C+B.C.

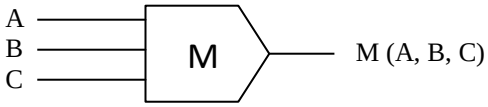


Fig 2(c) Majority gate.

By fixing the polarization of one input as logic "1" or "0", we can obtain an OR gate and an AND gate respectively. More complex logic circuits can then be constructed from OR and AND gates.

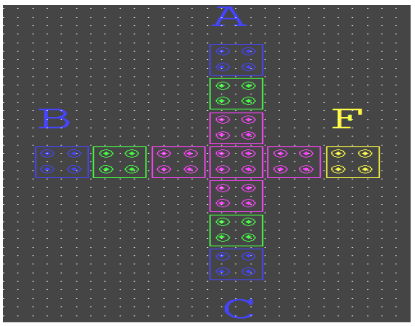


Fig 2(d) Layout of Majority gate.

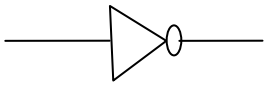


Fig 2(e) Inverter

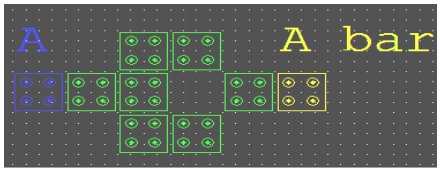


Fig 2(f) Layout of Inverter

III.BAUGH-WOOLEY MULTIPLER:

Baugh-Wooley Multiplier is especially used for only Two's complement signed and unsigned multiplication only. Baugh Wooley Two's complement Signed multipliers are the best known algorithm for signed multiplication because it maximizes the regularity of the multiplier and allow all the partial products to have positive sign bits. Baugh Wooley technique was developed to design direct multipliers for Two's compliment numbers .When multiplying two's complement numbers directly, each of the partial products to be added is a signed numbers. Thus each partial product has to be sign extended to the width of the final product in order to form a correct sum by the Carry Save Adder (CSA) tree[18].

Baugh-Wooley Multiplier is used for both unsigned and signed number multiplication. Signed Number operands which are represented in 2's complemented form. Partial Products are adjusted such that negative sign move to last step, which in turn maximize the regularity of the multiplication array. Baugh-Wooley Multiplier operates on signed operands with 2's complement representation to make sure that the signs of all partial products are positive. Here are using fewer steps and also lesser adders. Here a0, a1, a2, a3& b0, b1, b2, b3 are the inputs, the outputs are p0, p1... p7. As this design was done using pipelining resister in this architecture[18] ,so it will take less time to multiply large number of 2's complement but less than 32 bit .Above 32 bit Modified Baugh-Wooley Multiplier is used.

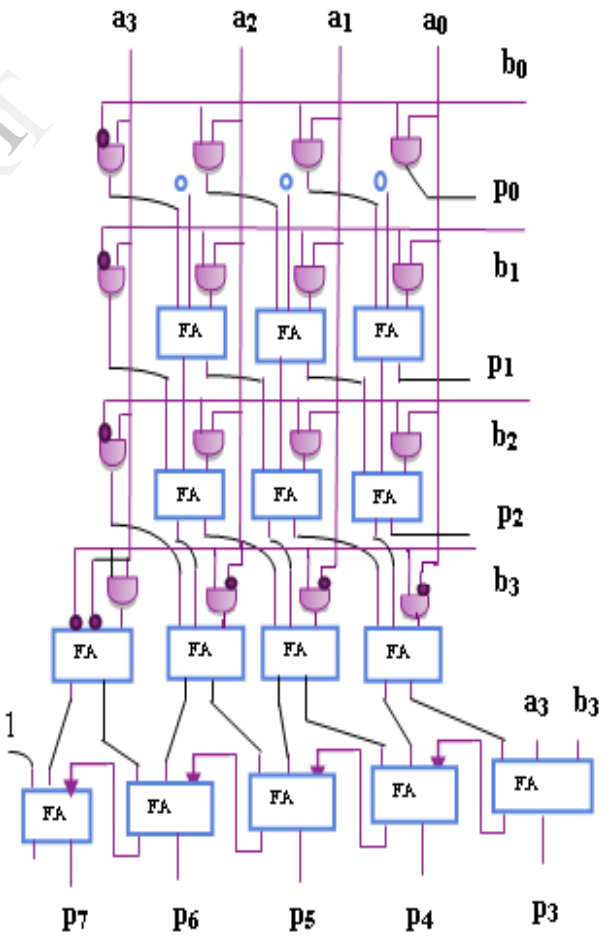
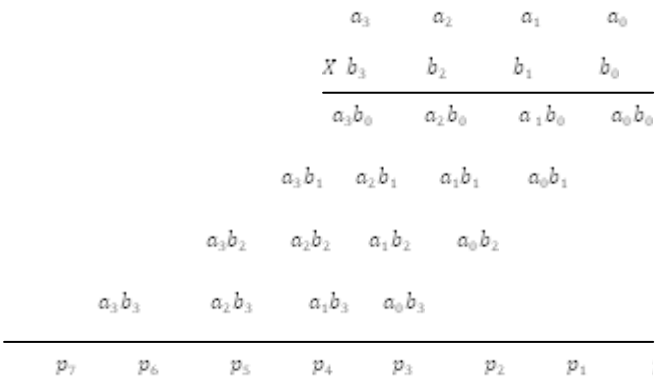


Fig 3(a). Block diagram of Baugh Wooley Multiplier

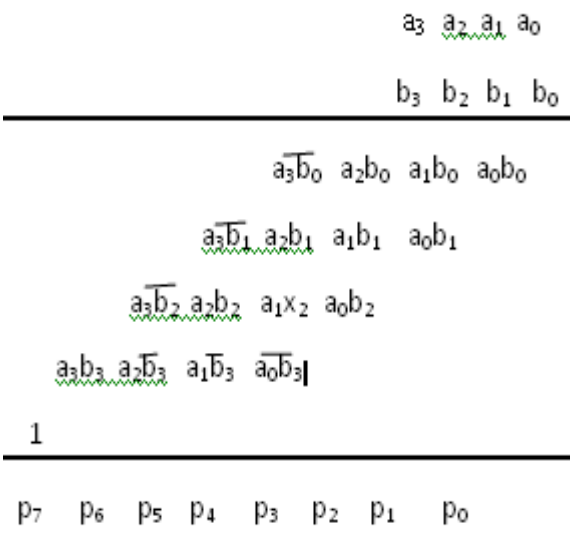
QCA IMPLEMENTATION:

For easy comparisons, 4 bit multiplier examples are shown. Fig. 3(b) shows the bit product matrix for 4 bit multiplication

Fig 3(b): Bit product matrix for 4 bit multiplication



Here to implement the Baugh Wooley Multiplier using QCA we are using one bit full adder has been taken by comparing [9 -14]. Using that adder structure the four bit Baugh - Wooley Multiplier according to Fig. 3(a)are implemented as shown in the Fig. 4 & the algorithm is shown below .



IV Figure 4 shows the layout of Baugh Wooley Multiplier using QCA. Multipliers for larger word sizes can be implemented easily by adding additional bit slices.

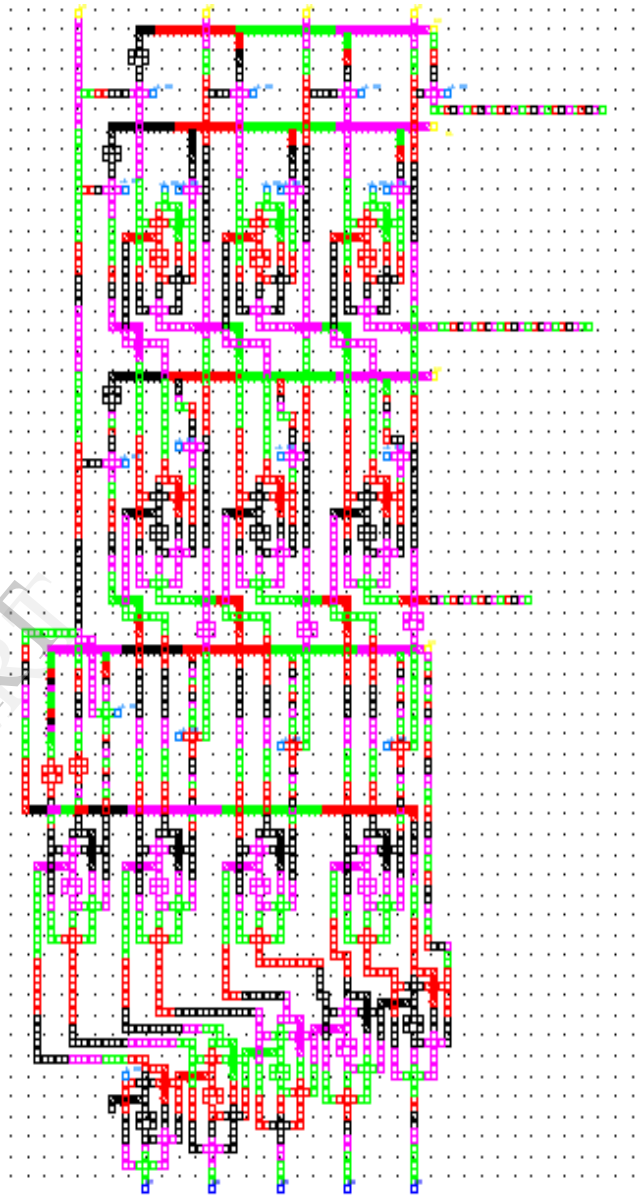
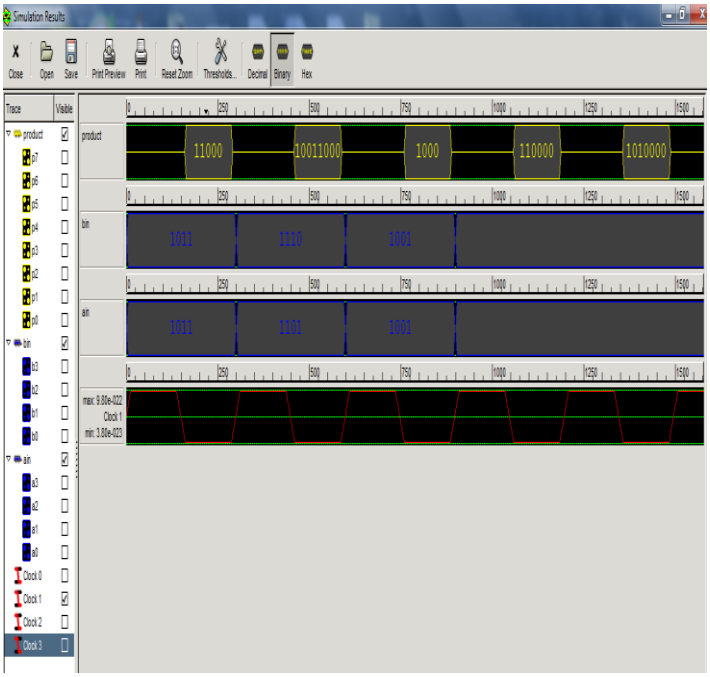


Fig 4: Layout of Baugh Wooley Multiplier

Simulation results

With QCA Designer tool the circuit functionality is verified by using Coherence vector engine.



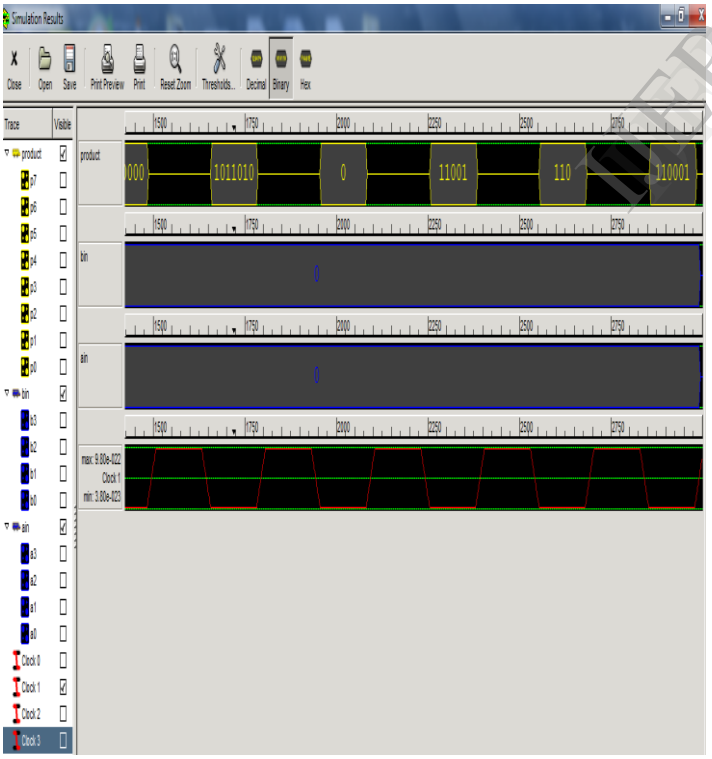


Fig4 (a): Simulation result of Baugh Wooley Multiplier

Performance Comparison:

Multiplier using QCA	**Complexity (cells)**	**Area (μm^2)**	**Delay (clocks)**
Systolic multiplier[16]	15,579	38.96	32
4X4 Wallace Multiplier [19]	3295	7.39	10
4X4 Dadda Multiplier [19]	3384	7.51	12
Baugh -wooley multiplier	3210	4.85	5.5

Table1.Various Multipliers performance

The above table shows the brief comparison between the various multipliers. In the CMOS architecture, the single processor design takes more clock cycles to perform a larger matrix due to more additions required in the accumulators, while due to the inherent parallelism, in the Baugh Wooley Multiplier design, the increase in the number of clock cycles are less. However, there is increased speed which is significantly greater than in the CMOS design. However, in the QCA design, internal wire delays cost more clock cycles. In the QCA Baugh- Wooley Multiplier design, the clock cycle count increases as in the CMOS design, because there is only one clock cycle delay between each PE in both technologies. Therefore, the clock cycle ratio increases much faster in the QCA design than in the CMOS design. In other words, QCA technology benefits more from employing Baugh Wooley Multiplier architectures than CMOS technology. QCA technology is a terahertz technology and although QCA designs require more clock cycles than the equivalent CMOS architectures, they run faster [16].

V.CONCLUSIONS:

In terms of area, QCA has huge advantages over CMOS technology. For instance, the silicon cost of a 4 bit 4x4 Baugh Wooley Multiplier implementation, designed using Synopsys Design Compiler with 182nm CMOS technology, requires approximately 552µm2. CMOS. In comparison, in QCA technology the area is only 4.85µm2, a factor of 114 smaller. By applying the Baugh Wooley Multiplier structure to this QCA design, significant benefits are achieved and great improvements are found over CMOS-based designs. In addition, QCA has significant area advantages over CMOS. In QCA matrix

multiplier design case study, a 22 magnitude area reduction can be achieved when compared with corresponding CMOS 32 nm implementation. In this paper the Baugh Wooley Multiplier using QCA where the delay and area were decreased compare to the MOS based Baugh Wooley Multiplier. Thus QCA is efficient way to design Baugh Wooley Multiplier within less delay and power consumption is by using pipelining and parallelism. These characteristics can minimize the effect of the inherent wire delay of QCA designs.

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