Design of d-q Domain Control Strategy for Static Synchronous Series Compensator

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Abstract

To improve the energy quality in distribution systems, many different solutions are implemented for example i) Active Power Filters ii) FACTS Controllers. This paper describes an active approach to series line compensation in which a synchronous voltage source, implemented by a gate turn-off thyristor (GTO) based voltage source inverter is used to provide controllable series compensation. This compensator, called Static Synchronous Series Compensator (SSSC). SSSC is controlled in such a way as to inject capacitive or inductive voltage drop in series with the line with the effective value of reactance settable and controllable independently of magnitude of line current. The special control scheme is designed for the power flow control of a transmission system with two identical parallel lines while the general control scheme can be used to solve the power flow control problem. With a balanced, distortion free system the best way to control a three phase system is to jump over the Synchronously Revolving Reference Frame or so called d-q plane. By using this d-q domain control strategy the injected voltages can be controlled for different switching times.

I. Introduction

The SSSC is generally connected in series with the transmission line with the arrangement as shown in figure below. The SSSC comprises a coupling transformer, a magnetic interface, voltage source converters (VSC) and a DC capacitor. The coupling transformer is connected in series with the transmission line and it injects the quadrature voltage into the transmission line. The magnetic interface is used to provide multi-pulse voltage configuration to eliminate low order harmonics. The injected voltage of the coupling transformer V_i is perpendicular to the line current I.

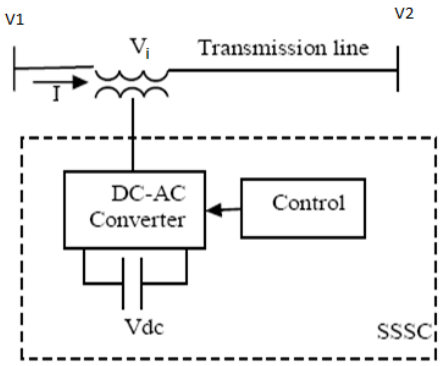

Fig 1: Simplified Diagram of SSSC

The SSSC is in principle a synchronous voltage source, which is typically connected in series with a transmission circuit to provide line compensation. This controllability is achieved by using a controllable interface between the DC voltage source (typically a capacitor) and the ac system. The series capacitive compensation basically to decrease the overall effective series transmission impedance from the sending end to the receiving end. The relationship characterizes the power transmission over a single line is:

$$P = \frac{V_1 V_2}{X} \sin \delta$$

P - Real power transmission over a single line

V - The sending end and receiving end voltage (assuming $V_1 = V_2 = V$)

X - The line impedance

δ - The power angle

SSSC is a power converter connected in series with the transmission line and it injects a voltage in quadrature with the line current to emulate a series capacitive or inductive reactance into the transmission line. A SSSC equipped with energy storage system and/or absorbing is also able to exchange real power with power system.

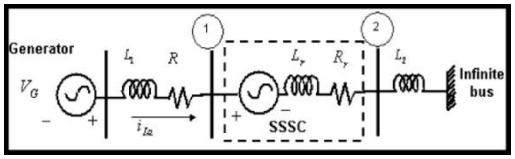

Fig 2: Line Diagram of SSSC

Reactive power exchange is controlled by the magnitude of the injected voltage to the transmission line, and angle control is used to regulate the active power exchange. The inductive or capacitive mode of operation is set by the injected voltage phase angle with respect to the transmission line current. When injected voltage is leading the line current, reactive power is absorbed and SSSC operates in inductive mode. In capacitive mode injected voltage is lagging the line current and injects reactive power to the transmission line.

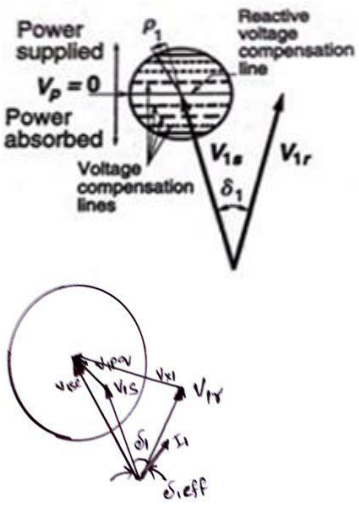

Fig 3: Variation of receiving end real and reactive power as a function of injected voltage.

It is also possible to control the SSSC such that it always injects a present value of voltage in quadrature with current, but independent of current. In both modes of control, it is possible to put an outer control loop which can be designed to maintain the real power flow in the line at a present value against bus voltage variations or bus angle variations. Similarly it is also possible to employ an outer loop to maintain the bus voltage to the right of SSSC constant. Also, by suitably modulating the reference setting (whatever that be) according to some relevant information it is possible to make use of SSSC to introduce damping in the system to improve dynamic stability and sub-synchronous behavior. Finally it is also possible to modulate the reference settings in such a way that the transient stability margins can be improved when the system undergoes large disturbances.

There has to be a DC source for a converter to produce ac- this DC source in a SSSC is a large DC capacitor. The capacitor maintains a large enough voltage for the inverter to generate a three phase system of voltages as per the compensation requirements. The inverter, as stated already, injects only quadrature voltage into the line. This means that the real power flow into or out of inverter is zero. Well, not exactly. When the entire line current flows through the inter phase transformer and inverter passive and active components there will be losses everywhere. If inverter has no real power coming in from line, then the DC side capacitor has to deliver these losses and soon it will discharge down to a level at which the SSSC has to trip. Hence there has to be a control loop on the DC side voltage, maintaining it constant by drawing or delivering active power suitably. Of course, since these active powers essentially take care of losses in the system it can be expected to be small. Thus the voltage injected by SSSC has to have a small component which is in phase with the current line.

The application is a transmission level application (otherwise, if it is distribution level, it will be called active series filter; at transmission levels only fundamental reactive compensation is usually attempted) and assumption of balanced system voltages and negligible harmonics will be permitted. And it is unlikely that SSSC will be expected to work when the system voltage (one or more phasors) go down to such low levels where PLLs will lose

lock. In fact under severe fault conditions SSSCs are bypassed by fast acting static bypass switches. Thus we have balanced, relatively distortion free voltage of sufficient amplitude at the bus to the left of SSSC installation and it is possible to lock a PLL system with sufficient ease at this point. Moreover at a balanced, distortion free system the best way to control a three phase system is to jump over to 'Synchronously Resolving Reference Frame' or the so called d-q plane. This lectures deals with such a control strategy.

The voltage level is high and even with interface transformer, the voltage levels and current levels will usually be beyond the capability of IGBTs (though they are catching up rapidly) and GTOs and other similar devices rule and when GTOs rule, switching frequency can only be low- and that brings in multi-pulse or multi-level or cascade inverters. Typically multi-pulse inverter is used- in one installation a 48 pulse three phase inverter comparing 8 three phase inverters of 6 pulse two-level types. The construction of 48 pulse waveform was done in transformer magnetic in this case.

II. Control strategy

The main function of the SSSC is to control the reactive power flow. This can be accomplished either by direct control of the line current (power) or alternatively by indirect control of the compensating impedance, X_c or the compensating voltage, V_i. The direct power flow control has the advantage of maintaining the transmitted power in a closed loop manner by the defined reference. However under some network contingency, the maintenance of the constant power flow may not be either possible or even desirable. Therefore in some applications the impedance (or voltage) control that maintains the impedance characteristic of the line may be preferred from the operating standpoint. The degree of series impedance compensation, S, is usually expressed as the ratio of the series injected reactance X_c, to the line reactants, X, S = Xs/X Therefore for a capacitive series compensation, the line series reactants is Xline = X – X_c, where Xs =S X. Similarly for an inductive series compensation tile line series reactance is Xline = X + X where Xs = SX. The basic function of d-q control strategy is to keep the SSSC voltage V_i in quadrature with the line current I and control the magnitude of V_i to meet the compensation requirement, which is the degree of series compensation.

The d-q domain control strategy for SSSC is explained with respect to the following system

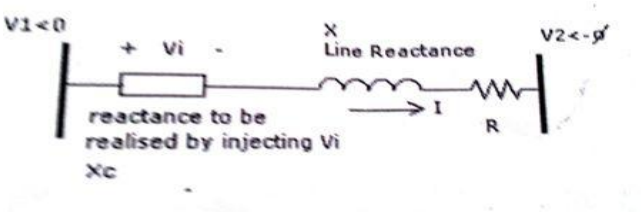

Fig 4: Two bus system

The d-q domain equations of the system are given below

$$V_{1d} - V_{2d} = Ri_d + X_c I_q - Xi_q$$

$$V_{1q} - V_{2q} = Ri_q - X_c I_d - Xi_d$$

Now, the line currents are sensed and transformed into d-q plane by using unit sine and cosine template waveforms. These template waveforms are generated by a digital PLL system locking on to the system voltage at the left side bus. The purpose of control is to maintain X_c ohms of compensating reactance in the line. For this purpose the required d and q component voltages can be calculated i.e., $_{Xc} I_q$ and $- X_c I_d$ can be calculated from the set value for X_c and calculated values of I_d and I_q. These values are reconverted into three phase quantities and given as reference single to PWM gating system of inverter .However, this is not enough because a small in phase voltage injection will be needed to meet the inverter losses. This is done with the help of PI controller on DC side voltage. When the DC side voltage goes down the PI controller output increases and this error output is used to inject KI_d volts in q-axis where k is error output. Essentially we are putting a resistance (fictitious) in series with X_c of value k. The power which goes into that resistance is the power that meets the losses in SSSC.

The values for V1 and V2 were 320 volts peak phase-neutral. The line reactance was 3 ohms and the line resistance was set as zero for simulation runs.

The d-q method will calculate the current components instantaneously and there is no need for a filter in d-q domain on sensed currents if currents are balanced and distortion free. However in presence of such corruptions d-q components will have high frequency contents like 100Hz and above and these should not be sent into the inverter reference . Hence 25 Hz low pass filter is used in the d-q lines in current sensing part. After filter placement the equations are modified as given below

$$V_{1d} - V_{2d} = Ri_d + X_c I_q + V_c I_d - Xi_q$$

$$V_{1q} - V_{2q} = Ri_q - X_c I_d + V_c I_q - Xi_d$$

Where V_C is the output of PI controller in the DC side voltage controller loop . The AC side of inverter is modeled as an ideal voltage source which generates the commanded voltages without any distortion, delay and with zero output impedance DC side is modeled by using power balanced to calculate the capacitor voltage. The PLL system is not modeled, in fact exact phase lock is not so important .The PLL output has to be in synchronism with the system voltage, but it need not have same phase that of mains.

Typical simulation results for sudden switching on of X_C value , sudden change of phase angle between the buses are given .The results given in figure reveals the DC voltage regulation dynamics .This dynamics comes into the picture whenever the phase relation between the injected voltage and line current undergo sudden changes as in case when the angle of one or both the bus voltages change instantaneously(due to the fault in the system elsewhere etc.,).This dynamics is dependent on the loading level in the line at the instant of system disturbance. This is so since the loop gain DC voltage control loop is proportional to the line currents.

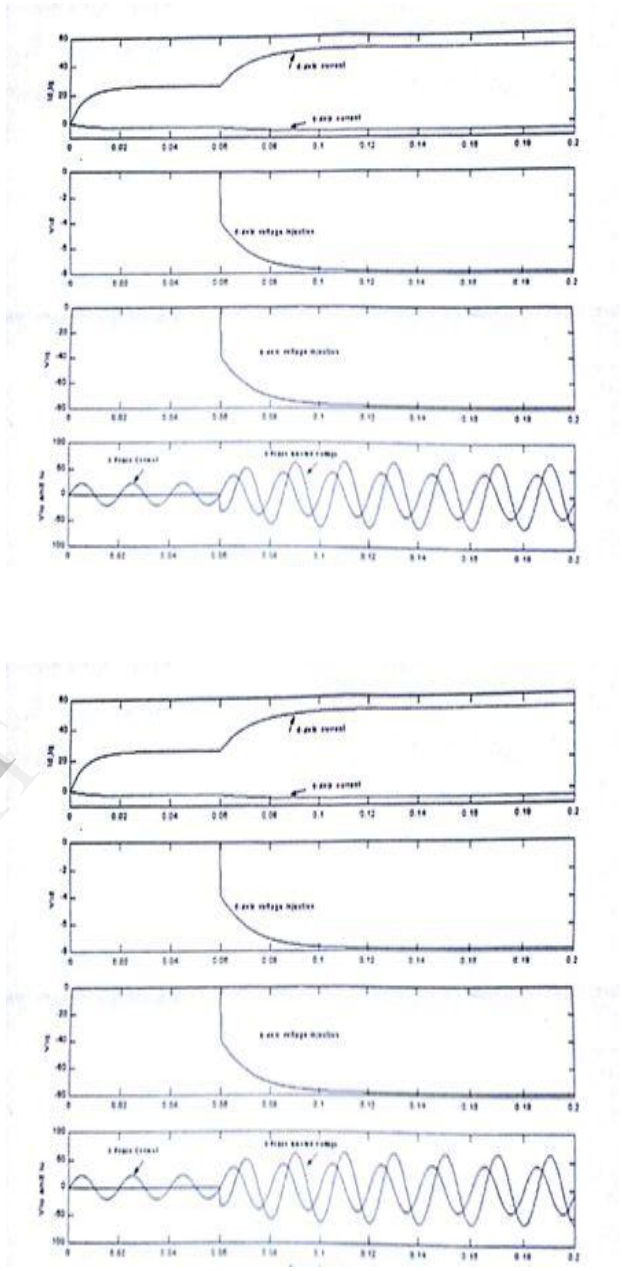

Fig 5: Simulation results for two switching times

III. Conclusion

The Static Synchronous Series Compensator offers an alternative to conventional series capacitive line compensation. Whereas the series capacitor is the impedance that produces the

required compensating voltage as the line current flows through it, SSSC is a solid-state voltage source that internally generates the desired compensating voltage independent of the line current. The voltage source nature of the SSSC provides the basis for its superior operating and performance characteristics not achieved by series capacitor type compensators. d-q domain control strategy improves power transfer capability compared to conventional control strategy. This control strategy can be widely employed for more number of SSSCs operating under IPFC mode. With unbalanced, distortion system the best way to control a 3-phase system is d-q domain control strategy.

IV. References

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BIOGRAPHIES

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