Design of Double Phase Clock Multiband Flexible Divider

G. Priya, Asst.Professor, M. Dinesh, Asst.Professor

N.S.N Engineering College,Cheran Engineering College, Karur.

Abstract--- Clock consumes nearly 60% of the total power in an IC since it is the only signal which runs to every part of the design with highest toggling rate so more care should be taken for developing a multiband low power clock. Wireless LAN (WLAN) in the multigigahertz bands, such as HiperLAN II and IEEE 802.11a/b/g, are recognized as leading standards for high-rate data transmissions and standards like IEEE 802.15.4 are recognized for low-rate data transmissions. The demand for lower cost, lower power and multiband RF circuits increased in conjunction with need of higher level of integration. In this Project IEEE 802.15.4 and 802.11 a/b/g WLAN frequency synthesizers is proposed based on pulse-swallow topology and it is modeled using Verilog HDL, simulated using Modelsim and Synthesized using Tanner tool. The multiband divider consists of a proposed wideband multimodulus 32/33/47/48 prescaler and an improved bit-cell for swallow (S) counter and can divide the frequencies in the three bands of 2.4–2.484 GHz, 5.15–5.35 GHz, and 5.725–5.825 GHz with a resolution selectable from 1 to 25 MHz**This design aim for developing a low power double clock for multiband frequency. The design is modeled using Verilog, simulated using Modelsim and synthesized using Tanner.**

Keywords: Highest toggling, Multiband frequency, Frequency synthesizer.

.

1. INTRODUCTION

The frequency divider is an important building block in today's RFIC and microwave circuits because it is an integral part of the phase-locked loop (PLL) circuit. In a typical PLL loop, the output of the voltage controlled oscillator(VCO) is divided down by the frequency divider to a frequency the temperature-compensated crystal oscillator (TCXO) operates (typically from 10 MHz to 30 MHz).The divided signal and TCXO are fed into the phase detector for comparison. The output phase difference is used to adjust the VCO output frequency. The frequency divider is also widely used to generate a precision I/Q signal if the input signal has a 50% duty cycle, for the modern in-phase and quadrature (I/Q) modulator or demodulator. For the signal with duty cycle other than 50%, an additional divideby-2 can be used to generate the 50% duty cycle. Compared with the traditional resistor and capacitor (RC) quadrature generation, the frequency divider approach is easier to implement, is lower power and offers smaller phase imbalance.

2. OBJECTIVE

With the smaller geometries in Deep Sub-Micron (DSM) technology, the number of gates that arerequired to be integrated on a single chip and total power consumption are increasing rapidly. Over the last two decades, low-power circuit design has become an important concern in VLSI design, a low-power single-phase clock multibandflexible divider for Bluetooth, Zigbee, and IEEE 802.15.4 and 802.11a/b/g WLAN frequency synthesizers is proposed based on pulse-swallowtopology. The multiband divider consists of a proposed wideband multimodulus32/33/47/48 prescaler and an improved bit-cell for swallow (S) counter andcan divide the frequencies in the three bands of 2.4–2.484 GHz, 5.15–5.35GHz, and 5.725–5.825 GHz with a resolution selectable from 1 to 25 MHz To further improve the performanceof the circuits and to integrate more functions on a single chip, the feature size have to shrink. Asa result, the power consumption per unit area grows.

3. DESIGN PARAMETERS

The most important parameters of high-speed digital circuits are the operating frequency and power consumption. The operating frequency is decided by the propagation delay and it is calculated as

$$f_{max} = \frac{1}{2 \times \max\left(t_{pLH}, t_{pHL}\right)}$$

Where t_{pLH} and t_{pHL} are the propagation delays of the low to high and high to low transitions. Thepower consumption of theCMOSdigital circuit is mainly decided by the switching power, which is linearly proportional to the operating frequency.The switching power is given by

$$P_{switching} = \sum_{i=1}^{n} f_{clk} C_{Li} V_{dd}^2$$

Where n is the number of switching nodes, f_{clk} is the clock frequency, C_{Li} is the load capacitance at the output node of the i th stage, and V_{dd}^2 is the supply voltage. Normally, the short-circuit power occurs in dynamic circuits when there exists direct paths from the supply to ground which is given by

$$P_{SC} = I_{SC} \times V_{dd}^2$$

Where I_{SC} is the short-circuit current. The analysis shows thatthe short-circuit power is much higher in E-TSPC logic circuits than in TSPC logic circuits. However, TSPC logic circuits exhibit higher switching power compared to that of E-TSPC logic circuits due to high load capacitance. For the E-TSPC logic circuit, the short-circuit power is the major problem. The E-TSPC circuit has the merit of higher operatingfrequency than that of the TSPC circuit due to the reduction in load capacitance, but it consumes significantly more power than the TSPC circuit does for a given transistor size.

4. BLOCK DIAGRAM

The frequency synthesizer reported in a 13.5-mW 5 GHz frequency synthesizer with dynamic-logic frequency divider, uses an E-TSPC prescaler as the first-stage divider, but the divider consumes around 6.25mW.Most IEEE 802.11a/b/g frequency synthesizers employ SCL dividers as their first stage while dynamic latches are not yet adopted for multiband synthesizers. In this paper, a dynamic logic multiband flexibleinteger N divider based on pulse-swallow topology is proposed which uses a low-power wideband 2/3 prescaler A 1.8-V 6.5-GHz low power wide band single-phase clock CMOS 2/3 prescalerand a wideband multimodulus 32/33/47/48 prescaler .The divider also usesan improved low-power loadable bit-cell for the Swallow –S counter.

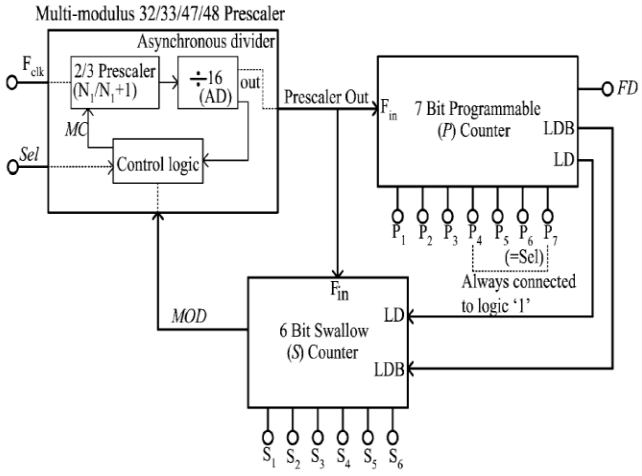

Fig.1

The E-TSPC 2/3 prescaler consumes large short-circuit power and has a higher frequency of operation than that of TSPC 2/3 prescaler. The wideband double-phase clock 2/3 prescaler used in this design consists of two D-flip-flops andtwo NOR gates embedded in the flip-flops as in Fig 2.

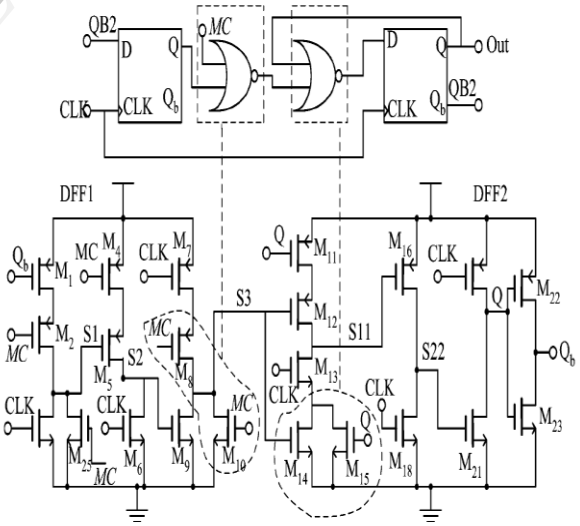

Fig.2

The first NOR gate is embedded in the last stage of DFF1, and the second NOR gate is embedded in the first stage of DFF2.

I.MULTIMODULUS 32/33/47/48 PRESCALER

The proposed wideband multimodulus prescaler which can divide the input frequency by 32, 33, 47, and 48 is shown in Fig. 1. It is similar to the 32/33 prescaler used

but with an additional inverter and a multiplexer. The proposed prescaler performs additional divisions (divide-by-47 and divide-by-48) without any extra flip-flop, thus saving a considerable amount of power and also reducing the complexity of multiband divider The multimodulus prescaler consists of the wideband 2/3 $\frac{N_1}{N_1+1}$ prescaler four asynchronous TSPC divide-by-2 circuits ((AD)=16) and combinational logic circuits to achieve multiple division ratios as shown in Fig.2. Beside the usual MOD signal for controlling $N/N+1$ divisions, the additional control signal Sel is used to switch the prescaler between 32/33 and 47/48 modes.

A. Case 1: $Sel = 0$

When $Sel = '0'$ the output from the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multimodulus prescaler operates as the normal 32/33 prescaler, where the division ratio is controlled by the logic signal MOD . If $MC = 1$, the 2/3 prescaler operates inthe divide-by-2 mode and when $MC = 0$, the 2/3 prescaler operates in the divide-by-3 mode.

B. Case 2: $Sel = 1$

When $Sel = 1$ the inverted output of the NAND2 gate is directly transfered to the input of 2/3 prescaler and the multimodulus prescaler operates as a 47/48 prescaler, where the division ratio is controlled by the logic signal MOD . If $MC = 1$, the 2/3 prescaler operates in divide-by-3 mode and when $MC = 0$ the 2/3 prescaler operates in divide-by-2 mode.

solution to the low power PLL synthesizers for Bluetooth, Zigbee, IEEE 802.15.4, and IEEE 802.11a/b/g WLAN applications with variable channel spacing.

SIMULATION RESULT

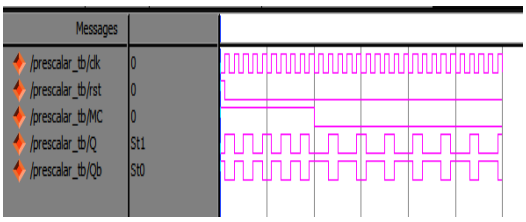

Fig.3.schematic of prescaler

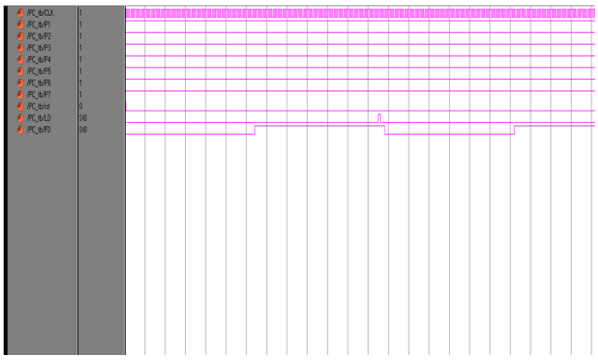

Fig.4.Schematic of Programmable counter

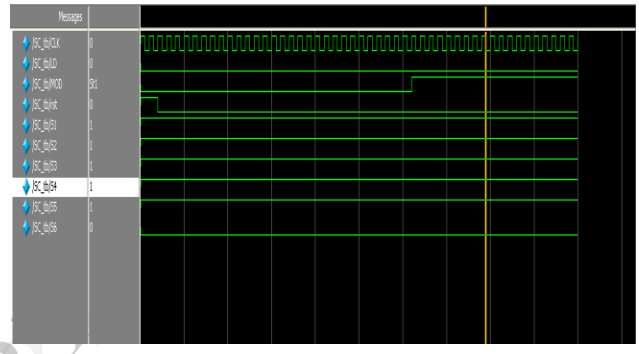

Fig.5.Scheamtic of Swallow counter

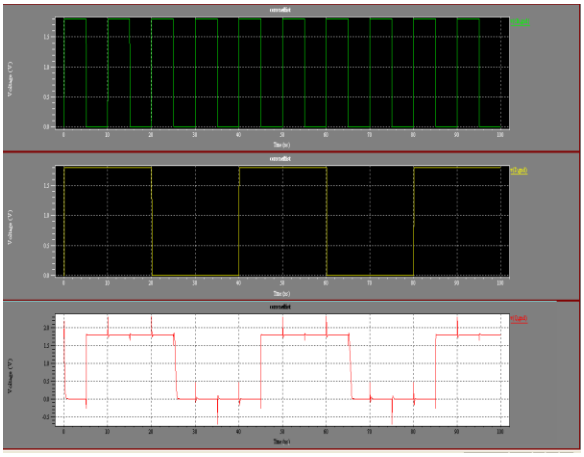

Fig.5 Propagation delay schematic in Tanner tool

Table.1

The following table represents the total time taken for simulation.

Data Path: rst to Fout

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
IBUF:I->O	19	1.218	1.164	rst_IBUF (rst_IBUF)
LUT3:I1->O	2	0.704	0.482	t4/d1/rbar_and00001
LUT3:I2->O	3	0.704	0.566	t4/d1/r_and00001
LUT3:I2->O	1	0.704	0.499	w4_and000028
LUT2:I1->O	1	0.704	0.595	w4_and000034 (w5)
LUT4:I0->O	1	0.704	0.424	m1/d2/rbar_and0000_SW0
LUT4:I3->O	2	0.704	0.622	m1/d2/rbar_and0000
LUT4:I0->O	3	0.704	0.706	m1/d2/s_and00001
LUT4:I0->O	5	0.704	0.712	m1/d2/dout1 (Q0)
LUT3:I1->O	3	0.704	0.566	t1/d1/r_and00001
LUT3:I2->O	2	0.704	0.622	t1/d1/rbar_and00001
LUT4:I0->O	3	0.704	0.706	t1/d1/s_and00001
LUT4:I0->O	5	0.704	0.712	t1/d1/dout1 (Q1)
LUT3:I1->O	3	0.704	0.566	t2/d1/r_and00001
LUT3:I2->O	2	0.704	0.622	t2/d1/rbar_and00001
LUT4:I0->O	3	0.704	0.706	t2/d1/s_and00001
LUT4:D->O	5	0.704	0.712	t2/d1/dout1 (Q2)
LUT3:I1->O	3	0.704	0.566	t3/d1/r_and00001
LUT3:I2->O	2	0.704	0.622	t3/d1/rbar_and00001
LUT4:I0->O	3	0.704	0.706	t3/d1/s_and00001
LUT4:D->O	5	0.704	0.668	t3/d1/dout1 (Q3)
LUT4:I2->O	3	0.704	0.706	t4/d1/s_and00001
LUT4:I0->O	4	0.704	0.587	t4/d1/dout1 (Fout_OBUF)
OBUF:I->O		3.272		Fout_OBUF (Fout)

Total 34.815ns (19.978ns logic, 14.837ns route) (57.4% logic, 42.6% route)

5. CONCLUSION

A dynamic logic multiband flexible integer- N divider is designed which uses the wideband 2/3 prescaler, multimodulus 32/33/47/48 prescaler. Since the multimodulus 32/33/47/48 prescaler has maximum operating frequency of6.2 GHz, the values of S and P counters can actually be programmed to divide over the whole range of frequencies from 1 to 6.2 GHz with finest resolution of 1 MHz and variable channel spacing. However, since interest lies in the 2.4- and 5–5.825-GHz bands of operation, the P and S counters are programmed accordingly. The proposed multiband flexible divider also uses an improved loadable bit-cell for Swallow S -counter and consumes a power of 0.96 and 2.2 mW in 2.4- and 5-GHz bands, respectively, and provides a solution to the low power PLL synthesizers.double edge multiband flexible divider is designed which consumed power of0.25 mw in 5-5.825GHz band of operation.

REFERENCES

1.H. R. Rategh *et al.*, "A CMOS frequency synthesizer with an injectedlocked frequency divider for 5-GHz wirless LAN receiver," *IEEE J. Solid-State Circuits*, vol. 35, no. 5, pp. 780–787.

2. P. Y. Deng *et al.*, "A 5 GHz frequency synthesizer with an injectionlocked frequency divider and differential switched capacitors," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 2, pp. 320–326.

3.L. Lai Kan Leung *et al.*, "A 1-V 9.7-mW CMOS frequency synthesizer for IEEE 802.11a transceivers," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 1, pp. 39–48.

4. M. Alioto and G. Palumbo, *Model and Design of Bipolar and MOS Current-Mode Logic Digital Circuits*. New York.

5.Y. Ji-ren *et al.*, "Atrue single-phase-clock dynamicCMOScircuit technique," *IEEE J. Solid-State Circuits*, vol. 24, no. 2, pp. 62–70.

6. S. Pellerano *et al.*, "A 13.5-mW 5 GHz frequency synthesizer with dynamic-logic frequency divider," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 378–383.

7.V. K. Manthena *et al.*, "A low power fully programmable 1 MHz resolution 2.4 GHz CMOS PLL frequency synthesizer," in *Proc. IEEE Biomed. Circuits Syst. Conf.*, pp. 187–190.

8. S. Shin *et al.*, "4.2 mW frequency synthesizer for 2.4 GHz ZigBee applicationwith fast settling time performance," in *IEEE MTT-S Int. Microw. Symp. Dig.*

9.S. Vikas *et al.*, "1 V 7-mW dual-band fast-locked frequency synthesizer,"in *Proc. 15th ACM Symp. VLSI*, pp. 431–435.

10.V. K. Manthena *et al.*, "A 1.8-V 6.5-GHz low power wide band singlephase clock CMOS 2/3 prescaler," in *IEEE 53rd Midwest Symp. Circuits Syst.*, pp. 149–152.

11.J. M. Rabaey *et al.*, "Digital integrated circuits, a design perspective,"in *Ser. Electron and VLSI*, 2nd ed. Upper Saddle River, NJ.