Design of Double Tail Comparator using FinFETIn 32nm Technology

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***Abstract*—In the recent years, there is an increasing demand forhigh-speed integrated circuits at low powerconsumption. The requirement for drasticlow-power, area efficient and high speed analog-to-digital converters is forcingtoward the use of dynamic regenerative comparators to maximize speed and power efficiency.A novel double tail comparator using FinFET is designed, which consumes very less power and can operate at high speeds when compared with the existing double-tail comparators proposed and simulated. The designed double tail comparator is simulated using LTPICE tool with 32nm technology. From the simulation results, it is observed that in the proposed double tail comparator both the power consumption and delay time are significantly reduced**.

Keywords*—Analog-to-digital converter; double-tail comparator; FinFET; LTSPICE; MOSFET

I. INTRODUCTION

Comparator is one of the most beneficial analog circuits required in many analog integrated circuits and also in digital design. It is a circuit that compares one analog signal with another analog signal or a reference voltage and gives a binary signal based on the comparison and works on two modes: reset and comparison phase. Comparator utilizes back to back cross coupled inverters to convert the voltage into digital output in a short period of time. The performance of thecomparator plays an important role in realization of high integration, low power, low cost and good design.

Comparators are most frequently known as 1-bit analog to digital converter and for that reason they are mostly used in large abundance in A/D converter. Due to high speed, low power consumption, high input impedance and full-output swing dynamic latched comparators are very interesting. They utilizes positive feedback mechanism with one pair of back-to-back cross coupled inverters (latch) in order to convert a small input-voltage difference to a full scale digital level in a short period of time. Very high speed comparators in excessive deep submicrometer CMOS technologies are hard to work at lower supply voltages [2].

The designing of high-speed comparators is more challenging when the supply voltage is considered small. Many techniques were developed to handle higher supply voltages, such as supply boosting methods [3], [4] techniques employing body-driven transistors [5], [6], current-mode design [7] and those using dual-oxide processes. Additional nMOS switches are added to circuit to overcome the static power consumption [1]. Instead of technological modifications, developing new circuit structures is preferred. The reason for this is toprevent stacking of too many transistors. Additional circuitry [8]-[9] can also be used to the conventional dynamic comparator to enhance the speed in low supply voltages. The component mismatch in the additional circuitry of the comparator should be considered. Double-Tail is derived from the fact that the comparator uses one tail for input stage and another tail for latching stage. It has less stacking and therefore it can operate at lower supply voltages. The structure of double-tail dynamic comparator existing is based on this fact. This separationenables fast performance [10] over a wide common-mode and supply voltage range.

A novel double-tail low power comparator using FinFET is proposed which result in extensive power saving and gain, compared to existingcomparator [10].FinFET is a multigate device, shown in Fig. 1. The two gates of it maintain a greater control over the channel so many performance parameters can be altered. The most important characteristic of the FinFET is that it has a conducting channel wrapped by a thin silicon "fin" from which it gains its name. The effective channel length of the device determines thickness of the fin. The FinFET is a technology that is used within ICs. FinFETs are not available of the form of discrete devices. FinFET technology is becoming more global as feature sizes within integrated circuits fall and there is a growing need to contribute very much higher levels of integration with less power consumption within integrated circuits.

The rest of the paper is organized as follows. The section II investigates the existing dynamic comparator. The proposed comparator is discussed in Section III. Section IV shows theoperation of proposed double-tail comparator which is followed by conclusion inSectionV.

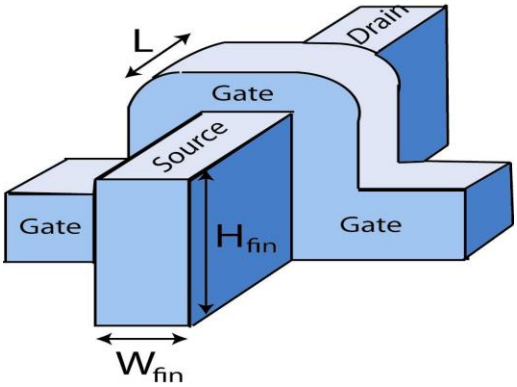

Fig. 1.Schematic of a FinFET.

II. EXISTING SYSTEM

The CMOS ICtechnology is being scaled down continuously and hasentered into the nanometerregion. The contraction of the CMOS technology has been widespread more aggressively with drastic thin sizes. This contraction of thedesign creates many significant challenges and reliability issuesin design which leads to augmented process variations, shortchannel effects, power densities and leakage currents etc. Very thin sized CMOS technologies [18] have been designed to be used inmany applications. Continuous reduction of channel lengthincreases the high speed devices in very large scale circuits.This steady miniaturization of transistor with each new generation of bulk CMOS technology has provided continual improvement in the performance of digital circuits. Due to the fundamental material and the process technology limitation, the scaling of bulk CMOS, however, faces significant challenges in the future. The 32 nm FinFET based transistors are used as a choice and solution for CMOS based technology with scaled device geometry. In these device structures, by limiting the off-state leakage, the effect of short-channel length can be controlled. Moreover, FinFETs has merits of reducining short channel effects, gate-dielectric leakage currents etc.

III. PROPOSED SYSTEM

FinFET is one of the promising and better technologies without compromising reliability and performance for its applications and the circuit design. This FinFET based transistors provide good trade off for power as well as for delay parameter.FinFETs has merit ofreducing short channel effects, gate-dielectric leakage currents etc.

A. Conventional Dynamic Comparator

The workingof the conventional dynamic comparatoris shown in Fig. 2. Theconventional dynamic comparatorcan be used in A/D converters having high inputimpedance, rail-to-rail output swing, and no static powerconsumption [11].

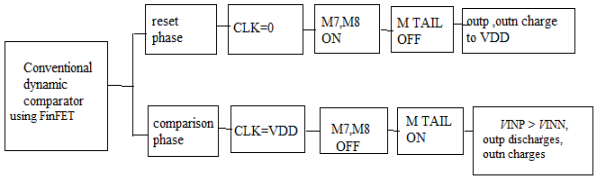

Fig. 2.Block diagram of the conventional dynamic comparator.

The schematic diagram of conventional dynamic comparator using FinFET is shown in Fig. 3. The comparator works on 2 modes, reset and decision making mode.During the reset phase, CLK = 0 and *M*tail is off, and reset transistors (*M*7 and *M*8) pullboth output nodes Out*n*and Out*p*to *V*DD to define a startcondition and to have a valid logical level during the phase. In comparison phase, CLK = *V*DD,and transistors *M*7 and *M*8 are off, where*M*tail is on. Output voltages (Out*p*, Out*n*), which has gone to *V*DD, start to discharge with differentdischarging rates depending on the corresponding input voltage (INN/INP). Consider whenVINP > VINN, at the time Out*p*discharges faster than Out*n*, hence when Out*p* falls to*V*DD–|*V*thp|before Out*n* thethe corresponding pMOS transistor (*M*5) will turn on initiating the latch regeneration caused by back-to-back inverters (*M*3, *M*5 and *M*4, *M*6). Thus, Out*n*pulls to *V*DD and Out*p*discharges to ground. If *V*INP < *V*INN, the circuits works vice versa.

The circuit has many merits such as high inputimpedance, rail-to-rail output swing, no static power consumption, and good robustness against noise and mismatch. It is possible to design large input transistorsto minimize theoffset.Due to parasitic capacitances of input transistors do not affect the switching speed of the output nodes. On the other side there are many demeritsto the circuit such as several stacking of transistors, a sufficiently high supply voltageis needed for a minimum delay time. Another demerit is the structure has only one current path, which is not favorable forregeneration.

B. Conventional Double-Tail Dynamic Comparator

As there are some drawbacks in conventional dynamic comparator a conventional double-tail comparator is used. The block diagram of conventional dynamic double-tail comparator using FinFET is shown Fig. 4. The schematic diagram is shown in Fig. 5. The structure has less stacking and therefore can works at lower supply voltages on comparing with the conventional dynamic comparator. The advantage of double-tail dynamic comparator is that there is a separate input gain stage and output latchstage. The grouping of inputand output stages as two distinct stages make this type of comparatorto have a lower and more stable offset voltage.

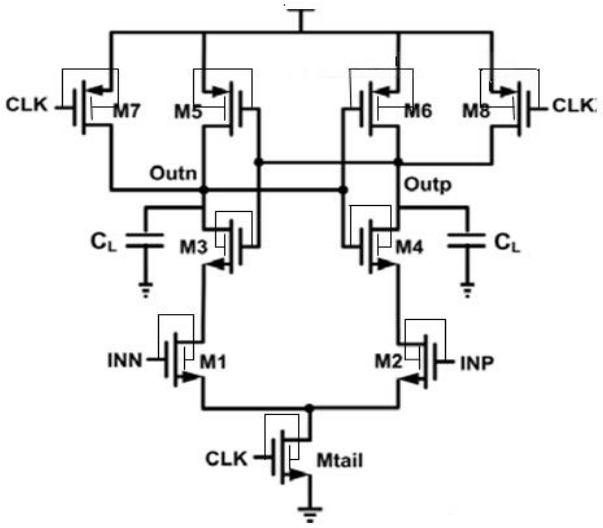

Fig. 3.Schematic diagram of conventional dynamic comparator usingFinFET.

The working of the double-tail comparator is based on 2 phase. In reset phase when CLK = 0, both tails such as Mtail1, and Mtail2 are off. During this time transistors M3 and M4 charge fn and fp nodes to VDD, which makes transistors MR1 and MR2 to discharge the outputnodes such as outp and outn to ground. In decision-making phase, when CLK =VDD, both tail turn on, M3-M4 turn off and voltagesat nodes fn and fp start to drop with the rate definedby IMtail1/Cfn(p) and a new voltage will build up. The intermediatestage formed by MR1 and MR2 passes new voltage to the crosscoupledinverters and also provides a good shielding betweeninput and output, which in turn leads to reduced noise. In reset phase when the nodes become charged from ground to VDD power consumption arises.

IV. PROPOSED DOUBLE-TAIL COMPARATOR

Fig. 6.Shows the schematicdiagram of the proposed double-tail comparator. It gives better result in low voltage operations, andis designed based on the double-tailstructure. Latch regeneration speed is increased by increasing voltage. Two control transistors (MC1 and MC2) are added to the first stage in parallel to M3/M4 transistors but in a cross coupled manner for the purpose of increasing speed.

A. Operation of proposed comparator

The working of the proposed comparator is as basic conventional double tail dynamic comparator but it has two input controlling transistors Mc1 andMc2 and two transitional stage transistors MR1 and MR2as shown in Fig. 5. In resetphase, when CLK= 0, both tailsare off, M3 and M4 pulls both fn and fp nodes to VDD, hence transistor Mc1 and Mc2 are at cut off state. The intermediate stage transistorsMR1 and MR2, reset both latch outputs to ground. In decisions making phase, when CLK= VDD, and both tail turn on. During this time the transistors M3 and M4 are in off state.

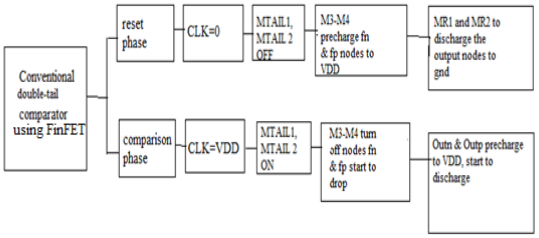

Fig. 4.Block diagram of the conventional double-tail comparator.

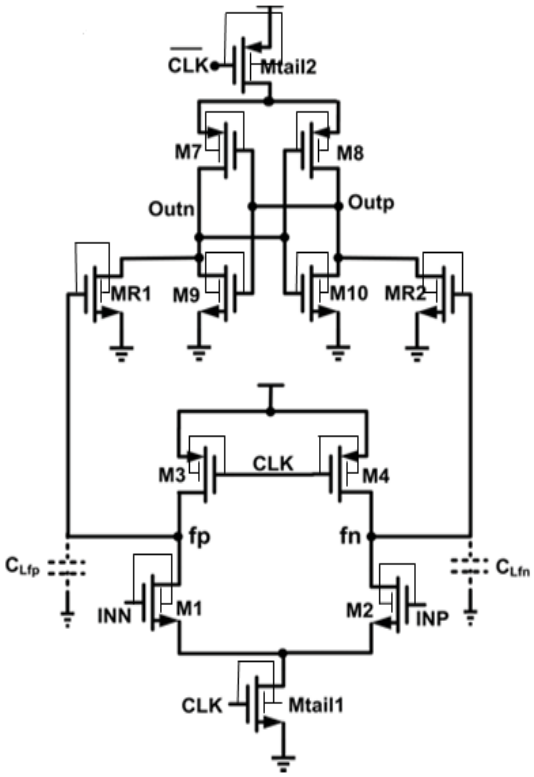

Fig. 5.Schematic of conventional double-tail comparator.

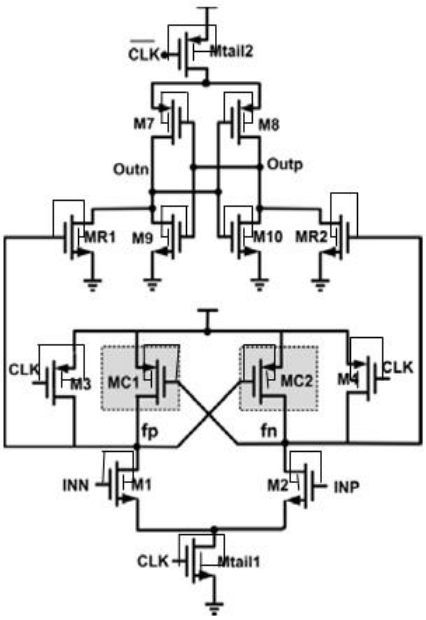

Fig. 6.Schematic of proposed double-tail comparator (main idea) using FinFET.

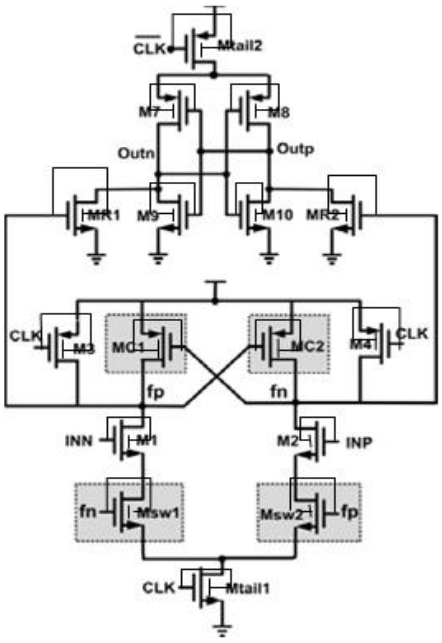

Fig. 7.Schematic of proposed double-tail comparator (final structure) using FinFET.

The Nodes fn and fp starts to drop at various rates according to the input voltages. Assume VINP > VINN, thus fn drops faster than fp. When fn goes on falling, the corresponding pMOS control transistor Mc1 starts to turn on, pulling node fp back to theVDD.When the comparator detects which node discharges faster, corresponding transistor turns on, pulling the other node back toVDD. Astime pass by, the difference in fn and fp increases in exponential manner leading to the reduction of latch regeneration time. When one of the control transistors gets turned on, a current from VDD is drawn to the ground through input and tail transistor, which leads to static power consumption. To overcome this drawback, two nMOS switches are used below the input transistor, Msw1 and Msw2 as shown in Fig. 7.

During the reset phase, both switches are closed and fn andfp start to fall with distinct discharging rates. When thecomparator detects, one of the fn/fp nodes is dischargingfaster, control transistor act as a way in which to increase the voltage difference. Assume that fp is pulling up to the *V*DDand fn should be discharged completely, hence the switch inthe charging path of fp will be opened,in order to prevent anycurrent drawn from *V*DD, but the other switch connected to fnwill be closed to allow the complete discharge of fn node.

When determining the size of tail transistor,it is necessary to ensure that the time it takes that one of the control transistors turns on must be smaller than start of regeneration. This can be easily overcomed by using low-threshold pMOS devices can as control transistors leading to faster turn on.In designing the nMOS switches, its drain-source voltage of the switches mustbe considered since it might limit the voltage headroom. This effect is suppressed by low-on-resistance nMOS switches. The effect of mismatch between control transistors is another basic issue. When determining the size of control, two issues should beconsidered. Firstly, the effect of threshold voltage mismatches and secondly the current factor mismatch. The threshold voltage and current factor mismatch is not negligible, when input voltage is small. Thisissue diminished by large input transistor.

In order to compare the modified comparator with the existing, conventional and double-tail dynamic comparators, all circuits have been simulated in a 32nm CMOS technology using LTSPICE. The pMOS and nMOS transistors in the circuits are sized tosatisfy its design issue. In order to measure the delay at theoutput nodes, CLK signal is set as the reference. The delay atthe output nodes (Outn and Outp) are measured with respectto the clock. The parameters used for the simulation are ΔVin, Vcm, VDD, INNand INP with the rise and fall time of the clockmaintained. Here the results of theexisting comparators in terms of delay, and power taken. From the simulation analysis it is clear that the proposed comparator consumes less power. The power consumption has been reduced significantly in the modified double-tail comparator using FinFET.

B. *Delay and Power analysis*

The proposed circuit has reduced power consumption when compared to the existing comparator structure. The reason is that in conventional double–tail topology using FinFET, both fn and fp nodes discharge to the ground during the decision making phase and each time during the reset phase they should be pulled up back to the VDD. But, in the proposed comparator, only one of the mentioned nodes (fn/fp) has to be charged during the reset phase. This

is due to the fact that during the previous decision making phase, depending on the status of control transistors, one of the nodes had not been discharged and thus less power is consumed. This can be seen when being compared with conventional topologies.

V. CONCLUSION

A performance comparison of existing and proposed double-tailcomparator in 32nm scaling technologies is carried out using the LTSPICE tool. The structures of both are analysed. On comparison of both structures in low supply voltage it is found that the proposed double-tail comparator has reduced power dissipation, delay and increased gain.

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