Design Of Efficient Low Power 9t Sram Cell

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Abstract

Memory is the most common part in CMOS IC's applications. The power consumption and speed of SRAMs are important issue that has led to multiple designs with the purpose of minimizing the power consumption during both read and write operations. In this paper, a novel 9T static random access memory (SRAM) cell design which consumes less dynamic power and has high read stability is predicted. This paper also includes the SRAM array structure, it consist of sense amplifier and address decoders. The Tanner EDA tool is used for observe the schematic solution at different technologies. Based on the results obtained when compared with the existing methods, by utilizing the above proposed method it is clearly observed that there is a decrease in power consumption and stability improvement of the memory cells.

1. Introduction

A SRAM cell consist of a latch, therefore the cell data is kept as long as power is turned on and refresh operation is not required for the SRAM cell. SRAM is mainly used for the cache memory in microprocessors, mainframe computers, engineering workstations and memory in hand held devices due to high speed and low power consumption. Each bit in an SRAM is stored on four transistors that form two cross-coupled inverters. The power consumption and speed of SRAM are important issue that has lead to multiple designs with the purpose of minimizing the power consumption during both read and write operations. High-performance on chip caches is a crucial component in the memory hierarchy of modern computing systems. In this technique each NMOS and PMOS transistor in the logic gates is split into two transistors are called Stack Technique [7]. Leakage current flowing through the NMOS transistor stack reduces due to the increase in the source to substrate voltage in the top NMOS transistor and also due to the drain to source voltage in the bottom NMOS transistor. This reduces the power dissipation in logic circuits. The proposed SRAM memory cell consumes lower power during read and writes operations compared to 6T conventional circuit. The ability of the cell to write properly and to have sufficient read noise margin is very important for sub threshold region. we examine many of such necessities for successful operation. Also, a new 9T SRAM combining the advantages of these circuits is proposed in the paper. A nine transistors (9T) SRAM cell configuration is proposed in this paper, which is amenable to small feature sizes encountered in the deep sub-micron/Nano CMOS ranges. Compared with the 8T and 10T cells of [1] and [2], the 9T scheme offers significant advantages in terms of power consumption. The conventional six transistor (6T) SRAM cell shows poor stability at very small feature size with low power supply. During the read operation, voltage division between the access and driver transistors causes the read stability to be very low. Hence in this paper, a 9T SRAM cell is proposed for high read stability and low power consumption. The proposed cell utilizes single bit-line (BL) for write operation, resulting in reduction of dynamic power consumption. During read operation, the data storage nodes are completely isolated from the bit lines, thus ornamental the read static noise margin.

Hence in this paper, a 9T SRAM cell is proposedfor high read stability and low power consumption [5]. The proposed cell utilizes single bit-line (BL) for write operation, resulting in reduction of dynamic power consumption. During read operation, the data completely isolated from the bit line, thus enhancing the read static noise margin.

2. Different Cell Designs

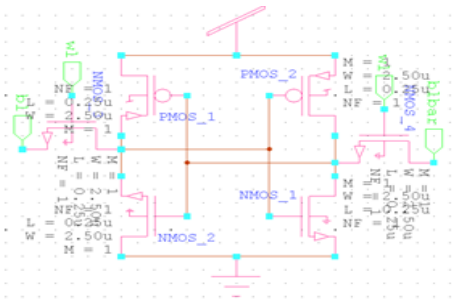

Figure 1 conventional 6T SRAM Cell

Figure.1 shows the conventional 6T SRAM cellwith transistor sizing in 125 nm CMOS technology.The schematic diagram of 6T SRAM cell is shown in Fig.1. Access to the cell is enabled by the word line (WL) which controls the two access transistors, in turn, control whether the cell should be connected to the bit lines: BL and BLB. They are used to transfer data for both read and write operations. While it's not strictly essential to have two bit lines, both the signal and its inverse are typically provided since it improves noise margins [11].

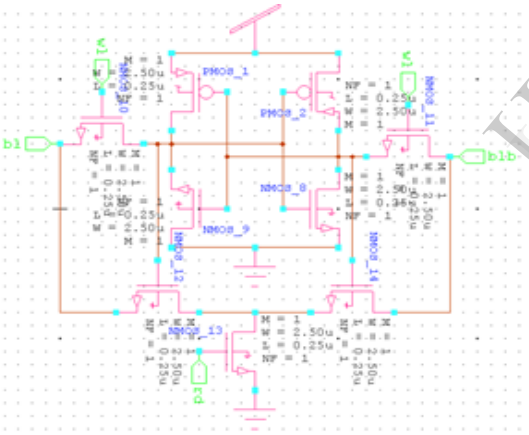

Figure 2 Schematic 9T SRAM Cell

Schematic of 9T SRAM cell is shown in the Fig. 2. This circuit shows reduced leakage power and enhanced data stability. The 9T SRAM cell completely isolates the data from the bit lines during a read operation. The idle 9T SRAM cells are placed into a super cutoff sleep mode, thereby reducing the leakage power consumption as compared to the standard 6T SRAM cells.

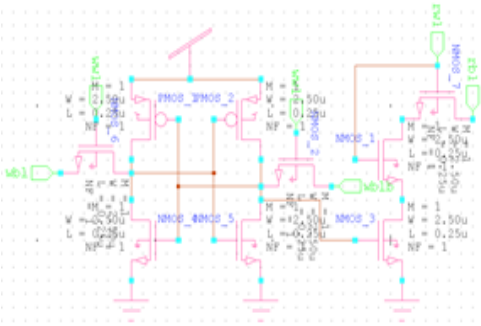

Figure 3 Bit Line Scheme

The optimal transistor sizing for this 9T SRAM cell considering stability, energy consumption and delay. A write bit line balancing scheme is proposed to reduce the leakage current of the SRAM cell. A 9T structure is to improve the SNM by separating the read access structures of the original 6T cell, thus making the read SNM equal to the hold SNM.An innovative precharging and bit line balancing scheme for writing operation of the 9T SRAM cell is also proposed for maximum standby power savings in an SRAM array.

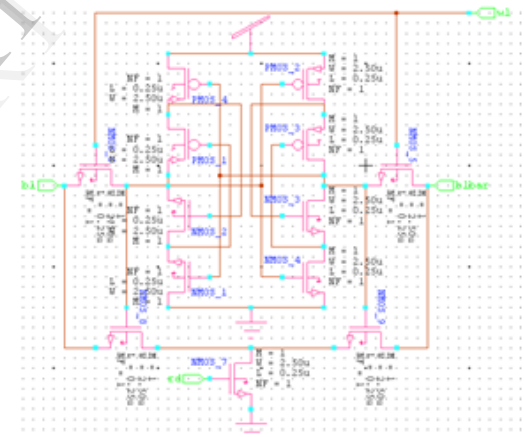

Figure 4 Stack Technique

Power consumption has become a critical designconcern for many VLSI systems [12]. Leakage current flowing through the NMOS transistor stack reduces due to the increase in the source to substrate voltage in the top NMOS transistor and also due to an increase in the drain to source voltage in the bottom NMOS transistor. This reduces the power dissipation in logic circuits. In this technique each NMOS and PMOS transistor in the logic gates are split into two transistors. A state with more than one transistor is off condition from a path from supply voltage to ground path consist of less leakage compared to the only one transistor off condition from a path from supply voltage to ground path.

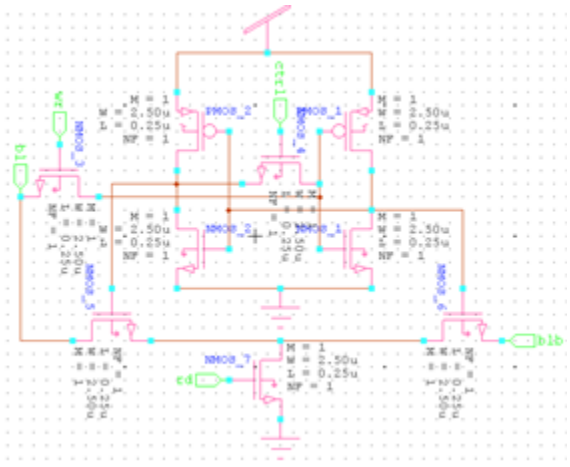

Figure 5 Improve Read Stability

The data in a conventional 6T SRAM cell as shown in figure.1, is most vulnerable to external noise due to the direct access of the data storage nodes by the access transistors (N3 and N4) connected to bit line (BL) and bit line bar (BLB) respectively[9]. During read operation, the voltage division between the access transistors and cross coupled inverters °fluctuate the storage node voltage, resulting in destructive read operation. The 9T SRAM cell in figure has an improved static noise margin (SNM) as compared to conventional 6T SRAM cell. The upper sub-circuit of the memory cell is essentially a 6T SRAM cell (composed of N1, N2, N3, N4, P1, and P2). The two write access transistors (N3 and N4) are controlled by a write signal (WR). The data is stored within this upper memory sub-circuit. The lower sub-circuit of the new cell is composed of the bit-line access transistors (N5 and N6) and the read access transistor (N7). The operations of N5 and N6 are controlled by the data stored in the cell. N7 is controlled by a separate read signal (RD). This structure completely isolates the bitlines from the data storage nodes during read operation hence improving the static noise margin (SNM).But during write operation it utilizes both bit line(BL) and bit line bar (BLB) capacitances for charging and discharging, resulting in increased dynamic power consumption.

In this 9T SRAM cell, the access transistor N4 is positioned in the feedback path and only access transistor N3 is connected to bit line (BL) to store data in the cell. Hence only one bit line capacitance (BL) will be charged and discharged during write operation which results in major reduction in dynamic power ingestion and at the same time the data stability of the 9T SRAM cell as in is also maintained. The upper sub circuit of the proposed cell has 6 transistors composed of N1, N2, P1, P2, N3 and N4. The 9T SRAM cell shown in figure has two write access transistors organized by a write signal (WR) connected to bit line (BL) and bit line bar (BLB).

The projected cell involves of one write access transistor (N3) coupled to BL, controlled by a write signal (WR), and one read and hold access transistor (N4) controlled by a control signal (CTRL). The lower sub circuit of the planned cell is collected of bit line access transistor (N5), bit line bar access transistor (N6) and read access transistor (N7) controlled by a read signal (RD) as shown in figure.5.During a write operation, WR signal is maintained at a high voltage (1" level). RD and CTRL signals are sustained at a low voltage (0" level). Hence the access transistors N4 and N7 are cut OFF and the write access transistor N3 is turned ON. To write a 1" to Node 1, BL is charged and 1" is forced to Node X through N3. This turns ON the transistor N2, forcing 0" into Node 2. This turns ON the transistor P1, forcing BL is discharged. Hence, to realize a write operation charging /discharging of only bit line (BL) is developed.

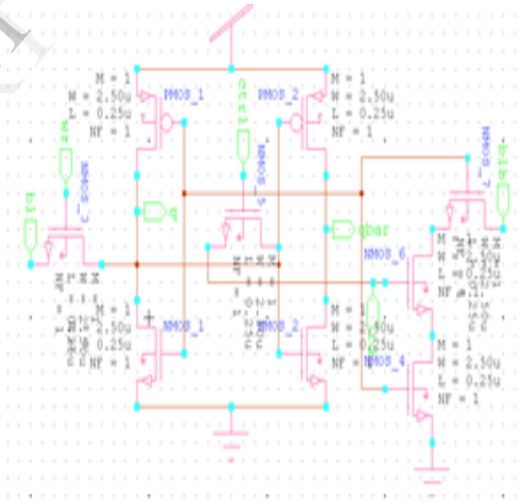

Figure 6 Proposed Design

Here only one single bit line capacitance (BL) will be charged and discharged during write operation which results in important reduction in dynamic power consumption and at the equal time the data stability of the 9T SRAM cell as in is also maintained. The planned cell maintains highly enhanced write margins and functionality, even when the PMOS are much stronger than the NMOS ones. This cell finishes full functionality deep into the sub-threshold section deprived of the need for special marginal circuits and techniques that require additional power, die area and timing schemes [6]. In

calculation, this circuit presents a low-leakage state, at which its static power is lower than any of the other enactments when operated at a similar supply voltage [3]. This is accomplished lacking any enactment degradation, while protection a reasonable SNM.

3. Simulation and Analysis

All the circuits have been simulated using BSIM 3V3 125nm technology on Tanner EDA tool with supply voltage ranging. The basic SRAM structure can be significantly optimized to minimize the delay and power at the cost of some area overhead. The optimization starts with the design and layout of the RAM cell, which is undertaken in consultation with the process technologists. For the most part, the thesis assumes that a ram cell has been adequately designed and looks at how to put the cells together efficiently. The power results values are calculated at different supply voltages and frequency. In our proposed memory design consume less power compared to design a 6T SRAM cell.

Table 1. Power comparison at 45nm technology

Different SRAM cells	POWER CONSUMPTION IN WATTS				
	VDD=1V	VDD=2V	VDD=3V	VDD=4V	VDD=5V
6T SRAM	6.2E-6	4.6E-5	1.2E-4	3.4E-4	3.3E-3
Bit Line Scheme	8.3E-6	7.6E-5	3.8E-4	4.8E-4	3.6E-3
Improve Read Stability	9.2E-6	2.1E-5	7.6E-4	6.1E-4	4.5E-3
Proposed Design	1.1E-7	6.8E-6	9.7E-6	7.3E-5	5.9E-4

Table 2. Power comparison at 250nm technology

Different SRAM Cells	Power Consumption in watts				
	VDD (1V)	VDD (2V)	VDD (3V)	VDD (4V)	VDD (5V)
6T SRAM	7.2E-4	1.1E-3	8.8E-4	2.2E-5	1.0E-5
Bit Line Scheme	6.6E-4	1.5E-3	8.2E-5	2.7E-5	1.2E-5
Improve Read Stability	6.4E-10	2.9E-10	8.9E-9	2.2E-9	1.4E-8
Proposed 9t Design	2.3E-11	8.7E-11	2.2E-10	5.1E-10	1.1E-9

Table 3. Power comparison at 180nm technology

Different SRAM cells	POWER CONSUMPTION IN WATTS				
	VDD=1V	VDD=2V	VDD=3V	VDD=4V	VDD=5V
6T SRAM	1.2E-11	4.6E-10	6.2E-10	2.4E-9	2.6E-9
Bit Line Scheme	2.3E-11	7.6E-11	9.7E-11	1.8E-10	1.6E-9
Improve Read Stability	1.2E-12	2.1E-11	4.6E-12	6.1E-12	4.5E-11
Proposed Design	1.1E-14	6.8E-14	9.7E-13	7.3E-13	5.9E-12

Table 4. Power comparison at different V_{th}

Different SRAM cells	POWER CONSUMPTION IN WATTS									
	VDD=1V		VDD=2V		VDD=3V		VDD=4V		VDD=5V	
	Vth(0.2)	Vth(0.4)	Vth(0.2)	Vth(0.4)	Vth(0.2)	Vth(0.4)	Vth(0.2)	Vth(0.4)	Vth(0.2)	Vth(0.4)
6T SRAM	6.7E-05	6.1E-06	1.0E-05	9.2E-04	6.9E-04	5.2E-04	1.4E-07	6.8E-08	5.2E-09	5.1E-09
Bit Line Scheme	7.7E-07	6.1E-10	3.3E-08	9.0E-09	1.6E-07	5.6E-08	4.1E-06	6.8E-09	7.7E-05	5.2E-08
Improve Read Stability	1.4E-11	1.1E-11	1.1E-11	1.2E-11	3.3E-90	3.4E-09	6.4E-09	1.0E-09	2.4E-09	4.3E-09
Proposed Design	1.5E-12	5.3E-11	5.3E-11	5.6E-11	1.3E-10	1.2E-10	2.6E-10	2.9E-10	5.6E-10	5.4E-10

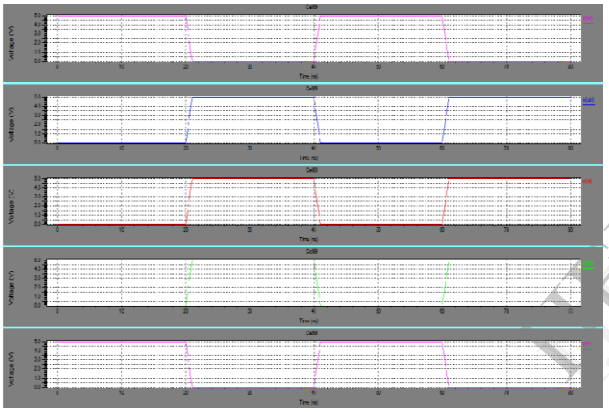

Figure 8: waveform for read operation of 9T SRAM

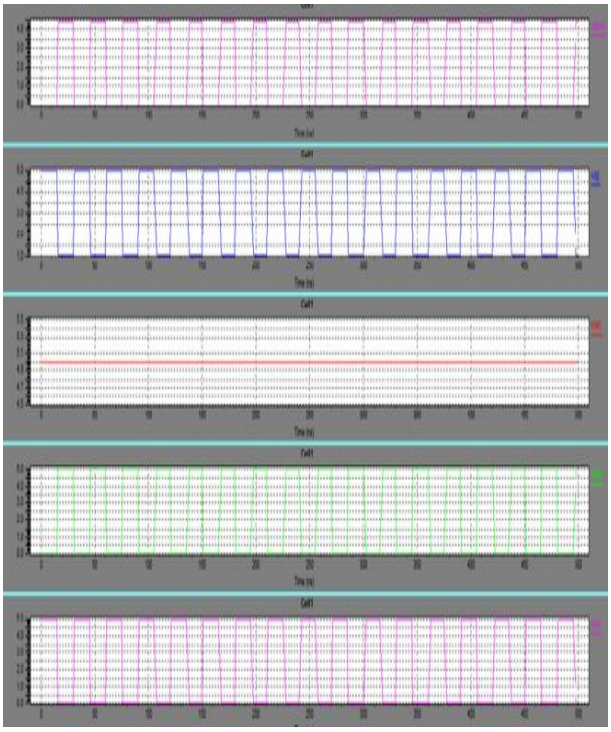

Figure 7: waveform for write operation of 9T SRAM

4. Conclusion

A Novel 9T SRAM cell is accessible in this paper for high read stability and low energetic power consumption. For low leakage and high speed circuits concern should be on both the factors speed and power. The proposed 9T SRAM cell provides two separate data access mechanisms for read and write operations. During the read operation, the data storage nodes are completely isolated from the bit lines, thereby improving the read SNM by twice as compared to the read SNM of the conventional 6T SRAM cell. During the write operation, the SRAM cell utilizes the charging/discharging of only one bit line (BL), resulting in reduction of dynamic power consumption as compared to conventional 6T SRAM cell. Different techniques have been analyzed to reduce the standby leakage current and dynamic power dissipation of the SRAM cell. In the proposed method 45nm and 125nm and 180nm technologies are analyzed using the Tanner EDA software and is used to analyze parameters such as power consumption, delay time and operating frequency. Based on the results obtained when compared with the existing methods, by utilizing the above proposed method it is clearly observed that there is a 45% decrease in power consumption and stability improvement of the memory cells.

5. References

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