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Design of Efficient Novel Multilevel Inverter by Reducing Harmonics with Reduces Number of Batteries and Switches

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***Abstract*-This paper proposes a 7 level and 15 level unequal voltage sources Multilevel Inverter (MLI) using Degree Modulated Pulse Generator (DMPG) Technique. This technique presents a modulation time control switching for generating the pulse for multilevel inverter and requires n dc sources to obtain (2^n– 1) output voltage level with a simple resistive load. This paper proposes a new concept of switching with reduced number of switches and batteries. There is comparison between 7 level and 15 level among output voltage and harmonic profile. Simulation work is observed by using the MATLAB/SIMULINK software which validated the proposed method and THD profiles are presented in FFT window.**

***Key Words*- Unequal voltage sources, Cascaded H-Bridge MLI, DMPG, Total Harmonic Distortion (THD), Switches and Batteries reduction**.

1. INTRODUCTION

The multilevel inverters are showing tremendous interest in the power industry as they requires huge power. Multilevel inverters are a suitable configuration to reach high power ratings and high quality output waveforms. As Inverter is a device which converters DC power into AC power by using electronic power switches[1]. Multilevel inverter gives three or more output levels[2]. The multilevel inverters are basically three types 1) Diode Clamped MLI, 2) Capacitor clamped MLI and 3) Cascaded H-bridge MLI. Multilevel inverters have many advantages. The main attractive features of MLI are as outlined are as1) Output voltages have extremely low distortion and low dv/dt. 2) They draw current with very low distortion. 3) They operate with a lower switching frequency. A popular topology for multilevel inverters is the cascaded H-bridge multilevel inverter which is based on the series connection of single phase H-bridge inverters with separate DC sources. In this, the output voltage waveform is nearly sinusoidal even without filtering. If the number of DC sources in single phase inverters is n, then the number of output levels will be (2n+1). Therefore an increase in n will increase the number of levels in the output. But for each added inverter four switching devices will be added.

Cascaded MLI topology proposed by reduced number of power switching devices as required for the same number of output levels in Cascaded H-bridge Multilevel Inverter topology[3]. It uses unequal number of battery sources in the inverter[4]. Here the MLI is operating as a half bridge for intermediate voltages and full bridge for maximum voltages, this concept provides a staircase waveform of seven levels and fifteen levels across R load. This paper deals with switching for fifteen level to obtain equal step multilevel inverter output with only ten switches and three unequal voltage sources. The modulation technique used here is Degree modulated pulse generator (DMPG)[5]. This modulation technique is based on degree generation, calculated through the output voltage divided into equal proportion. This paper also deals with comparison the voltage profile and total harmonic profile between 7 and 15 level MLI.

2. SEVEN LEVEL NOVEL MULTILEVEL INVERTER

In 7 level MLI total eight power switches are uses to control the output voltages. The proper switching combination makes its possible to get desired output voltage level. For maximum output voltage level $3V_{DC}$: switches S1, S3, Sa and Sd are ON and remainings are in OFF mode.

For $2V_{DC}$: switches S2, S3, Sa and Sd are ON and others are OFF.

For V_{DC} : switches S1, S4, Sa and Sd are ON and others are OFF. The remaining output level can be analyzed by seeing the table no. 1.

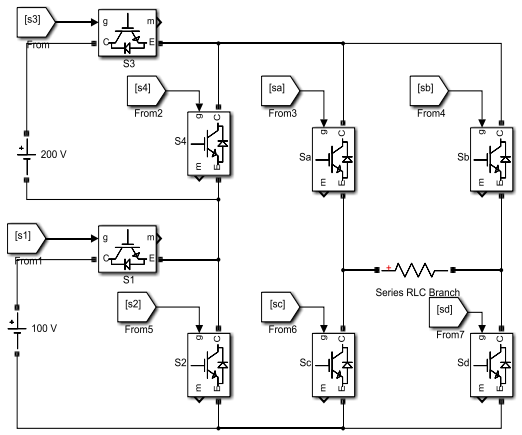

Figure 1:Proposed multilevel inverter with unequal sources for 7 level MLI

Table no, 1: Switching patter for 7 level MLI

Levels	S1	S2	S3	S4	Sa	Sb	Sc	Sd	VR_L
1	1	0	1	0	1	0	0	1	$3V_{DC}$
2	0	1	1	0	1	0	0	1	$2V_{DC}$
3	1	0	0	1	1	0	0	1	V_{DC}
4	0	0	0	0	0	0	0	0	0 V
5	1	0	0	1	0	1	1	0	$-V_{DC}$
6	0	1	1	0	0	1	1	0	$-2V_{DC}$
7	1	0	1	0	0	1	1	0	$-3V_{DC}$

3. FIFTEEN LEVEL NOVEL MULTILEVEL INVERTER

In 15 level MLI total ten power switches are uses to control the output voltage level. The proper switching combination makes its possible to get desired output voltage level. For maximum output voltage level $7V_{DC}$: switches S1, S3, S5, Sa and Sd are ON and remainings are in OFF mode. For $6V_{DC}$: switches S2, S3, S5, Sa and Sd are ON and others are OFF. For $5V_{DC}$: switches S1, S4, S5, Sa and Sd are ON and others are OFF. For $4V_{DC}$: switches S2, S4, S5, Sa and Sd are ON and others are OFF. For $3V_{DC}$: switches S1, S3, S6, Sa and Sd are ON and others are OFF. For $2V_{DC}$: switches S2, S3, S6, Sa and Sd are ON and others are OFF. For V_{DC} : switches S1, S4, S6, Sa and Sd are ON and others are OFF. The remaining output level can be analyzed by seeing the table no. 2.

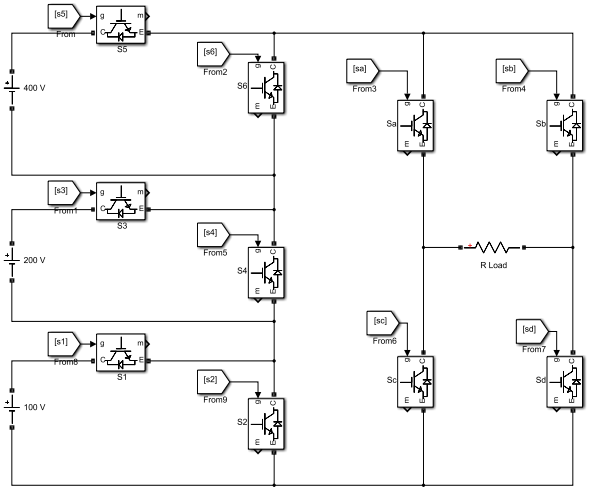

Figure 2: Proposed multilevel inverter with unequal sources for 7 level MLI

Table no. 2: Switching patter for 15 level MLI

Levels	S1	S2	S3	S4	S5	S6	Sa	Sb	Sc	Sd	VR_L
1	1	0	1	0	1	0	1		0	1	$+7V_{DC}$
2	0	1	1	0	1	0	1	0	0	1	$+6V_{DC}$
3	1	0	0	1	1	0	1	0	0	1	$+5V_{DC}$
4	0	1	0	1	1	0	1	0	0	1	$+4V_{DC}$
5	1	0	1	0	0	1	1	0	0	1	$+3V_{DC}$
6	0	1	1	0	0	1	1	0	0	1	$+2V_{DC}$
7	1	0	0	1	0	1	1	0	0	1	$+V_{DC}$
8	0	0	0	0	0	0	0	0	0	0	0V
9	1	0	0	1	0	1	0	1	1	0	$-V_{DC}$
10	0	1	1	0	0	1	0	1	1	0	$-2V_{DC}$
11	1	0	1	0	0	1	0	1	1	0	$-3V_{DC}$
12	0	1	0	1	1	0	0	1	1	0	$-4V_{DC}$
13	1	0	0	1	1	0	0	1	1	0	$-5V_{DC}$
14	0	1	1	0	1	0	0	1	1	0	$-6V_{DC}$
15	1	0	1	0	1	0	0	1	1	0	$-7V_{DC}$

4. SWITCHING AND CONTROL SCHEME

The modulation technique here used is Degree modulated pulse generator(DMPG) to develop the desired switching pulses to control the power switches. Here the first half cycle of output level analyzed and divided into equal segment to get the θ(degree) value. The simulink model for seven level MLI is given in figure 3 and the gate driver pulses are shown in figure 4a and 4b.

The simulink model for fifteen level is given in figure 5 and gate driver pulses are shown in figure 5a and 5b respectively.

To obtain equal step firing a seven level output is divided into 8 equal intervals. The value of degree (θ) of the entire half signal is 22.5. Therefore the degree interval for each state is given by $\theta = 22.5$

θ and Switches	S1	S2	S3	S4	Sa and Sd	Sb and Sc
0 - 22.5	0	0	0	0	0	0
22.5 - 45	1	0	0	1	1	0
45 - 67.5	0	1	1	0	1	0
67.5 - 90	1	0	1	0	1	0
90 - 112.5	1	0	1	0	1	0
112.5 - 135	0	1	1	0	1	0
135 - 157.5	1	0	0	1	1	0
157.5 - 180	0	0	0	0	0	0

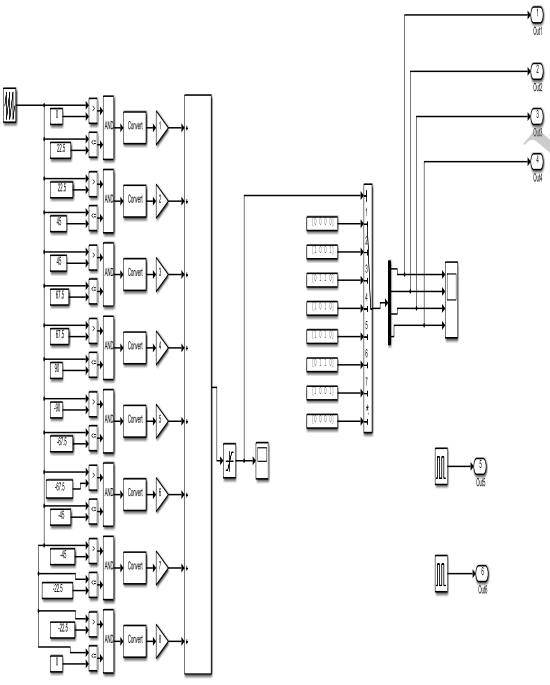

Figure 3:Simulink model for Gate driver circuit of 7 level MLI

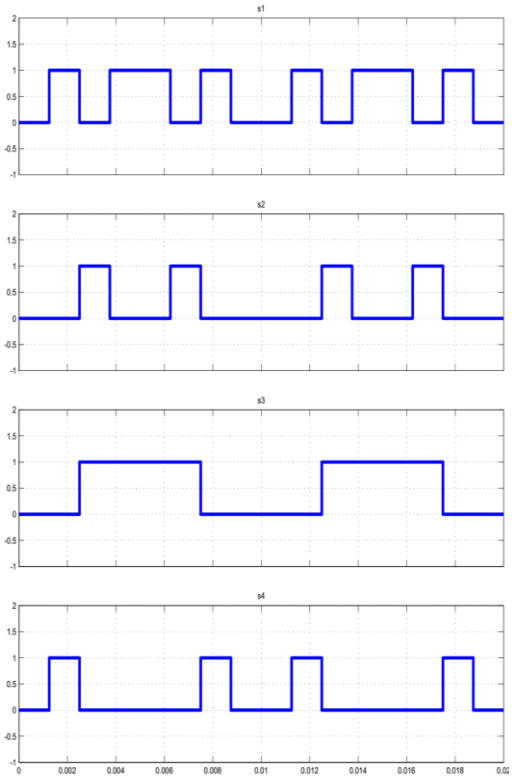

Figure 4.a: Gate Pulses for Power switches(S1,S2,S3,& S4) of 7 level MLI

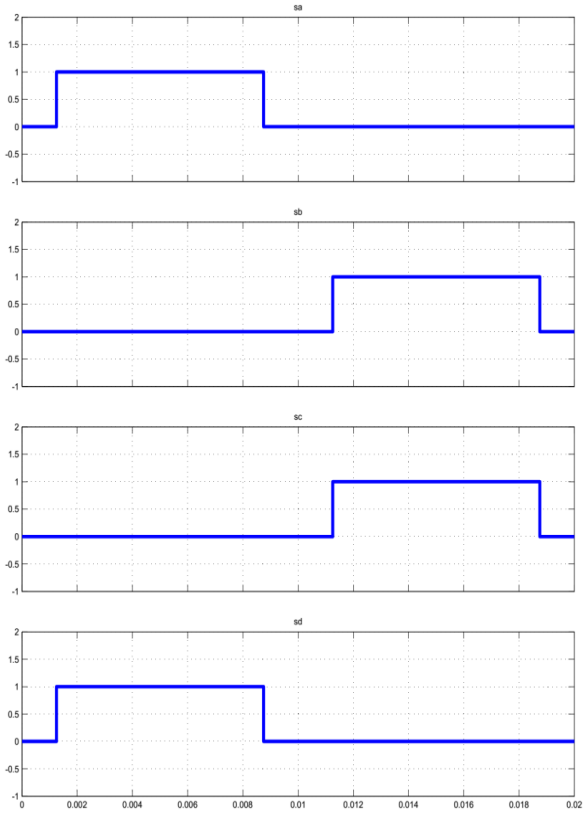

Figure 4.b: Gate Pulses for Power switches(Sa,Sb,Sc,& Sd) of 7 level MLI

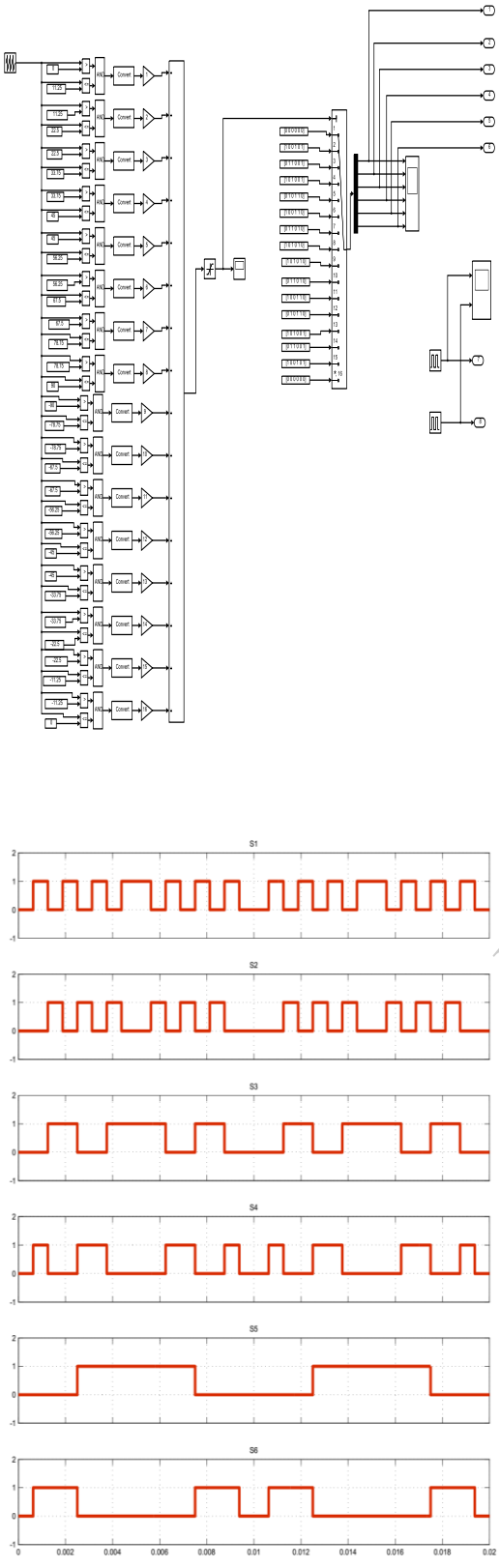

Figure 6.a: Gate Pulses for Power switches(S1,S2,S3,S4,S5,& S6) of 15 level MLI

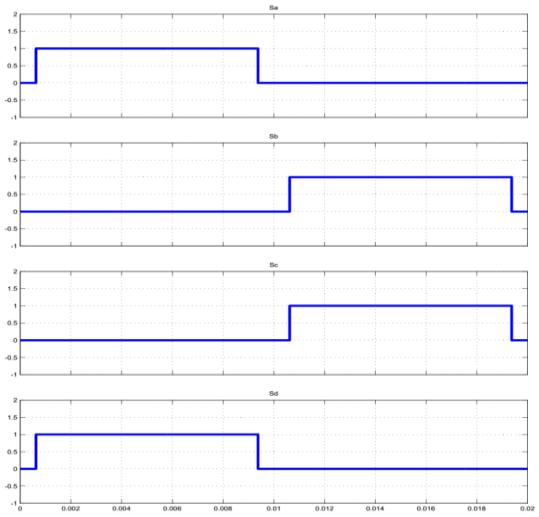

Figure 6.b: Gate Pulses for Power switches(Sa,Sb,Sc,& Sd) of 15 level MLI

5. COMPARISON

In this paper the output voltages of MLI for 7 level and 15 level are shown in figure 7 and 8 respectively. The total harmonic distortion profile is shown in figure 9 and 10 respectively. The detail comparison can be analyse as for the table no. 3.

The comparison of component between MLDCL Inverter and Novel MLI shown in table no 3. The novel multilevel inverter effectively reduces the number of switches and their gate drivers. On the Table no. 3 relation between the number of voltage sources and number of switches required in different inverters.

Table no.: 3 COMPONENT COUNT COMPARISON

Types of Inverter	No of level 2^n-1, n=1,2,3,...	No. of Batteries (Sources)	No. of switches
MLDCL Inverter with unequal source voltages	7	2	8
	15	7	16
	31	15	16
	63	31	20
Voltage switching for MLI with unequal sources (varying 2^n, n=0,1,2,....)	7	2	8
	15	3	10
	31	4	12
	63	5	14

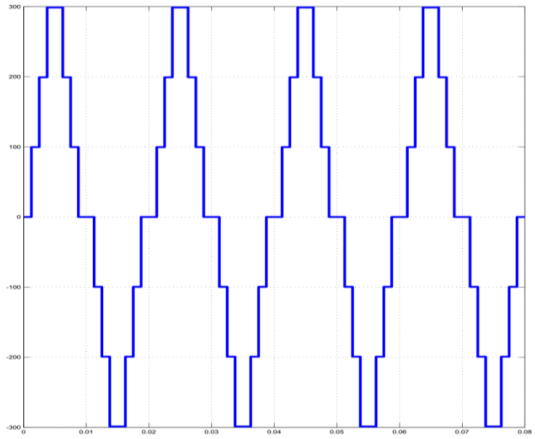

Figure 7: Output voltage of 7 level MLI

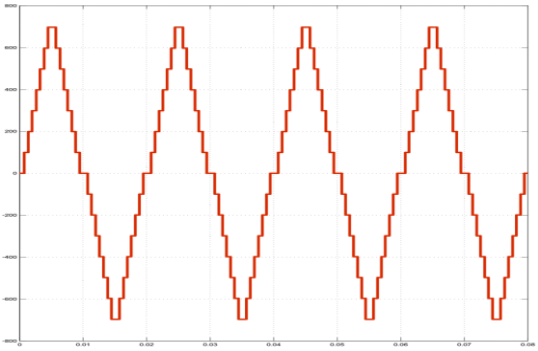

Figure 7: Output voltage of 15 level MLI

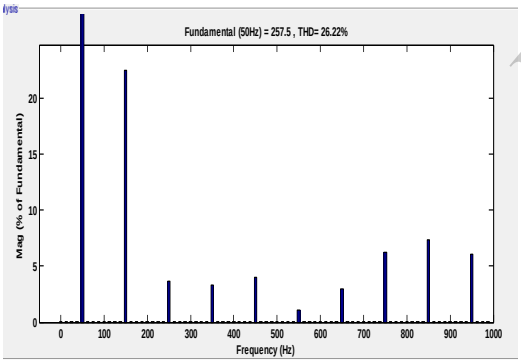

Figure 8: FFT window for 7 level MLI

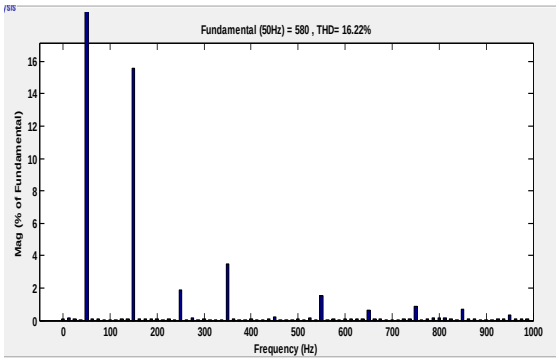

Figure 9: FFT window for 15 level MLI

Table no. 4: Comparison of THD's of 7 level and 15 level MLI

Novel MLI	Output Voltage Profile	Total Harmonic Distortion (THD)
7 Level	257.5	26.22%
15 Level	580	16.22%

6. CONCLUSION

In this paper a Multilevel Inverter with unequal voltage sources that required only two-battery sources for seven level and three-battery for fifteen level respectively. A seven level and fifteen level with equal step degree modulated switching control has been applied to obtain a multilevel ac output voltage. Multilevel Inverter with unequal voltage sources is simulated using MATLAB Simulink. The discussed Multilevel Inverter with unequal voltage sources needs least number of power switches than the other existing multilevel inverters for the same level of output waveform. As the number of levels increases in Multilevel Inverter with unequal voltage sources the number of switches, gate driver and batteries are reduced with better output waveform. The comparison between seven and fifteen level is analyzed. As the level is increased the harmonic profile is also reduced.

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