Design Of Energy Efficient CMOS Logic Circuits Using Adiabatic Logic

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Abstract

Energy efficiency is one of the most important features of modern electronic systems designed for high speed and portable applications. The power consumption of the electronic devices can be reduced by adopting different design styles. Adiabatic logic style is said to be an attractive solution for such low power electronic applications. This paper presents an energy efficient technique for digital circuits that uses adiabatic logic. The Energy dissipation in conventional CMOS circuits can be minimized through adiabatic technique. By adiabatic technique dissipation in PMOS network can be minimized and some of energy stored at load capacitance can be recycled instead of dissipated as heat. But the adiabatic technique is highly dependent on parameter variation. .This paper evaluates the inverter and multiplexer in different adiabatic logic styles and their results were compared with the conventional CMOS design. The simulation results indicate that the proposed technique is advantageous in many of the low power digital applications. It is find that adiabatic technique is good choice for low power application in specified frequency range.

Keywords: Adiabatic, Charge recovery, low power, energy efficient, digital circuits, sinusoidal power clock.

1. Introduction

Power consumption plays an important role in the present day VLSI technology. As many of the present day electronic devices are portable, they need more battery backup which can be achieved only with the low power consumption circuits that are internally designed in them. So energy efficiency has become main concern in the portable equipments to get better performance with less power dissipation. As the power dissipation in a device increases then extra circuitry is necessary to cool the device and to protect the device from thermal breakdown which also results in increase of total area of the device. In order to overcome these problems the power dissipation of the circuit is to be reduced by adopting different low power techniques. The less the power dissipation, the more efficient the circuit will be.

From the past few decades CMOS technology plays a dominant role in designing low power consuming devices. Compared to different logic families CMOS has less power dissipation which made it superior over the previous low power techniques. The power consumption in conventional CMOS circuit is due to switching activity of the devices from one state to another state and due to the charging and discharging of load capacitor at the output node.

The power dissipation in conventional CMOS design can be minimized by reducing the supply voltage, node capacitance value and switching activity. But reducing the values of these parameters may degrade the performance of the device. So an efficient low power technique other than CMOS is needed that has less power dissipation compared to CMOS which can be done by using adiabatic technique.

The present paper focuses on a novel energy efficient technique called adiabatic logic which is based on energy recovery principle. In this technique instead of discharging the consumed energy is recycled back to the power supply thereby reducing overall power consumption. In the present paper the performance of inverter and multiplexer is evaluated in different adiabatic logic styles and their results were compared with the conventional CMOS design. The performance of this device was evaluated in different adiabatic techniques of ECRL and PFAL. Simulation results shows that the proposed technique is efficient over the conventional CMOS design in terms of power dissipation.

2. CMOS DESIGN

CMOS is the basic building block of many of the digital circuits. The CMOS circuit itself acts as an inverter. It can be realized as a combination of PMOS in the pull up section whose source is connected to power supply and NMOS in the pull down section whose source is connected to ground and the output is taken across the drain junction of the two devices. The CMOS circuit has less power dissipation when compared to many of the previous VLSI families

of RTL, TTL and ECL. The power consumption in CMOS is due to the switching activity of the transistors from one state to another state, charging and discharging of the load capacitance and frequency of operation.

2.1 INVERTER

The basic CMOS inverter circuit is shown in figure 1

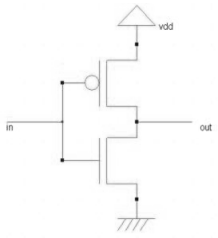

Fig. 1: CMOS inverter

The operation of the circuit can be evaluated in two stages of charging phase and discharging phase. During the charging phase, the input to the circuit is logic LOW. During this phase, the PMOS transistor conducts and NMOS transistor goes in to OFF state which charges the output value to power supply results in logic HIGH output. The equivalent circuit consists of a resistor in series with the output load capacitance which shows a charging path from power supply to output terminal. Here the resistor acts a PMOS ON resistor.

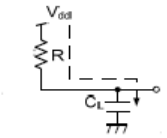

Fig. 2: Equivalent circuit for charging process in CMOS

During the discharging phase, the input to the circuit is logic HIGH. During this phase, the NMOS transistor conducts and PMOS transistor goes into OFF state which results in a discharging path from output terminal to ground. The value that is stored at the output during the charging phase discharges towards the ground results in logic LOW output. The equivalent circuit consists of a resistor in series with output terminal to ground. Here the resistor acts as NMOS ON resistor.

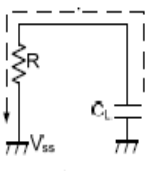

Fig. 3: Equivalent circuit for discharging process in CMOS

From the operation of the CMOS design it is evident that during the charging process, the output load capacitor is charged to Q = CLVdd and the energy stored at the output is (½)CLVdd2. During the discharging phase, the amount of energy dissipated is also (½)CLVdd2. So the total amount of energy dissipated during the charging and discharging phases is

$$E_{dissipated} = CLVdd^2 \quad (1)$$

2.2 MULTIPLEXER

A multiplexer as shown in figure 4 is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. A multiplexer of 2n inputs has n select lines, which are used to select which input line to send to the output. Multiplexers are mainly used to increase the amount of data that can be sent over the network within a certain amount of time and bandwidth. A multiplexer is also called a data selector.

An electronic multiplexer makes it possible for several signals to share one device or resource, for example one A/D converter or one communication line, instead of having one device per input signal.

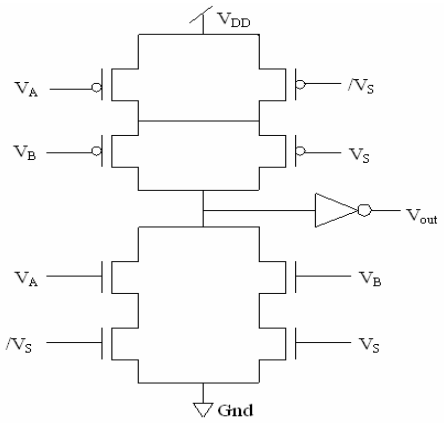

Fig. 4: CMOS multiplexer

An electronic multiplexer can be considered as a multiple-input, single-output switch. The schematic symbol for a multiplexer is an isosceles trapezoid with the longer parallel side containing the input pins and the short parallel side containing the output pin.

The power dissipation of CMOS can be reduced by minimizing the supply voltage, node capacitance and switching activity to some extent. But reducing the values of these parameters may suffer from some disadvantages. Reducing the load capacitance is strongly limited by the technology. Reducing the

supply voltage may degrade the performance of the device. Reducing the supply voltage may also suffer from leakage problems.

In order to overcome these problems an efficient low power technique called adiabatic logic is explained in this paper.

3. ADIABATIC LOGIC

The word ADIABATIC is derived from the Greek word "adiabatos", which means there is no exchange of energy with the environment and hence no energy loss in the form of heat dissipation. Adiabatic logic is commonly used to reduce the energy loss during the charging and discharging process of circuit operation. Adiabatic logic is also known as "energy recovery" or "charge recovery" logic. As the name itself indicates that instead of dissipating the stored energy during charging process at the output node towards ground it recycles the energy back to the power supply thereby reducing the overall power dissipation and hence the power consumption also decreases. The adiabatic logic uses AC power supply instead of constant DC supply; this is one of the main reasons in the reduction of power dissipation.

The adiabatic logic can be explained with the help of basic inverter circuit

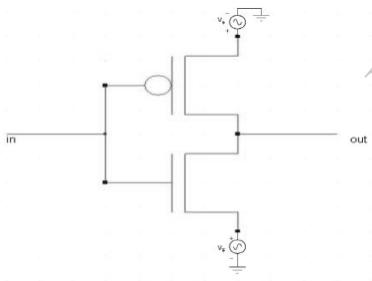

Fig. 5: Adiabatic inverter

The adiabatic inverter circuit can be constructed using CMOS inverter with two AC power supplies instead of DC supply. The power supplies are arranged in such a way that one of the clock is in phase while the other is out of phase with the first one. The operation of the adiabatic inverter can be explained in two stages. During the charging phase, the PMOS transistor conducts and NMOS transistor goes into OFF state which charges the output load capacitor towards the power supply results in logic HIGH output.

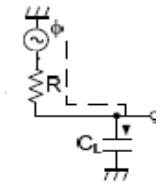

Fig. 6: Equivalent circuit for charging process in adiabatic inverter

During discharging phase, the NMOS transistor conducts and PMOS transistor goes into OFF state. Instead of discharging the stored value at the output towards ground, the energy is recycled back to the power supply. Its equivalent circuit consists of a resistor in series with output load capacitance and power supply.

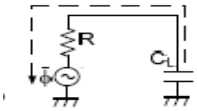

Fig. 7: Equivalent circuit for charge recovery process in adiabatic inverter

The charging process and the charge recovery process are efficient only when the charging voltage is varying one. Lower the rate of charging, lesser the power drawn from the supply voltage.

4. ADIABATIC TECHNIQUES

Adiabatic logic has a different logic style which helps in the reduction of the power dissipation of the circuit. The present paper explains basic CMOS circuits using some of the important adiabatic techniques.

4.1 ECRL

Efficient charge recovery logic consists of two cross couple PMOS transistors in the pull up section where as the pull down section is constructed with a tree of NMOS transistors. Its structure is similar to Cascade Voltage Switch Logic (CVSL) with differential signalling. The logic function in the functional block can be realized with only NMOS transistors in the pull down section. The basic inverter and full adder in ECRL logic can be constructed as

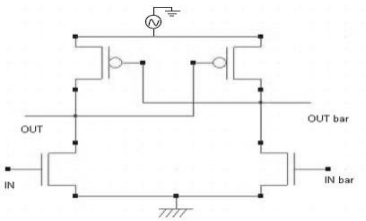

Fig. 8: ECRL inverter

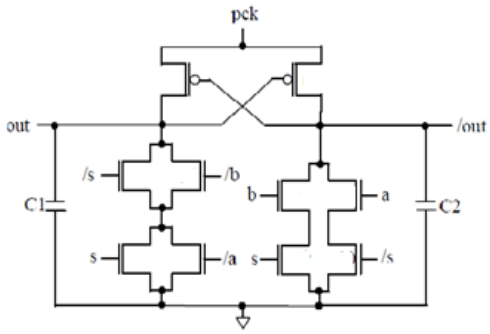

Fig. 9: ECRL Multiplexer

4.2 PFAL

The Positive Feedback Adiabatic Logic is a partial energy recovery circuit. It is also known as PAL-2N (Pass transistor Adiabatic Logic). The core of PFAL logic is a latch made up of two PMOS and two NMOS transistors that avoid logic level degradation on the output nodes. The logic function in the functional block can be realized with only NMOS transistors connected parallel to the PMOS transistors. The primary advantage of PFAL over ECRL is that the functional blocks are in parallel with the PMOSFETs forming transmission gate. It also has the advantage of implementing both the true function and its complimentary function.

Using PFAL, the basic inverter and multiplexer can be constructed as

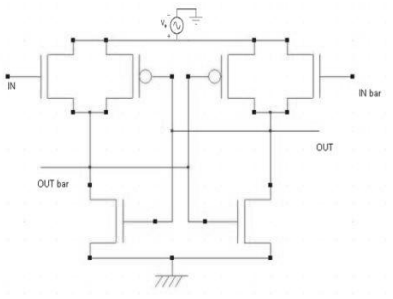

Fig. 10: PFAL inverter

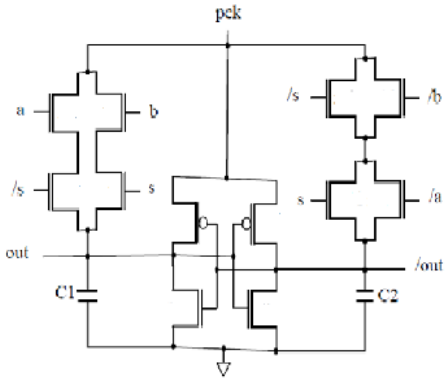

Fig. 11: PFAL Multiplexer

5. SIMULATION RESULTS

The simulation results were verified using PSPICE software and designed in Mentor Graphics IC Design Architect in Standard TSMC 0.35 µm CMOS Technology was simulated in ELDO Simulator. The simulation results of inverter and multiplexer in conventional CMOS design and different adiabatic logic design styles were presented in this section.

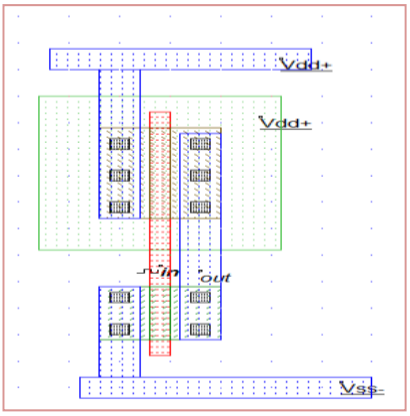

Fig. 12: Layout of cmos inverter

Fig: 12 shows the layout of CMOS Inverter without any DRC errors. In this design for drawing the layout only one metal layer is used.

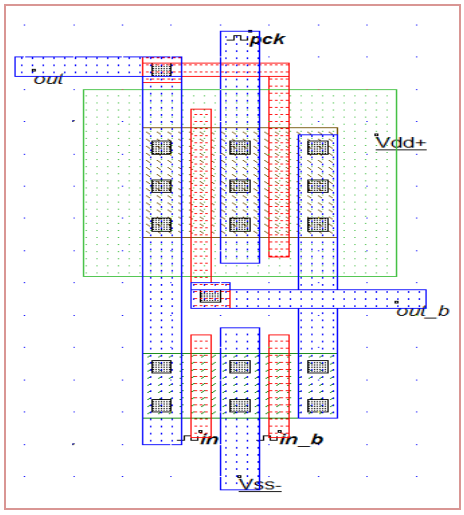

Fig 13: ECRL INVERTER LAYOUT

Fig: 13 shows the layout of ECRL Inverter without any DRC errors. In this design for drawing the layout only one metal layer is used.

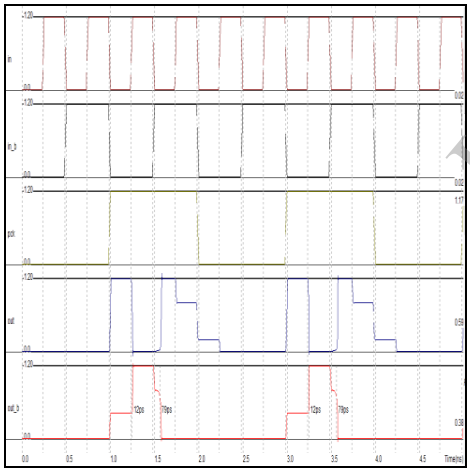

Fig 14: Simulated waveforms of ECRL Inverter

Fig. 14 shows the simulated waveforms of ECRL Inverter, where the uppermost two signals indicate input signals, the bottom signal indicate power clock and the last two signals are output and its complimentary

Fig: 15 shows the layout of ECRL Multiplexer without any DRC errors. In this design for drawing the layout only one metal layer is used.

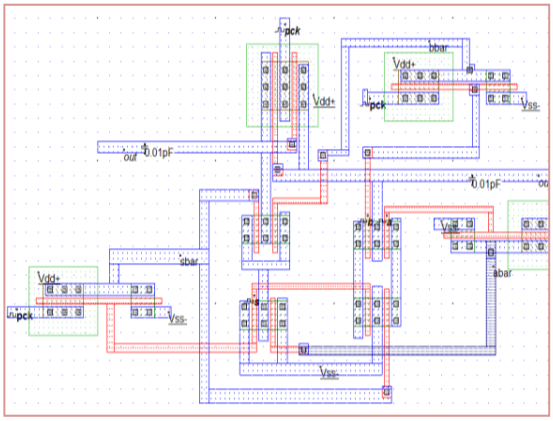

Fig:15: ECRL MULTIPLXER LAYOUT

Fig.16 shows the simulated waveforms of ECRL multiplexer, where the uppermost two signals indicate input signals, the bottom signal indicate power clock and the last two signals are outputs and its Complimentary signal.

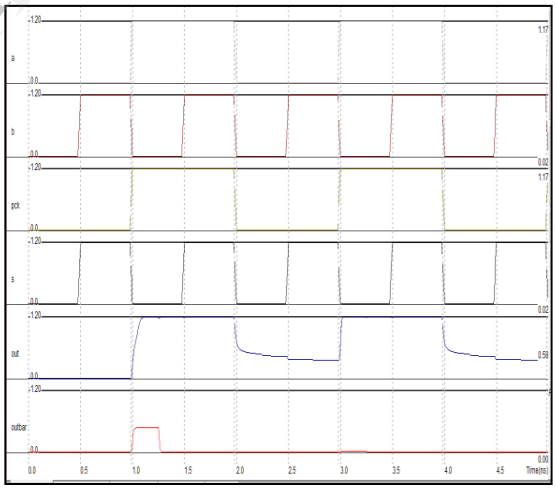

Fig 16: Simulated waveforms of ECRL Multiplexer

Fig: 17 Shows the layout of PFAL Inverter without any DRC errors. In this design for drawing the layout only one metal layer is used

Fig.18 shows the simulated waveforms of PFAL Inverter, where the uppermost two signals indicate input signals, the bottom signal indicate power clock and the last two signals are output and its complimentary signal.

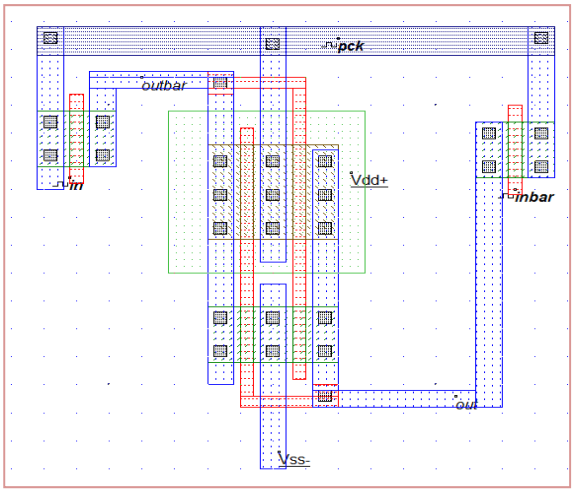

Fig:17: PFAL INVERTER LAYOUT

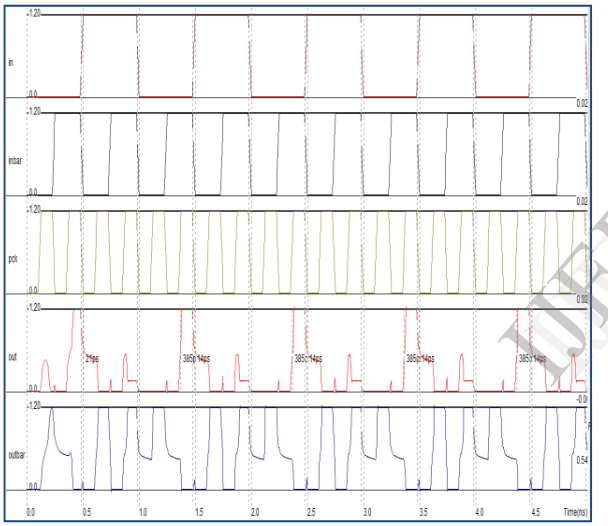

Fig 18: Simulated waveforms of PFAL Inverter

Fig: 19. Shows the layout of PFAL Multiplexer without any DRC errors. In this design for drawing the layout only one metal layer is used.

Fig.20 shows the simulated waveforms of PFAL Multiplexer , where the uppermost two signals indicate input signals, the bottom signal indicate power clock and the last two signals are output and its complimentary signal.

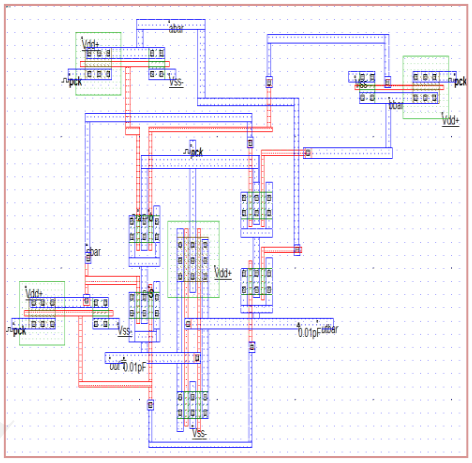

Fig 19: PFAL MULTIPLEXER LAYOUT

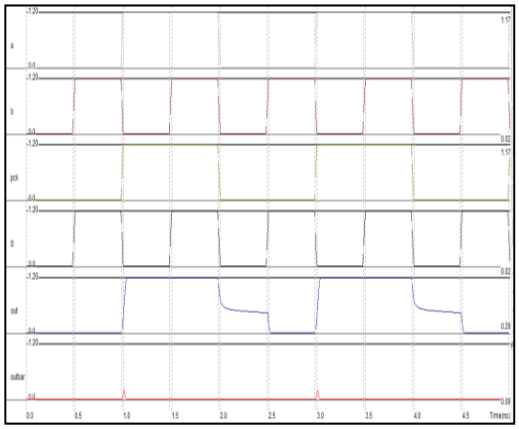

Fig 20: Simulated waveforms of PFAL Multiplexer

The below tables shows the comparison of CMOS, ECRL and PFAL Inverter and Multiplexer.

PARAMETER	POWER DISSIPATION	AREA(L*B)
CMOS INVERTER	3.703uw	6.415um^2
ECRL INVERTER	0nw	9.968um^2
PFAL INVERTER	0nw	19.98um^2

Table: 1.Comparison Of CMOS, ECRL And PFAL INVERTER

PARAMETER	POWER DISSIPATION	AREA(L*B)
CMOS 2:1 MULTIPLEXER	17.753uw	125.01um^2
ECRL 2:1 MULTIPLEXER	0nw	129.11um^2
PFAL 2:1 MULTIPLEXER	0nw	146.11um^2

Table: 2.Comparison Of CMOS, ECRL And PFAL MULTIPLEXERS.

Tables show that the power dissipation of different adiabatic logic styles is lesser than the conventional CMOS design. The power supply that is given to the adiabatic circuits is also lesser than the conventional CMOS design.

6. CONCLUSION

This paper proposes energy efficient adiabatic logic for digital circuits. The comparison has been done for different parameters of inverter and multiplexer in different adiabatic logic styles and CMOS design. The results show that the proposed adiabatic logic has less power dissipation compared to conventional CMOS design and it also uses less power supply. These advantages made this logic more convenient for energy efficient digital applications.

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